Electron transport via a few grain boundaries in heavily doped polycrystalline-silicon point contact devices

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Polycrystalline-silicon (poly-Si) nanowires have been used as a building block for single-electron devices. In the poly-Si nanowires, individual silicon grains and grain boundaries (GBs) act as an electron island and a tunnel junction, respectively. Apparently the size of the silicon grains should be reduced to as small as few nanometers to make the charging energy of the islands large enough to observe Coulomb blockade (CB) effects. Therefore, great efforts have been made to form very thin poly-Si films with a small grain size of < 10 nm [1], [2]. On the other hand, the properties of the GBs as a tunnel barrier have not been studied in detail, and there has been no clear guideline to optimise the GBs in terms of high temperature CB device operation. The aim of this work is to clarify the relationship between the microscopic properties of the GB tunnel barriers and the CB operation of the devices, which is derived from the experimental results on the electron transport via individual GBs.

For this purpose, we have fabricated heavily doped poly-Si point contact (PC) devices where both length and width of the channel are as small as the grain size (see the inset of Fig. 1). A 50 nm-thick heavily phosphorus-doped poly-Si film was formed by solid-phase crystallisation of an amorphous silicon film at 850℃ for 30 min in an Ar ambient. Doping concentration of the film was estimated to be 10^{20} cm^{-3} by using process simulation. Scanning electron microscope image of the Secco etched poly-Si film is shown in Fig.1, indicating that the grain size ranges from 20 nm to 150 nm. We have designed the length and width of our PC devices to be from 30 to 50 nm so that the devices may contain either no GB or a few GBs at most (see Fig. 2). The PC devices with side gates were fabricated with e-beam lithography and reactive ion etching. For comparison, PC devices with an oxidation process at 1000℃ for 15 minutes were also fabricated.

Current-voltage (I_{ds}-V_{ds}) characteristics of the PC devices have been measured at temperatures between 19K and 300K (see Fig. 3), and the GB potential barrier height V_B was evaluated from the temperature dependence of the resistivity (see Fig.4). The PC devices without oxidation showed non-linear I_{ds}-V_{ds} characteristics for about 33% of the fabricated devices while the rest of the devices exhibited linear characteristics. The observed non-linear characteristics are simply attributed to the potential barriers of the GBs in the PC region because they exhibit no CB oscillation. It is found that V_B decreases with increasing the channel width and increases with increasing the channel length, indicating that electron transport in poly-Si is controlled by percolation conduction through a few GBs with distributed barrier heights.

On the other hand, clear CB has been observed for the PC devices with oxidation (Fig.5). The CB oscillation was observed at temperature up to 40K, indicating that the oxidation of poly-Si increases tunnel barrier height at GBs due to enhanced oxidation along GB and shrunk the size of grains (islands) due to surface oxidation. Temperature dependence of the threshold voltage V_T measured for the PC devices with oxidation is plotted in Fig. 6: V_T is defined as voltage difference between the intersections of the extrapolated linear current with the horizontal axis. At low temperatures V_T represents CB gap given by e/C_Σ where C_Σ is a total capacitance of the grain. By increasing temperature, V_T decreases steeply due to disappearance of the CB effects around 40K, and then approaches a constant value of about 35 meV at higher temperatures, which is basically determined by the effective GB potential barrier height.

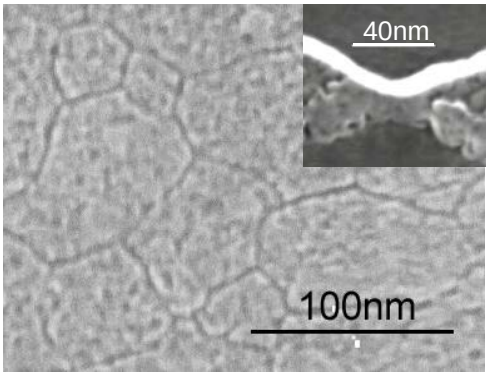

Fig.1 Scanning electron microscope (SEM) image of a Secco etched poly-Si film. GBs are clearly delineated. The inset shows point contact device with W/L=30nm/30nm fabricated in poly-Si layer.

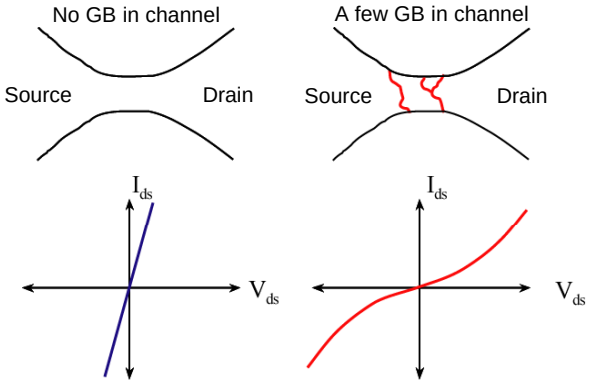

Fig.2 Schematic drawings of electrical characteristics for the PC devices without GB in channel and with a few GBs in channel.

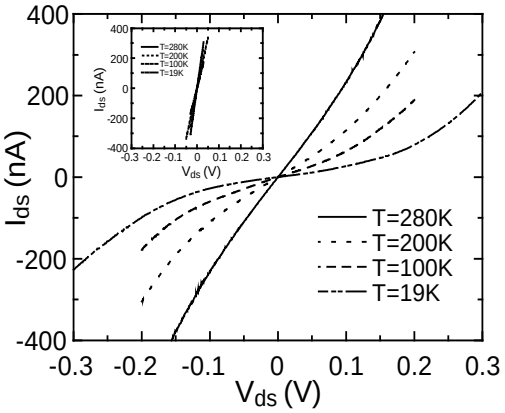

Fig. 3 Nonlinear I_{ds}-V_{ds} characteristics for the PC device with W/L=40nm/50nm. The inset shows linear I_{ds}-V_{ds} characteristics for the PC with same dimension.

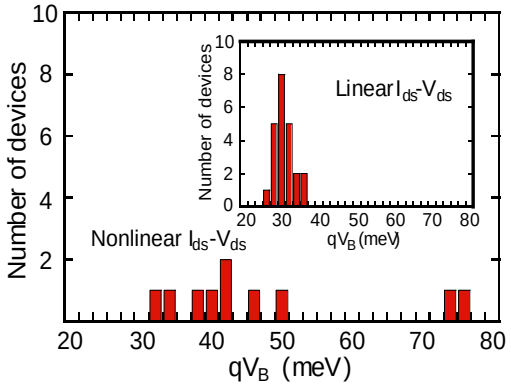

Fig.4 Distribution of potential barrier height qV_B for the device with nonlinear I_{ds}-V_{ds} characteristics. The inset shows that for the device with linear I_{ds}-V_{ds} characteristics.

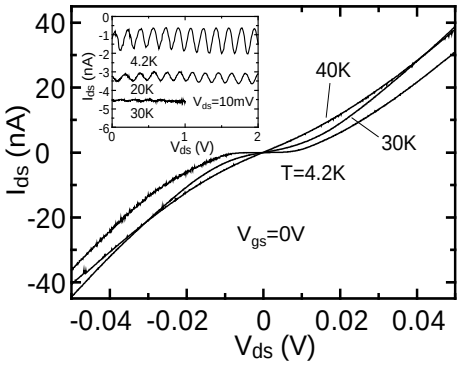

Fig.5 I_{ds}-V_{ds} characteristics for the oxidized PC device with W/L=40nm/50nm. The inset shows I_{ds}-V_{gs} curves. The Coulomb blockade oscillations were observed up to 40K.

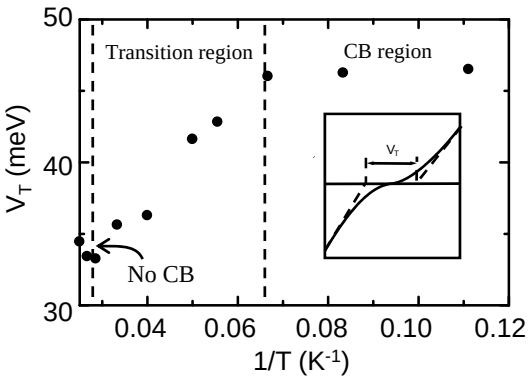

Fig.6 Temperature dependence of threshold voltage V_T for the PC devices with W/L=40nm/50nm. V_T was defined as voltage difference between the intersections of the extrapolated ON current with the horizontal axis.

Reference:

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[2] Y. T. Tan, T. Kamiya, Z. A. K. Durrani and H. Ahmed: To be published in Appl. Phys. Lett. on 19 Feb. 2001