Analysis of multi-phase clocked electron pump circuits

Shuhei Amakawa
Microelectronics Research Centre, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, United Kingdom
Phone: +44-1223-337493, FAX: +44-1223-337706, e-mail: sa264@cam.ac.uk

Hiroshi Mizuta and Kazuo Nakazato
Hitachi Cambridge Laboratory, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, United Kingdom
Phone: +44-1223-442903, FAX: +44-1223-467942, e-mail: mizuta@phy.cam.ac.uk

Pump circuits consisting of single-electron transistors are analyzed in which electrons are pumped by multi-phase clock pulses. The operation of this type of pump was experimentally demonstrated by Tsukagoshi *et al.*[1] The pump contains three or more multiple-tunnel-junction (MTJ) transistors as shown in Fig. 1. The structure necessarily leads to the clocking-gate capacitances $C_{\mathrm{G}i}$ being much greater than other capacitances, and therefore each component transistor may be regarded as being voltage-biased.[2] The pump might possibly be useful for constructing logic circuits, such as binary-decision-diagram (BDD) circuits.[3] To explore the possibility, the pump's charge transport mechanism and power dissipation is studied using the semiclassical model.

Each MTJ transistor is approximated with a two-junction single-electron transistor as shown in Fig. 1(b)[2] and the pump is assumed to be uniform. Because of the comparatively large $C_{\mathrm{G}i}$, we may analyze the pump circuit using the Coulomb blockade stability diagrams of each individual transistor. Electron pumping at the low temperature limit can be qualitatively understood with the use of stability diagrams. In the case of the four-transistor pump in Fig. 1, electrons are supposed to flow from the left to the right. However, some electrons might flow in the reverse direction and reduce the net current, consuming extra energy in vain. Electron flow should be rectified for efficient pump operation. This can be achieved by properly choosing the side-gate biases of "edge transistors" (TR1 and TR4) while setting all other side-gate biases to zero volts. In Fig. 2(a), the relevant node-voltages are plotted on stability rhomboids, under well-chosen V_{g1} and V_{g4}. In this condition, no stability borders for reverse tunneling are crossed, and hence electrons flow only in one direction. When V_{g1} and V_{g4} are swept, the optimal condition occurs around the current maxima, where the power is not maximal. The net number of electrons N_{c} is approximately $N_{\mathrm{c}} \approx \{V_{\mathrm{p}} - [\phi_1(\mathrm{A}) - \phi_1(\mathrm{D})]\}/\delta\phi$. The estimate by this expression gives $N_{\mathrm{c}} \simeq 46.7$, and the simulation result is $N_{\mathrm{c}} \simeq 45.4$. The power dissipation due to tunneling is $P = f \times N_{\mathrm{c}} e \times \sum_i V_{\mathrm{diff}}^{(i)}$ where $V_{\mathrm{diff}}^{(i)}$ is the voltage drop across the ith transistor when that is conducting. The estimated power is $P \simeq 0.6\,\mathrm{pW}$. The simulation result is also $P \simeq 0.6\,\mathrm{pW}$. The charge transfer mechanism in pumps with more transistors can be understood in the same way.

The charge transport becomes much more involved at higher temperatures, and the analysis using the stability diagrams is less effective. Qualitatively, stability rhomboids effectively shrink with temperature, and the side-gate biases of the edge transistors that give a maximal current tend to shift toward the center of the rhomboids. The power consumption decreases because of the shrinkage. The highest operation temperature is determined roughly by $e^2/2C_{\mathrm{G}}k_{\mathrm{B}} \simeq 9\,\mathrm{K}$. Figure 3 shows the current in a three-transistor pump circuit as a function of the normalized phase delay $f\delta t$ [see Fig. 1(c)]. In their experiment, Tsukagoshi *et al.* found $f\delta t = 0.25$ to be optimal.[1] They also observed both positive and negative currents. Figure 3(a), which is in the optimal condition at $T = 0\,\mathrm{K}$, shows strong rectification. However, as the temperature becomes higher, the net current vanishes rather quickly. With zero side-gate biases, current continues to flow at higher temperatures as shown in Fig. 3(b). The higher temperature results are in good agreement with the experimental results of Tsukagoshi *et al.*[1]

If the clock frequency f is too high, the pump cannot fully follow the clock signals. The upper frequency limit f_{max} for $T = 0\,\mathrm{K}$ can be estimated to be $f_{\mathrm{max}} \approx e/(8V_{\mathrm{p}}R_{\mathrm{T}}C_{\mathrm{G}}^2)$, above which the pump operation is expected to degrade. Our numerical result is $f_{\mathrm{max}} \approx 1 \times 10^8\,\mathrm{Hz}$, which is confirmed in Fig. 4(a). At non-zero temperatures, thermal errors affect pumping more at low frequencies,[2] and it is seen as deeper current troughs in Fig. 4(b) at low f. The upper frequency limit does not differ significantly from that for the zero-temperature case.

This work was carried out under the management of FED as a part of the MITI R&D of Industrial Science and Technology Frontier Program (Quantum Functional Device Project) supported by NEDO.

---

[1] K. Tsukagoshi and K. Nakazato, Appl. Phys. Lett. **71**, 3138 (1997).
[2] M. B. A. Jalil, H. Ahmed, and M. Wagner, J. Appl. Phys. **84**, 4617 (1998).
[3] K. Tsukagoshi, B. W. Alphenaar, and K. Nakazato, Appl. Phys. Lett. **73**, 2515 (1998).

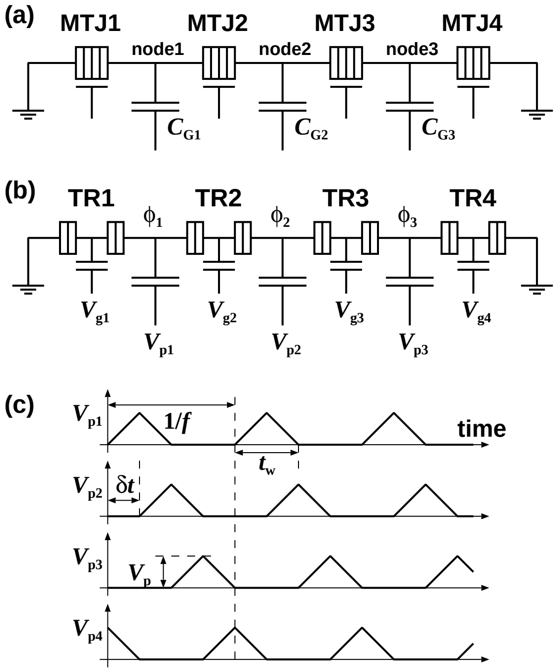

FIG. 1. (a) Pump with four MTJ transistors. Clocking-gate capacitances C_{Gi} are much larger than other capacitances. (b) Simpler model with two-junction transistors. (c) Triangular pulses are used to drive the pump. The parameters used in simulations are $C_1 = C_2 = 2\,\mathrm{aF}$, $C_g = 1\,\mathrm{aF}$, $C_0 = 0.5\,\mathrm{aF}$, $C_G = 100\,\mathrm{aF}$ and $R_T = 200\,\mathrm{k\Omega}$. With these parameters, the change in ϕ_i due to tunneling of a single electron is approximately[2] $\delta\phi \approx e/C_G \simeq 1.6\,\mathrm{mV}$ and sufficiently smaller than the other relevant voltage scale $e/C_\Sigma \simeq 29\,\mathrm{mV}$.

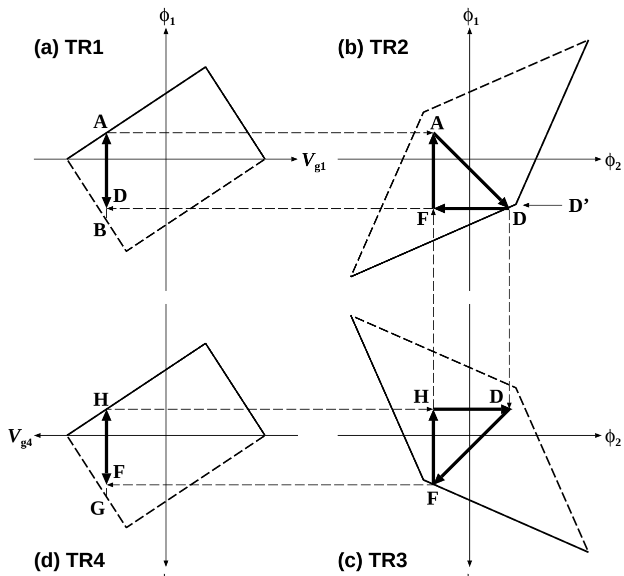

FIG. 2. Steady trajectories for well-chosen V_{g1} and V_{g4} at $T = 0\,\mathrm{K}$. Borders for forward-direction tunneling are drawn with solid lines and those for reverse-direction tunneling are drawn with broken lines. $V_{g2} = V_{g3} = 0\,\mathrm{V}$. The state points draw triangles in the ϕ_i-ϕ_{i+1} planes.

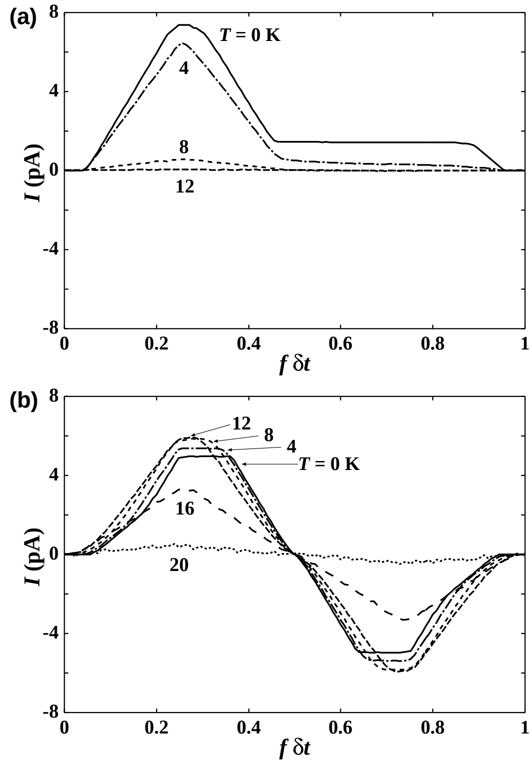

FIG. 3. Net current versus normalized phase delay $f\delta t$ for different temperatures. See also Fig. 1(c). $V_p = 100\,\mathrm{mV}$ and $f = 1\,\mathrm{MHz}$. (a) $V_{g1} = -42\,\mathrm{mV}$, $V_{g2} = 0\,\mathrm{V}$ and $V_{g3} = 42\,\mathrm{mV}$, which gives the triangular condition at $T = 0\,\mathrm{K}$. (b) $V_{g1} = V_{g2} = V_{g3} = 0\,\mathrm{V}$.

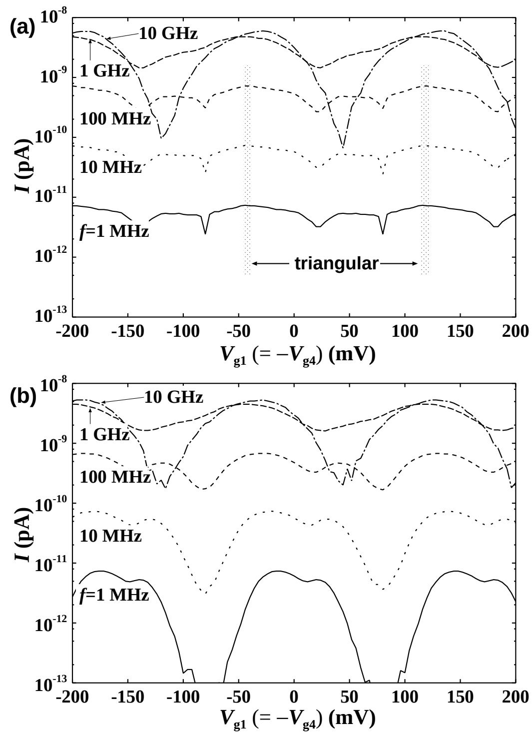

FIG. 4. Frequency dependence of the pump current. (a) $T = 0\,\mathrm{K}$. (b) $T = 12\,\mathrm{K}$.