High-speed single-electron memory: cell design and architecture

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Abstract

A new silicon-based single-electron memory cell is presented for use as a high-speed RAM. Novel architecture and operation schemes are evaluated by conducting Monte Carlo single-electron simulations. By performing transient waveform analysis. a high-speed write operation IS demonstrated with a write time shorter than IO nsec.

L-SEM (Lateral Single Electron Memory) cell

The L-SEM architecture is mtended to achieve high-speed write operations comparable to DRAM operation. In this new memory-cell (see Fig. 1(a)), an m-plane MTJ Multiple Tunnel Junction) [1] is integrated into the gate of a MOSFET (Metal-Oxide-Semiconductor FET), and the write operation IS achieved by the electrons tunnelling through the MTJ between the word electrode and the memory node.

The lateral size of the T-shaped memory node region may be chosen of the order of a few tens of nanometers to meet the current lithography conditions. Therefore. the single-electron memory operation is generalised in the L-SEM cell by employing CB (coulomb Blockade) due to multiple electrons ranging from a few to a few tens rather than purely one. The stored memory node voltage is sensed by monitonng the current through the MOS channel induced under the memory node. The memory-cell array consists of one L-SEM device connected to the source. data and word lines (Fig. I(b)).

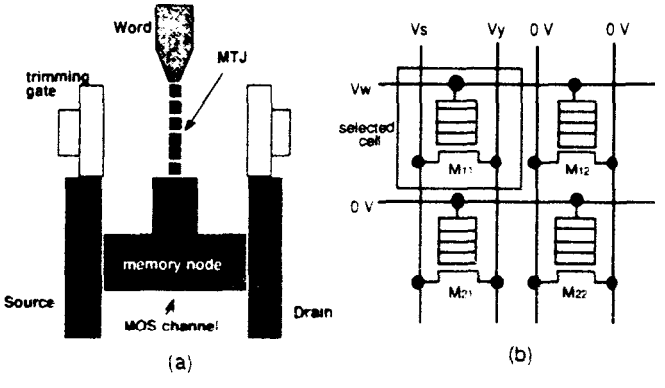

Fig 1 (a) L-SEM structure and (b) memory-cell array

This is a different operation principle from those of other quantum-dot single electron memory cells [2]-[4] where charge injection is done between the MOS channel and the nanometre-scale memory node through the gate oxide. These quantum-dot memory cells are classified as non-volatile memory, and have in general long data retention times. However. the write/erase operations of these memory cells are inherently slow, typically ranging from 10" to 10^{-3} seconds. since the operations rely on the Fowler-Nordheim runnelling currents through a solid oxide barrier under large electric fields.

The L-SEM cell structure with the MTJ has several advantages. Firstly. it enables larger tunnelling currents. resulting in faster charging / discharging operations. Secondly. because of its gain cell nature, the L-SEM overcomes the inherent low-noise-margin issue of the conventional one-transistor/one-capacitor (1-T) DRAM cells. Thirdly, the use of the MTJ suppresses the leakage current due to co-tunnelling. Finally, the cumbersome offset charge effects may be reduced: this issue will be discussed in the last section of this paper.

In this work the cell structure was first designed by using a 2D capacitance simulator. Second the I-V characteristics of the key MTJ were simulated to evaluate the Coulomb gap. and finally full memory sequences were simulated by using a single-electron circuit analysis simulator [5]. Figure 2 shows the cycle timing diagram for the common source Vs and data Vy voltage, Vsy, and word voltage, Vw. for writing the '0' and '1' sequences.

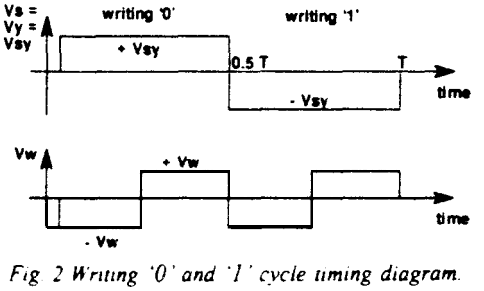

Fig 2 Writing '0' and '1' cycle timing diagram.

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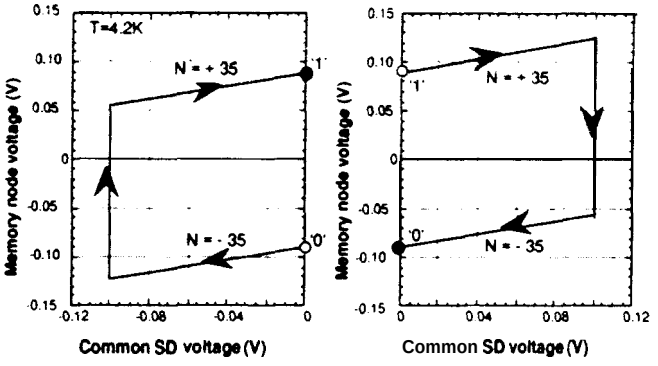

Fig. 3 The hysteresis loop of the memory **node** *voltage as a function of* **common** *source and dara volrage.*

When such a voltage sequence is applied. the L-SEM shows node voltage hysterests as shown in Fig. 3. The simulation was done at 4.2K for an L-SEM with a 5-nm-dot MTJ and for zero trimming gate bias. For writing '0' (right-hand side). a positive bias of 0.1 V is first applied to both the source and data electrodes. A negative voltage pulse of -0. 12 V is then applied to the word to inject electrons mto the memory node? After a positive word voltage pulse of 0.12 V is apphed. the source and data voltages are finally turned off to zero. and the operation point moves to the final state '0'. For writing '1' (left-hand side), a negative bias of -0.1 V is first applied to both the source and data electrodes, and other sequences are the same as those for writing '0'.

The upper and lower branches of the hysteresis correspond to +35e (the absence of 35 electrons) and -35e (the presence of 35 electrons) charge states. respectively. The size of the hysterests may be varied by tuning the tnmming gate bias. The full sequences for writing '0' and '1' selectively to the cell M_{11} are summarised in army circuit diagrams in Figs. *4 and 5. The* memory-cell consists of one L-SEM device connected to the source&data lines and word linc. In Fig. *4* the left column shows the sequences to write '0' selectively to the memory-cell M_{11}. First a positive bias of 0.1 V is applied to both the source and data lines connected to M_{11}. The right column depicts the operation point of the memory indicated in (V_{node}, V_{sy}) space. In this representation the negative voltage pulse of -0. 12 V apphed to the word line shifts the blockade region downwards. Under these circumstances. since the operation point is outside the blockade region, it can not stay here and so moves to Inside.

Third. the positive word voltage pulse of 0.12 V is applied and this operation point remains to stay in the same place. Finally. the source and data voltages are turned off to zero. and the opetatton point moves to the final state '0'.

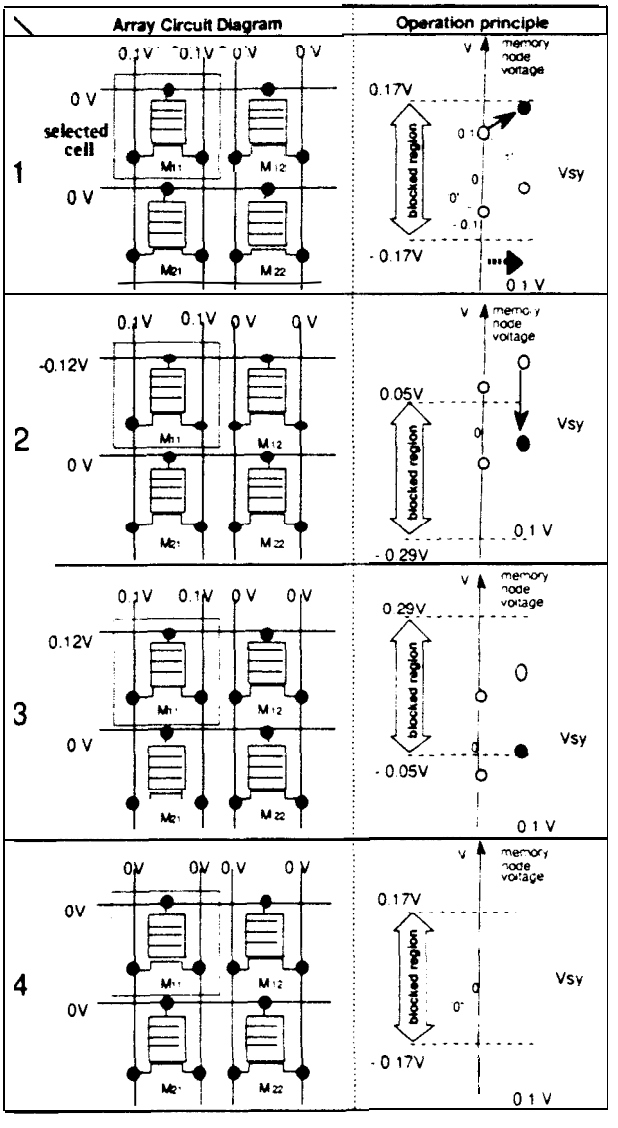

Fig 4 Sequences for writing '0' selectivel\ to r h e memon cell M..All rhe voltage parameters are chosen for the L-SEM with 5 \ 5 nm'-island-MTJ Vsy and Vw are 0.1V and 0.12 I'

High-speed write operation of L-SEM

Transient memory node voltages were next investigated to evaluate the write time of the L-SEM. In Fig. 6. the cycle timing diagrams for Vsy and Vu (Figs. 6(a) and (b)). and the ttmc-dependence of the memory node voltage (solid line) and the corresponding number of electrons stored on the memory node (broken line) are shoun for the same write '0' and '1' sequences (Fig. 6(c)). Vsy and Vw were chosen to be 100 and 180 mV. respectively.

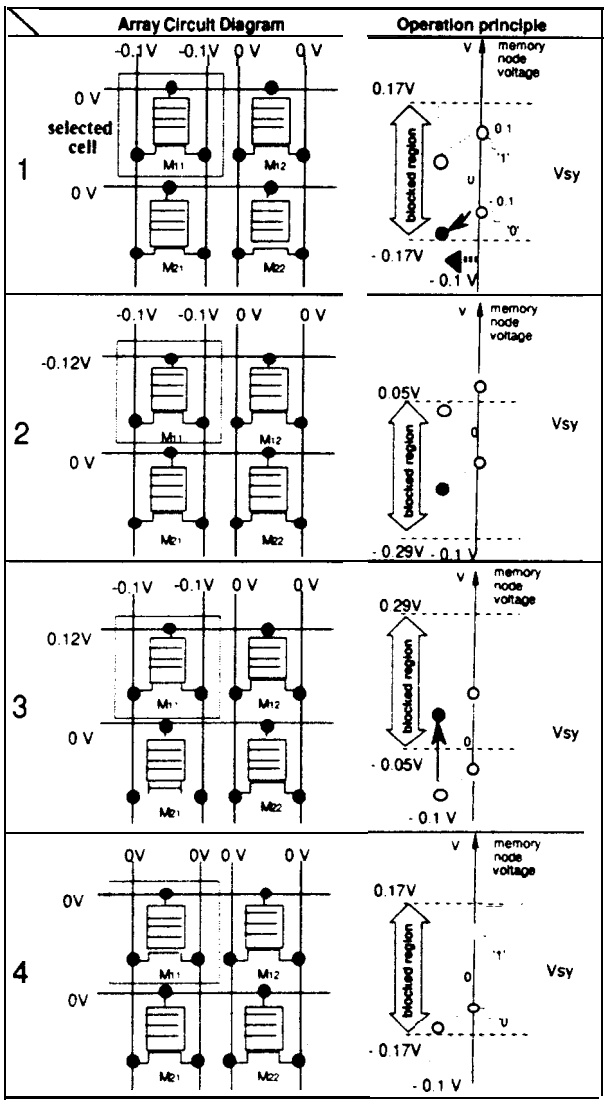

Fig. 5 Sequences/or writing '1' selectively to the memory cell M_{11}

Fast switching is achieved between high and low levels with a switching time as short as 10 nsec. Details of discretised charging/discharging steps can be seen in Fig. 6. We investigated the effects of the word voltage pulse height on these write operations. Figure 7 (a) shows the transient of the memory-node voltage for various values of Vw. It can be seen that the switching becomes faster with increasing Vw since a larger Vw results in a larger tunnelling current through the MTJ. leading to faster charging-up. In Fig. 7(b). the switching time t_{THL} is plotted as a function of Vw. The switching occurs above a certain threshold voltage and then t_{THL} decreases rapidly. This is because a larger tunnelling current flows with increasing Vw over the critical voltage. and t_{THL} approaches the limit determined by $C_{\Sigma}R$.. it can be seen that t_{THL} can be reduced to less than 10 nsec for the present 5-nm-islands L-SEM cell structure

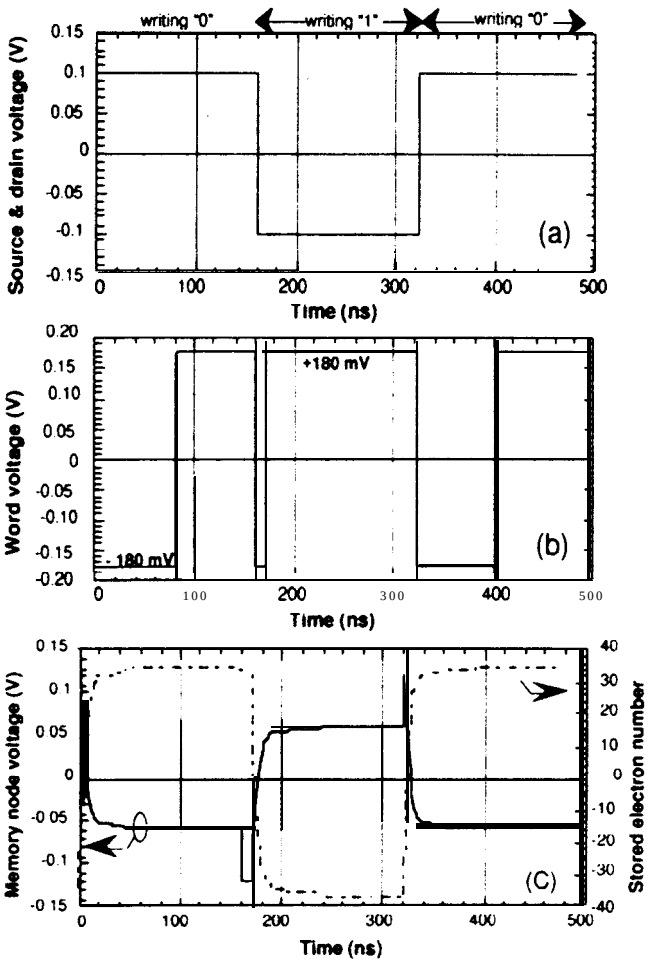

Fig. 6 Cycle timing diagrams((a) and (b)) and corresponding transient memory node voltage and electron number srored on the memory node ((c)) for write sequences

L-SEM with 2D network tunnel junction

An alternative L-SEM cell structure with a 2D network tunnel junction (NTJ) (see Fig.8(a)) was also examined to achieve a further improvement of the write operation. Larger tunnel currents are expected for the NTJ structure simply because the channel width is effectively increased. Such NTJ structures may be realised in metal-dot tunnel junction devices. An equivalent circuit is shown in Fig. 8(b) for a 6 x 7 tunnel junction army. The I-V characteristics and t_{THL}-Vw dependence simulated for the L- SEM with 2x2-nm^2-island NTJ are show in Figs. 9(a) and (b), and compared with the results for 2x2-nm^2-island MTJ shown in Fig. 9(b).

The runnelling current becomes a few times larger by employing an NTJ simply because of the reduced tunnel resistance. This results in a shoner switching time (Fig. 9(b)). A switching time as short as 2 nsec is achieved which is comparable to that of the latest DRAM. In conclusion the new L-SEM architecture enables high-speed write operation and, by optimising the tunnel junction configuration. it is possible to achieve a write time shorter than 10 nsec.

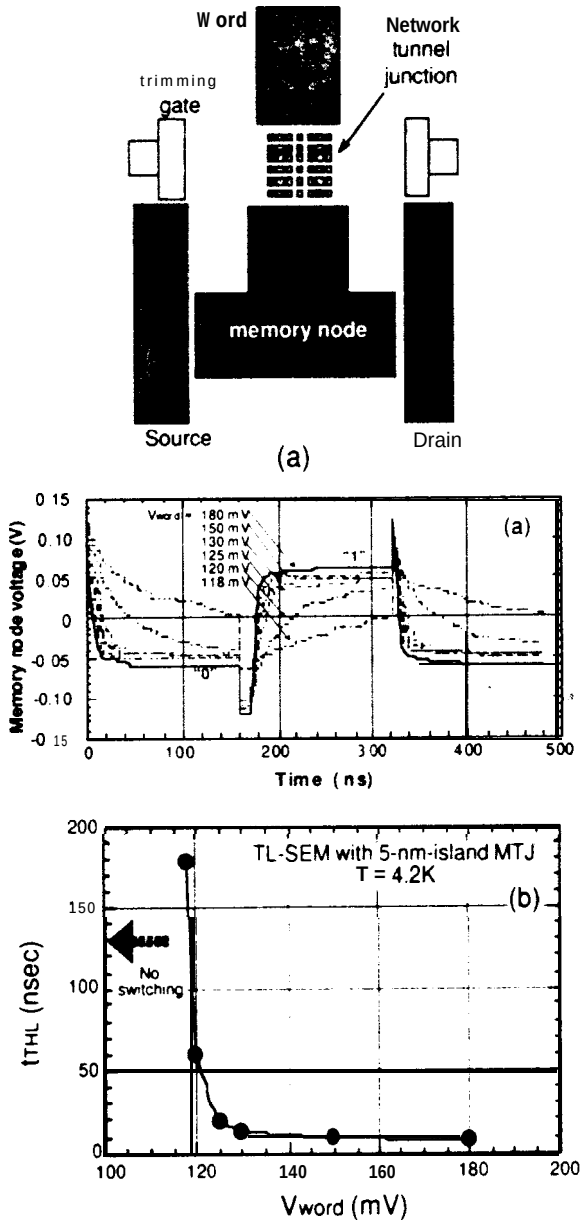

Fig 7 **(a)** *Transient memory* **node** *voltage simulated with various values of Vw for rhe L-SEM with 5x5-nm -island MTJ at 4.2K (b) Vwdependence of* t_{THL}

Discussion on Offset charge effects

In this **final** section, we discuss the offset charge effects in the L-SEM cell. We have so far **considered** an ideal memory system without any **fractional** background charge. However. charged defect states at **silicon/oxide** interfaces are more or less inevitable in the real device structures, which may cause senous effects on the memory operations. From the stand-point of memory design, the most crucial effect of the offset charge is uncontrollable change in the critical voltage. If the offset charge on each island varies in a random manner, the critical voltages of the **MTJs** in the memory army are also scattered completely, and there will 'be a finite probability that the CB of the MTJ is broken and the stored data cannot be **retained** in some memory cells. In these circumstances. a *new* circuit operation which is independent of background charge is necessary [6].

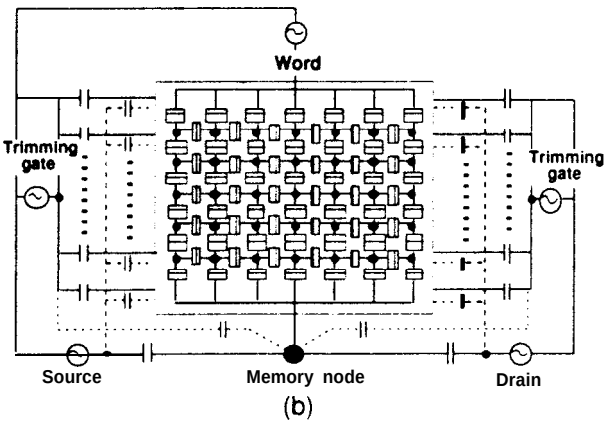

Fig 8 (a) L-SEM with .?D network tunnel junction (b) 4 quantum equivalent circuit for the L-SEM with NTJ

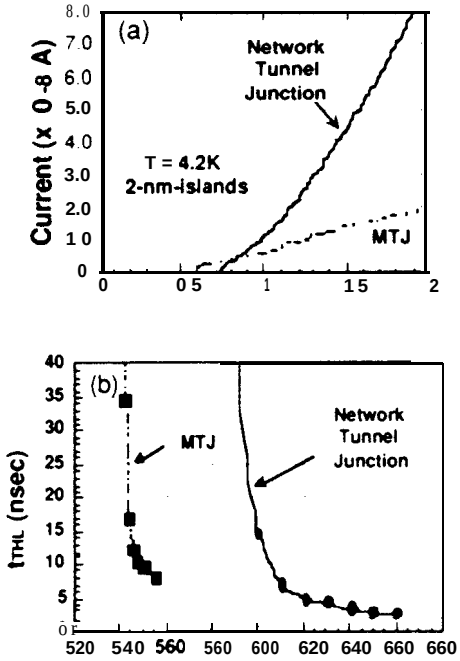

Fig 9 (a) I-V characteristics and (b) t_{THL}*-Vw curve simulated for the L-SEM The NTJ is compared with the MTJ at 4 2K*

However. a **density** of interface defects **achieved** in recent silicon process **technologies** is typically of the order of 10^{-10} cm^{-2}. **which** results in. at most. only a few defects over the core MTJ area of **the** single L-SEM-cell. As long as the offset charge is **induced** by those few defects. the offset charges on the islands of the **MTJ** are not random but there should be a certain correlation among them. To make clear it. we have conducted a **preliminary** simulation for the L-SEM system with a single defect charge

introduced. The defect is assumed to be located in 2 nm distance from the chain of the islands. and is moved parallel to the chain (see Fig. 10).

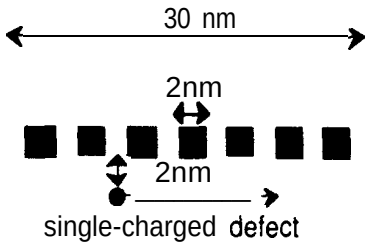

Fig.10 MTJ with a single charged *defect configuration*

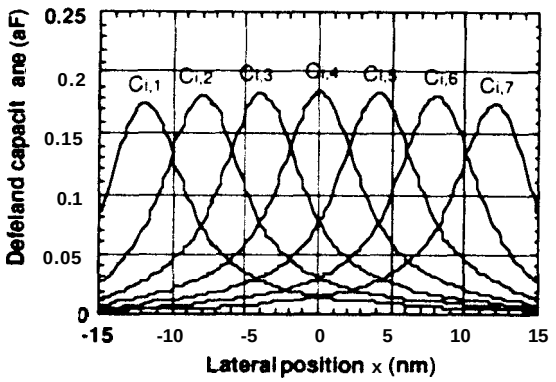

Fig. I I The charge on each island induced by a single defect charge plotted as a function of the defect position The *induced* charge is *plotted as an effective capacitance between the defect and islands.*

.Figure 11 shows the defect position dependence of the charges induced on each island. The capacitance parameters between the defect and islands were obtained from these results. In the single-electron circuit simulations, the single defect is modelled as an extra node with a single negative charge, -e, on it. The position-dependent capacitance parameters were then introduced to the equivalent circuit as addihonal capacitances. Simulations for the I-V characteristics were repeated by moving a single defect charge from the one edge to the another of the MTJ. The critical voltages taken from the I-V characteristics were plotted in Fig. 12 as a function of defect position.

Statistical analysis was performed on these results: the distribution of the upper critical voltages was plotted in Fig. 13. The entire distribution looks like a Poisson distribution with a main peak which is slightly below the original critical voltage of 0.2 V. It should be noted that distribution has a tail towards the larger voltage regime. but no fmite probability is seen around zero critical voltage. This means that blockade state is always maintained independent of defect positions. This is because many of the tunnel junctions in the MTJ can act to provide a good blockade even though some of the tunnel junctions close to the defect are broken.

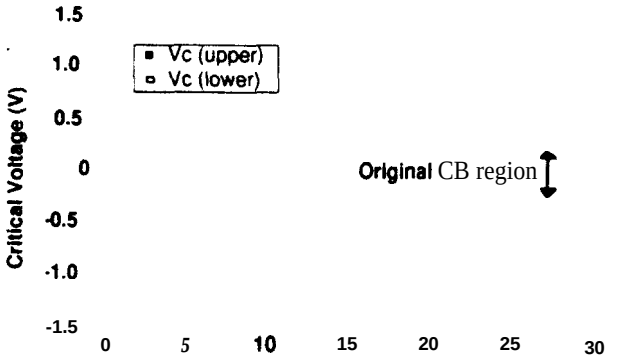

Fig.12 Upper and lower critical voltages calculated by moving a single charged defect in parallel to rhe MTJ.

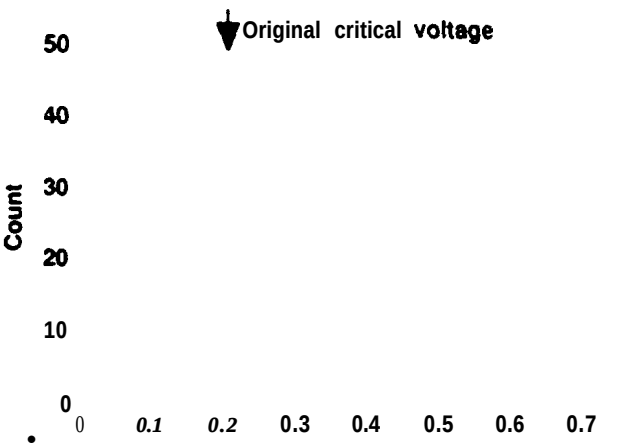

Fig. 13 Distribution of the upper critical voltages induced by a single defect charge.

In addition, a well defined main peak in the distribution still enables us to work in the same manner as that for an ideal system. This is indeed a big advantage of the MTJ compared with a single tunnel junction in which the blockade is determined only by one tunnel junction. Therefore. as long as the number of the charged defects in one cell is kept smaller than the number of the tunnel junction in the MTJ. the L-SEM structure is robust for offset charge problems. These considerations are depicted in Fig. 14. In this figure a solid line represents defect densities which provide one defect per one island area of the MTJ. This indicates that the MTJ with island size as small as a few manometre satisfies this criterion, and the L-SEM with such MTJs can operate without having special circuit arrangements.

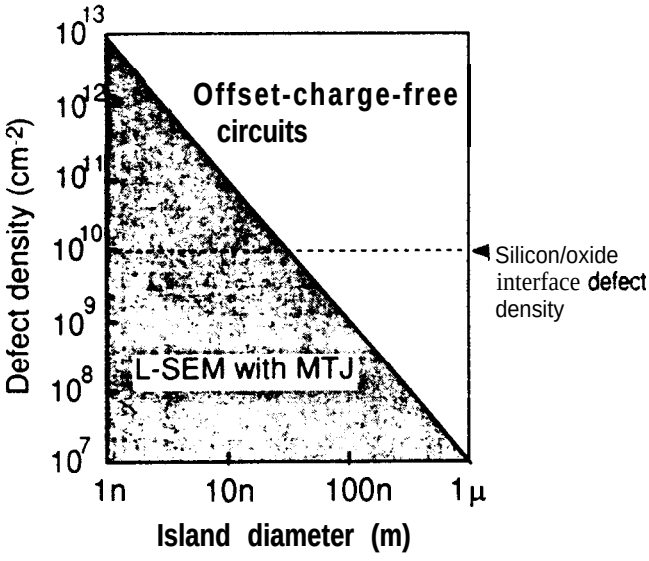

Fig. 14 The shaded region represents rhe condition in which the L-SEM with the MTJ works despite the charged dejects. Above rhe boundary a different offset-charge-free circuit scheme is required.

Conclusion

New L-SEM cell design and architecture based on the MTJ were presented for use as a high-speed RAM. A unique few electron operation scheme was shown by conducting single-electron circuit simulations, and a high-speed write operation was demonstrated with a charging/discharging time shorter than 10 nsec. The robusmess of the L-SEM was also discussed in terms of the offset charge issue.

Acknowledgement

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