Nanocrystalline Silicon Point-Contact Single-Electron Transistor

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In recent years, there has been considerable interest in single-electron transistors (SETs) fabricated in thin, continuous, polysilicon films which may be incorporated easily into conventional CMOS processes [1]. In these devices, the charging islands are formed by the crystalline grains and the tunnel barriers are formed by the grain-boundaries and associated depletion regions. In standard polysilicon films, the grain size and capacitance is not small enough to observe single-electron effects at greater than cryogenic temperatures. Nanocrystalline silicon (nc-Si) is a chemically tailored material where crystalline grains <10 nm in size are embedded in an amorphous silicon matrix. The very small size of the grains raises the possibility of single-electron effects even at room-temperature. Single-electron charging effects up to 60 K have been demonstrated in as–deposited nc-Si point-contact SETs [2]. Here, we report room-temperature single-electron effects in nc-Si SETs, where low-temperature oxidation has been used to modify the inter-grain tunnel barriers.

The nc-Si material was prepared using a low-temperature (equal to or less than 300°C) PECVD process from a SiF_4: H_2: SiH_4 gas mixture. A continuous, ~30 nm thick film was deposited from the plasma on a 150nm thick SiO_2 layer thermally grown on an *n*-type silicon substrate. The films were doped *n*-type *in situ* using PH_3 and the room-temperature carrier concentration was $10^{20}/cm^3$. Raman spectroscopy performed on the film indicated a grain-size of ~4 nm – 8 nm and a crystalline volume fraction of 70%. The point-contact SETs were defined in the nc-Si film using electron-beam lithography and reactive-ion etching in a $SiCl_4/CF_4$ plasma. The SETs were then oxidised at 750°C for 1 hour, followed by annealling in argon at 1000°C for 15 minutes. In this process, the grain-boundaries were likely to be oxidised more than the crystalline grains. Fig. 1 shows an SEM image of a SET with a ~50 nm x 30 nm cross-section point-contact defined between source and drain regions. Two lateral side-gates are used to control conduction through the point-contact.

Figure 2 shows the drain-source current-voltage (I_{DS}/V_{DS}) characteristics at 23 K in a SET with a 30 nm x 30 nm point-contact. A high-resistance Coulomb blockade region is seen around zero V_{DS}. This region is 100 mV wide at V_{GS}= 1 V and is modulated periodically by the gate voltage. Figure 3 shows the I_{DS}/V_{GS} characteristics at V_{DS} = 20 mV as a function of temperature. Periodic single-electron oscillations in I_{DS} can be observed even at 300°K. Fig. 4 shows the corresponding I_{DS}/V_{DS} characteristics, which remain non-linear up to 275°K. These effects may be attributed to single-electron charging in the point-contact, associated with an island formed by a nc-Si grain isolated by grain-boundary tunnel barriers of amorphous silicon/ SiO_x.

[1]A. C. Irvine, Z. A. K. Durrani, H. Ahmed, and S. Biesemans, Appl. Phys. Lett. **73**, 1113 (1998).

[2]Y. T. Tan, T. Kamiya, Z. A. K. Durrani, H. Ahmed, To be published in Appl. Phys. Lett. **78**, (19 Feb. 2001).

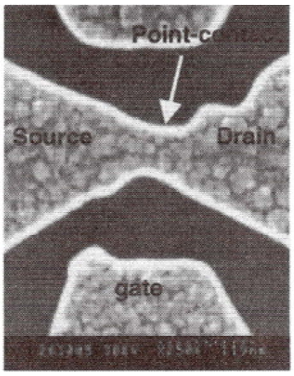

Fig. 1. Nanocrystalline silicon point-contact SET.

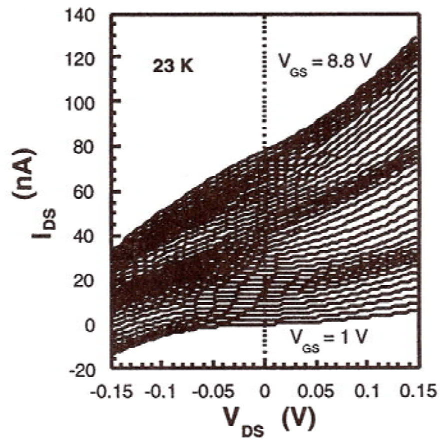

Fig. 2. I_{DS}/V_{DS} characteristics of a nc-Si SET at 23 K. V_{GS} increases from 1 V to 8.8 V in 0.2 V steps. The curves are offset in current by 2 nA for each step in gate voltage.

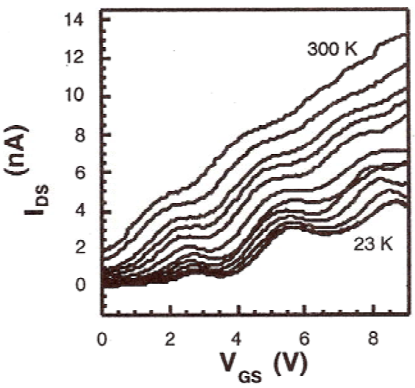

Fig. 3. I_{DS}/V_{GS} characteristics of a nc-Si SET at V_{DS}= 20 mV. The lowest temperature curve is measured at 23 K. The temperature for the remaining curves is increased from 50 K to 300 K in 25 K steps.

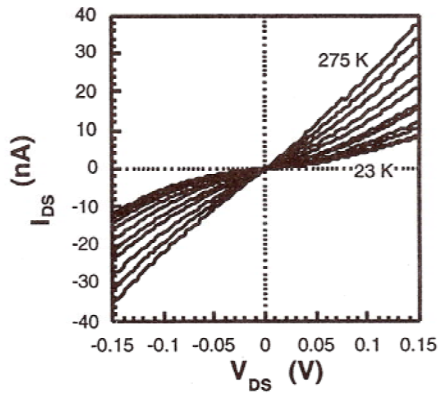

Fig. 4. I_{DS}/V_{DS} characteristics in a nc-Si SET at V_{GS}= 2 V. The lowest temperature curve is measured at 23 K. The temperature for the remaining curves is increased from 50 K to 275 K in 25 K steps.