

Carrier transport across a few grain boundaries in polycrystalline silicon

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Polycrystalline silicon (poly-Si) films have been a key material for the state-of-the-art thin film technologies. Poly-Si thin film devices is projecting to be nanometer scale. Carrier transport properties in poly-Si films have been intensively studied so far. It is more interesting to understand that local inhomogeneity of GBs significantly affect performance of the nanometer scale devices. In this study, we focused on electron transport across a few grain boundaries using nanometer scale devices.

50 nm-thick highly phosphorus-doped poly-Si film was fabricated by solid-phase-crystallization of amorphous silicon at 850°C for 30 min on a-SiO_x grown single-crystal silicon. Then, Side-gated point-contact devices were fabricated by e-beam lithography. SEM and TEM observation indicated that the average grain size was ~20nm. Thus the channel dimension (width/length) was varied from 30 to 50 nm to characterize electron transport across GBs in the channel. Source-drain current-voltage (I_{ds} - V_{ds}) characteristics was measured between 19K and 300K and the GB potential barrier height (V_B) was evaluated from the temperature dependence of resistivity. We observed linear I_{ds} - V_{ds} characteristics in ~66% of the devices, in contrast, other devices exhibited non-linear I_{ds} - V_{ds} characteristics at low temperature. The latter was attributed to the existence of GBs in the channel, which was consistent with the simulation results. The V_B value was distributed between 10 and 77 meV. It was also confirmed that the V_B value decreased with the channel width and increased with the channel length, suggesting that transport mechanism involves percolation conduction through the distribution of the V_B along GB.

