Yield Model Characterization for Analogue Integrated Circuit Using Pareto-Optimal Surface

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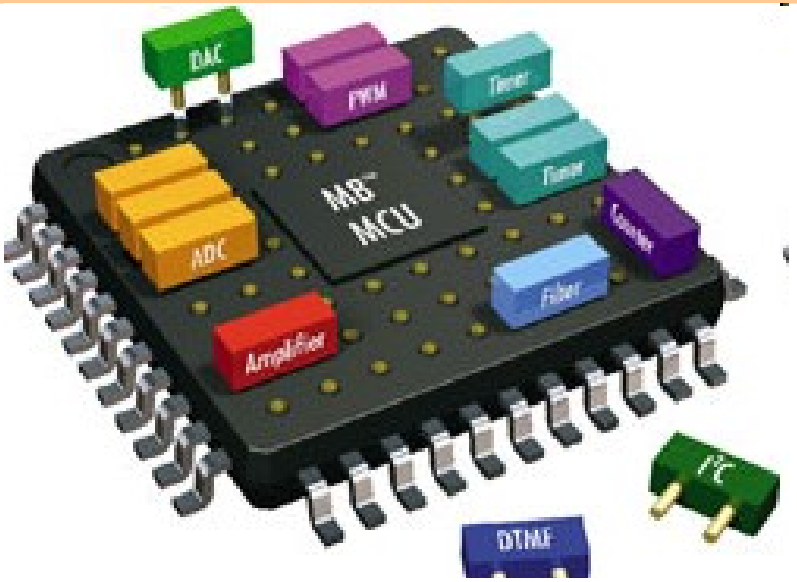
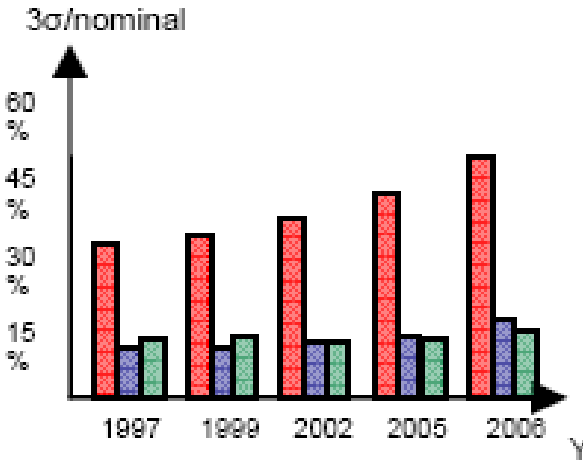
Outline

- **Introduction to Analogue IC Design and its challenges**
- **Background**
  - Development in Analogue CAD
  - Multi Objective Optimization (MOO)
  - Weight Based GA
- **Design Algorithm**
- **Design Experiment & Result**
  - OTA design
- **Current & Future Work**
- **Summary**

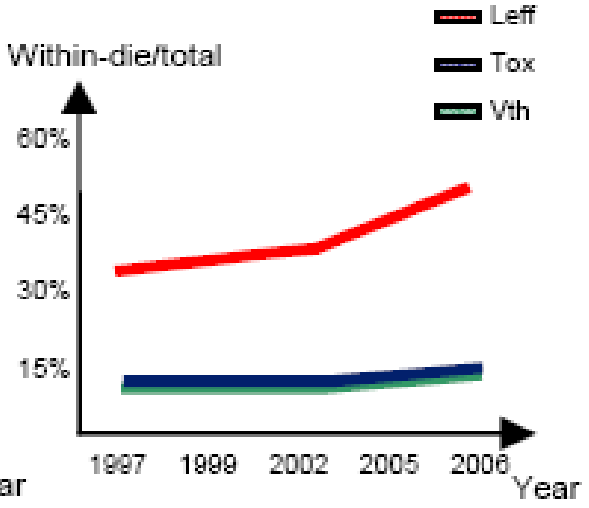
Introduction

- **Transistor Trend**
  - Reduction of transistor size
    - 500nm → 45nm
  - Emphasis on mixed signal
  - Force to use digital process for analog blocks.
- **Variation**
  - On-chip variations getting worse [1]
  - Great challenge to analog world





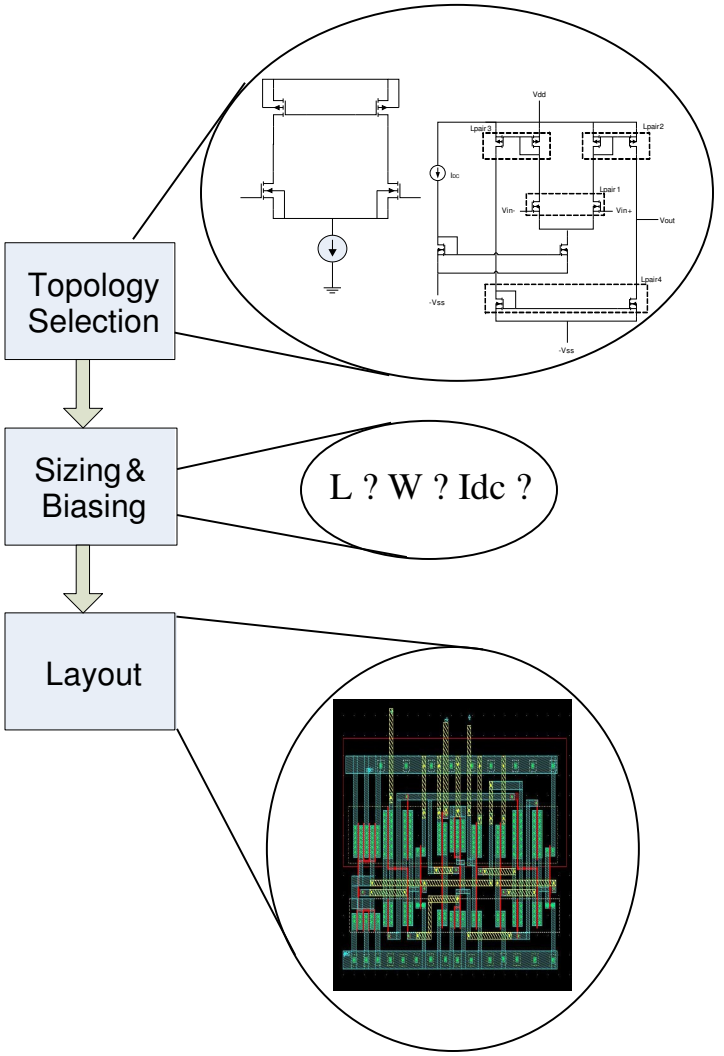
3σ parameter total variation relative to nominal value

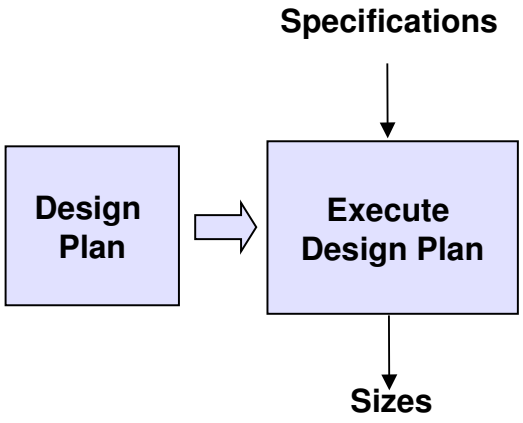


Percentage of total variation accounted for by within-die variations

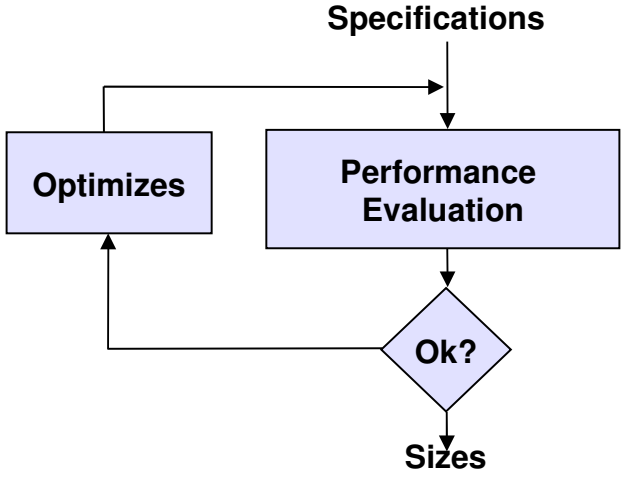
Background

- **Analogue IC Design**
  - Topology Selection
  - Device Sizing
  - Layout
- **Device Sizing Evolution**
  - Hand-calculation → automatic sizing (CAD)
- **Development in Automatic Sizing**
  - Cadence NeoCircuit





Knowledge-Based Design



Optimization - Based Design

Background

- **Multi Objective Optimisation**
  - Optimisation formulation for more than one objective

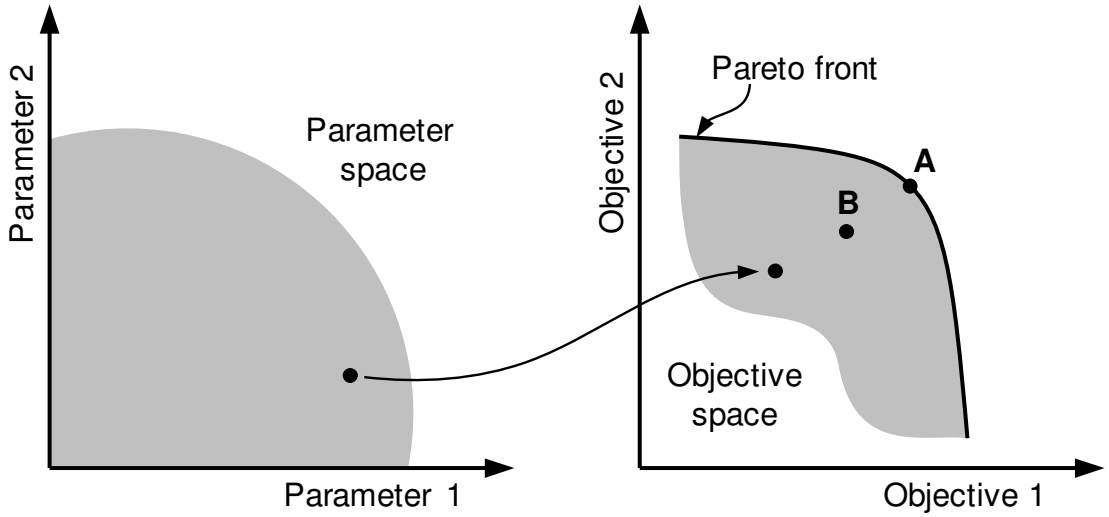
$$Minimise / Maximise\ f_m(x),\ m = 1,2...M$$

$$Subject\ to\ g_j(x) \geq 0,\ j = 1,2...J$$

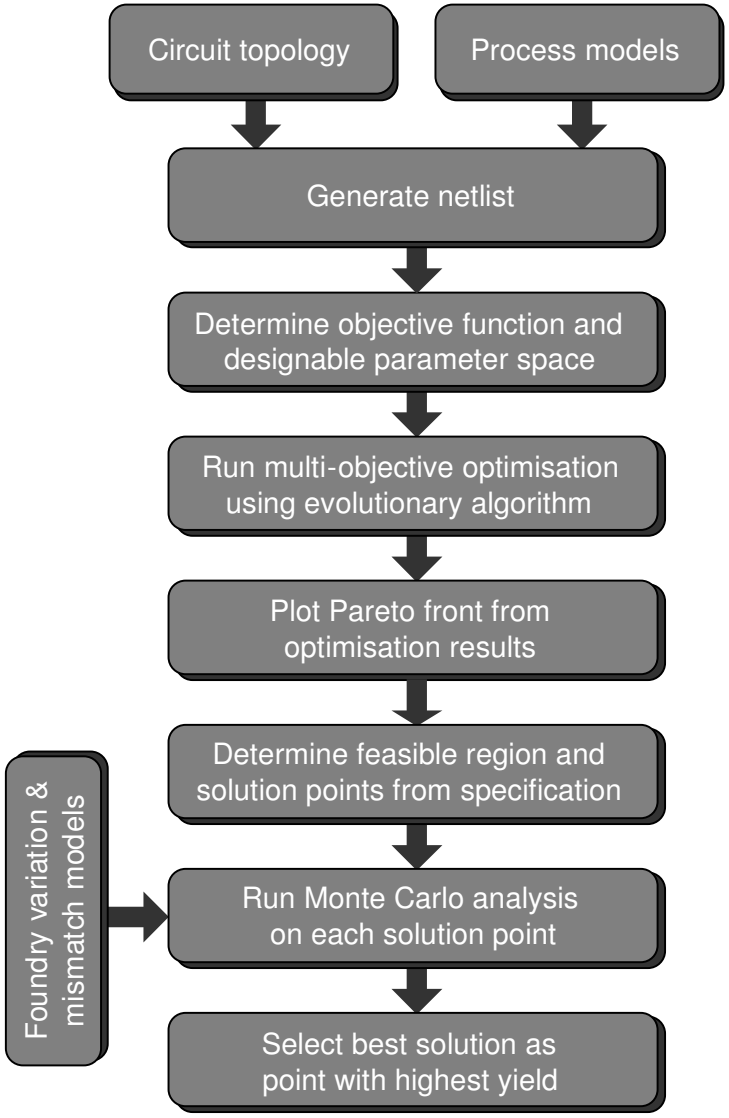
  - The outcome : set of optimal solutions ⇨ PARETO FRONT [2]
- **Weight Based GA**
  - Conversion of multi objective into scalar optimization using weighted summation

$$\sum W_m f_m(x),\ m = 1,2...M$$

  - Weight vectors determined by GA



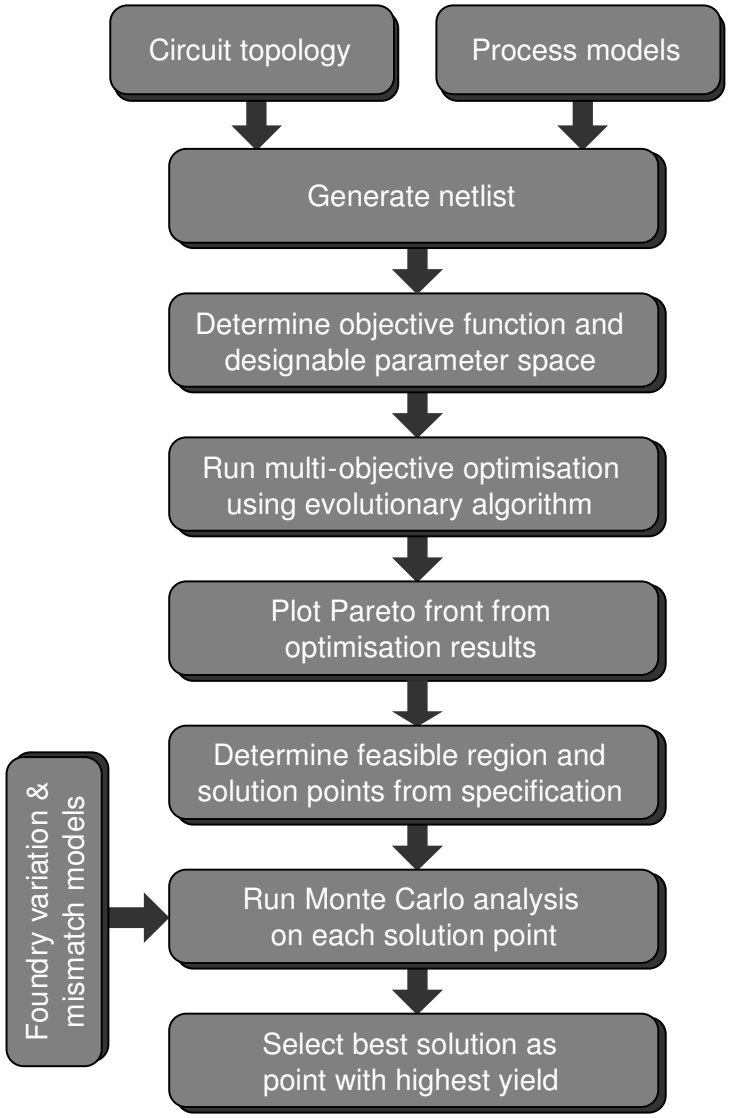
Design Algorithm

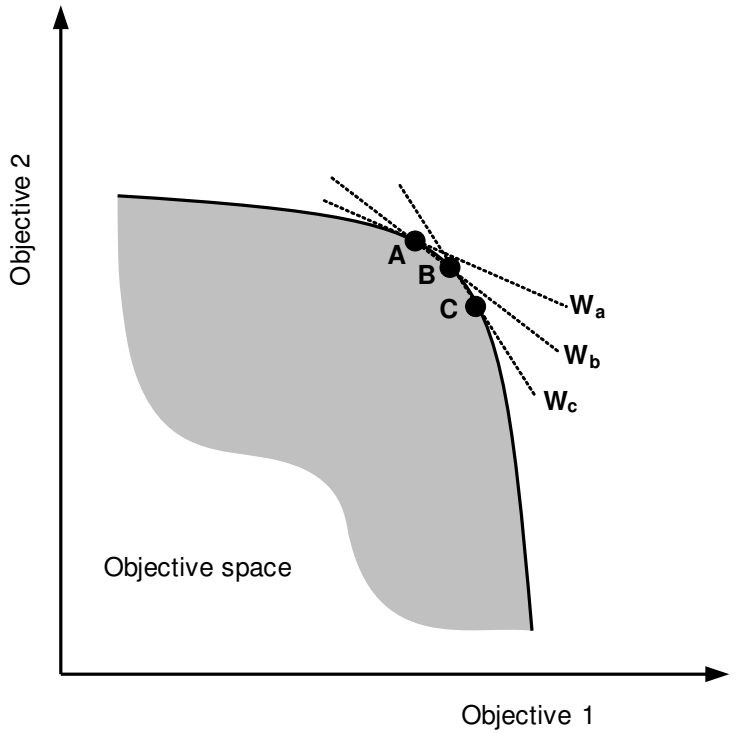



```
.subckt milota_g1 inm inp out vdd vss
c1 net39 out  0.5e-12
i0 net6 vss  dc=Idc
m8 net6 net6 vdd vdd modp w=weff3 l=leff3
m6 net27 net6 vdd vdd modp w=weff3 l=leff3
m5 out net6 vdd vdd modp w=weff5 l=leff5
m0 net39 net35 vss vss modn w=weff2 l=leff2

.LIB '~\amsc35.lib' NOM

.ac dec 10 1k 1000E+06
.measure ac gain find vdb(Out, In) at=1k
.measure ac fc when vdb(Out, In)=`gain-3.0'
.measure ac gainpeak max vdb(Out, In)
.measure ac pbripp PARAM=`gainpeak-gain'
```

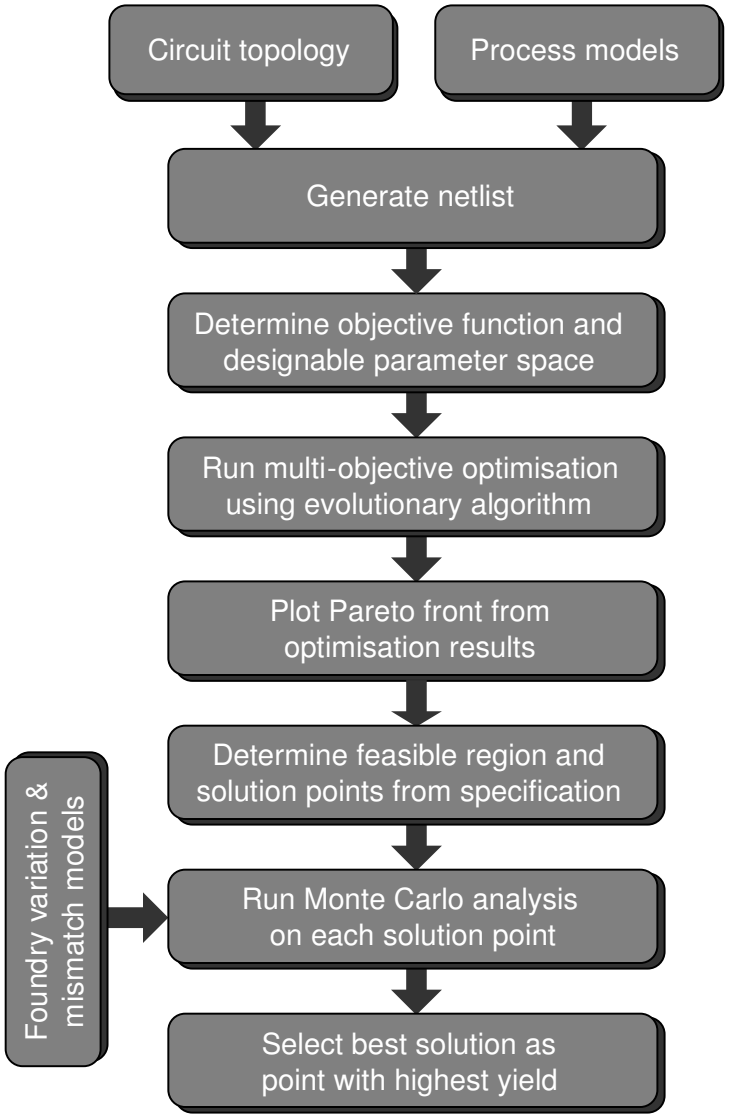
P_1	P_2	P_3	P_4	W_1	W_2

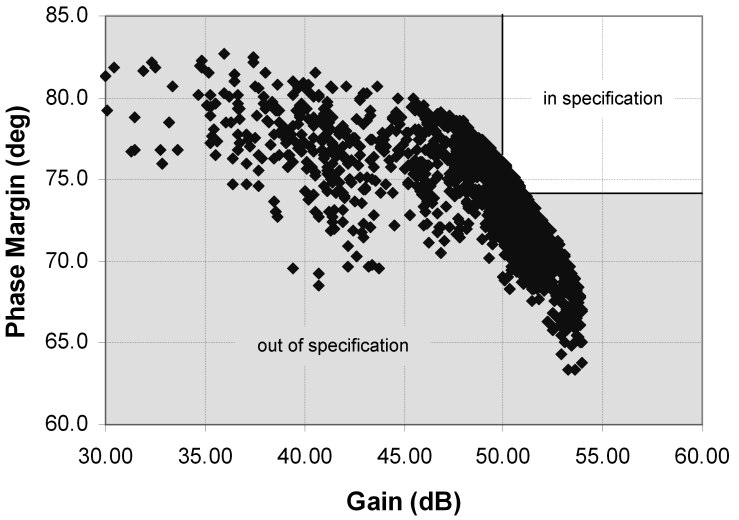
Design Algorithm

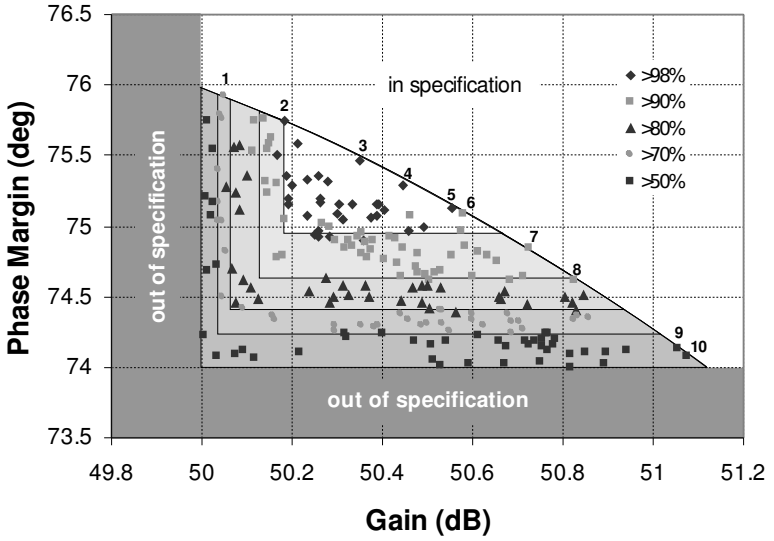




Design Algorithm

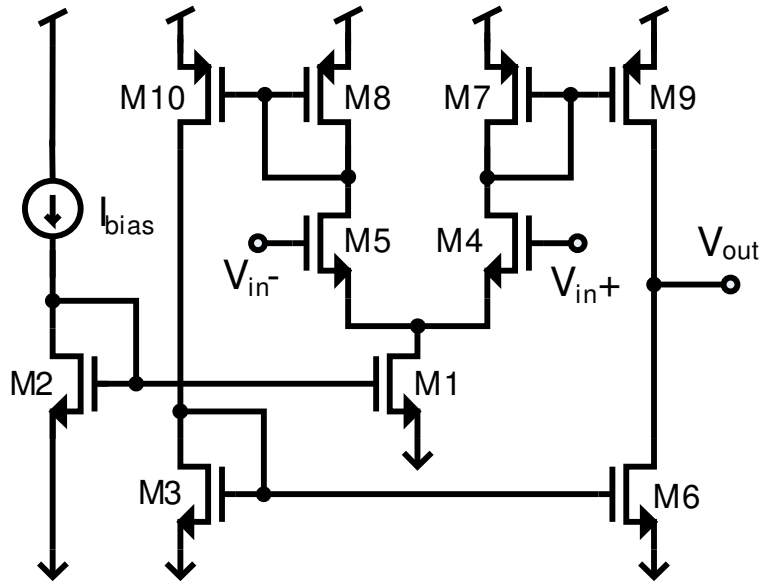






Design Example & Result

- **Symmetrical OTA**
  - 8 designable parameters
  - 2 performance function: gain & pm



Design Parameter:	Range:
W_1 (M5,M4)	10um - 60um
L_1 (M5,M4)	0.35mm - 4mm
W_2 (M7,M9)	10um - 60um
L_2 (M7,M9)	0.35mm - 4mm
W_3 (M10,M8)	10um - 60um
L_3 (M10,M8)	0.35mm - 4mm
W_4 (M3,M6)	10um - 60um
L_4 (M3,M6)	0.35mm - 4mm
W_{g1} (Gain weight)	0 – 1 (normalised)
W_{g2} (Phase weight)	0 – 1 (normalised)

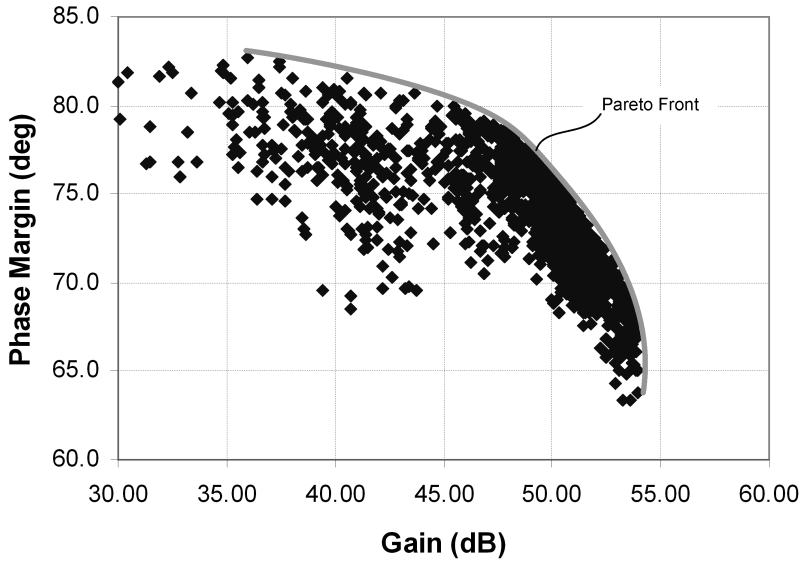
- **GA String**

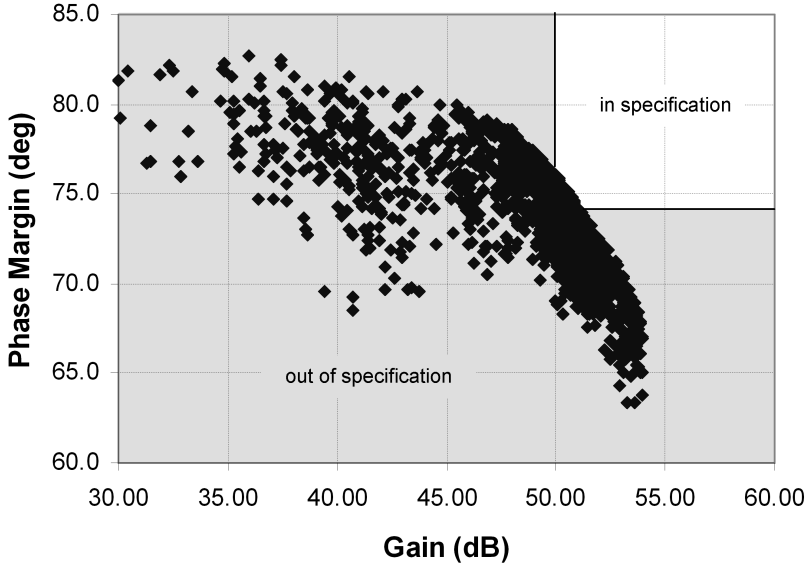
W_1	L_1	W_2	L_2	W_3	L_3	W_4	L_4	W_{g1}	W_{g2}

Design Example & Result

- Design Specifications & Pareto Plot

Objective function:	Specification:
Open loop gain	>50dB
Phase margin	>74deg

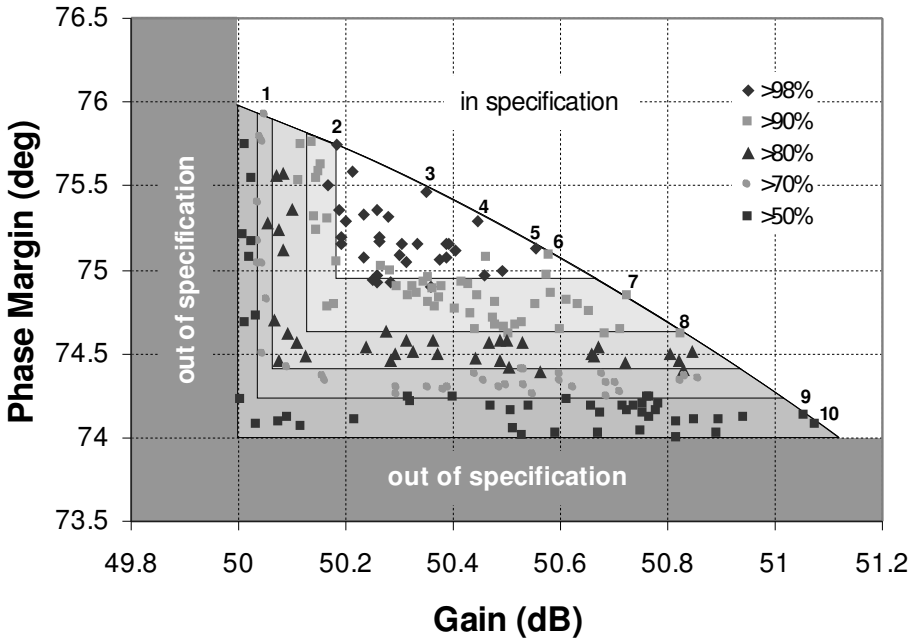




Design Example & Result

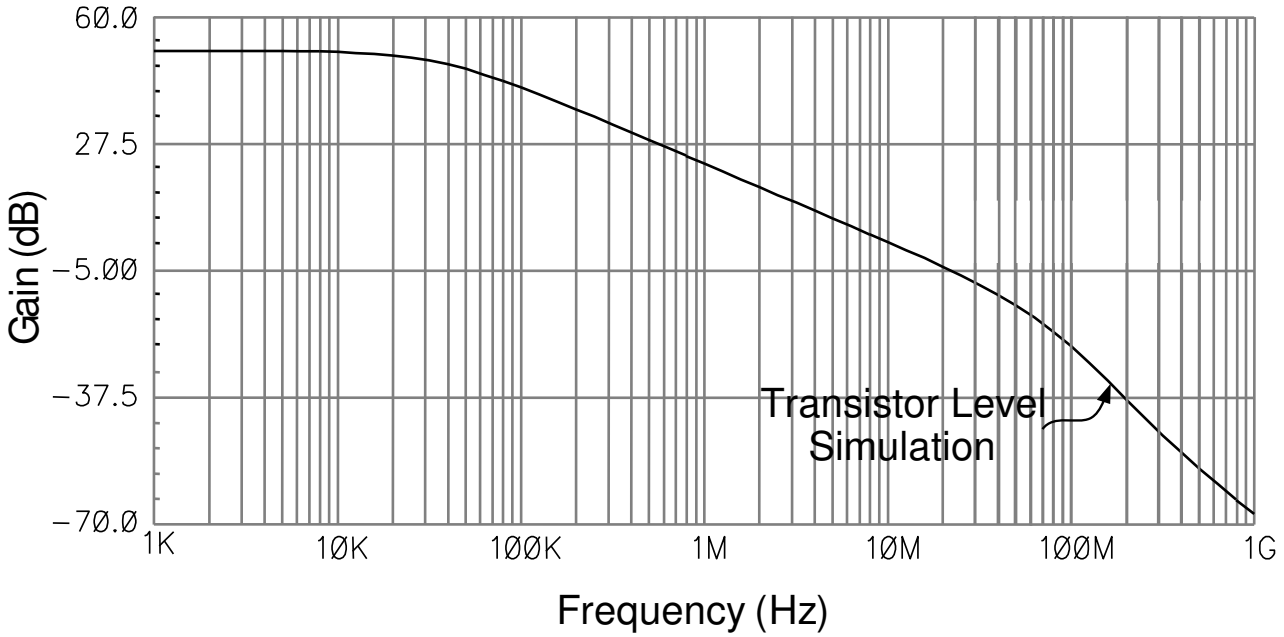
Design Point:	Gain (dB):	Phase Margin (deg):	Yield (%):
1	50.17	75.8	98
2	50.35	75.5	100
3	50.46	75.3	99
4	50.54	75.2	98
5	50.57	75.1	97
6	50.72	74.9	94
7	50.81	74.6	91
8	50.86	74.5	88
9	51.04	74.2	58
10	51.06	74.1	55

Design Point Yield Percentage



Yield Contour

Design Example & Result



Verification

Design Summary

Parameters:	Values:
No. Generations	100
Evaluation Samples	10,000
Pareto Points	1022
Region of Interest Points	10
CPU Time	48 minutes

Future Work

- **On Chip Verification**
  - A silicon design of OTA has been submitted that uses the presented methodology
  - To compare and verify on chip measurement with simulation data
- **Pareto-Modelling**
  - Performance Model
  - Variation Model
- **System Level Application**
  - System Level Design utilizing performance & variations model
    - High Order Video Filter

Summary

- Big challenge for analogue circuit in DSM
- Process variations getting worse
- A new algorithm that characterize the circuit performance and yield using Pareto-front
- Create opportunity to model the performance and variation based on Pareto-front
- The example shown demonstrate the algorithm and the behaviour has been verified with transistor level simulations.

References

[1] M.Buhler et. al. “Date 2006 Special Session : DFM/DFY Design for Manufacturability and Yield-influence of process variations in digital, analog and mixed-signal circuit design.” In Proc. Of the Design Automation and Test in Europe Conference and Exhibition, 2006.

[2] K.Deb, Multi-Objective Optimisation Using Evolutionary Algorithms, John Wiley & Sons Ltd, 2001.

[3] B.D.Smedt, G.Gielen, “Holmes: Capturing the yield-optimized design space boundaries of analogue and RF Integrated Circuits.” In. Proc. Of the Design Automation and Test in Europe Conference and Exhibition, 2003.

Thank You

Any Questions?

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