Yield Model Characterization For Analog Integrated Circuit Using Pareto-Optimal Surface

Sawal Ali, Reuben Wilcock, Peter Wilson, Andrew Brown
Electronics System Design Group, School of Electronics and Computer Science
University of Southampton, UK
{shma05r, rw3, prw, adb}@ecs.soton.ac.uk

***Abstract*— A novel technique is proposed in this paper that achieves a yield optimized design from a set of optimal performance points on the Pareto front. Trade-offs among performance functions are explored through multi-objective optimization and Monte Carlo simulation is used to find the design point producing the best overall yield. One advantage of the approach presented is a reduction in the computational cost normally associated with Monte Carlo simulation. The technique offers a yield optimized robust circuit design solution with transistor level accuracy. An example using an OTA is presented to demonstrate the effectiveness of the work.**

I. INTRODUCTION

Advances in CMOS technology over the last decade have led to increased integration of analog and digital functional blocks onto a single chip. In such mixed signal environments, the analog circuits must use the same basic transistors as their digital neighbours. The design of these analog blocks requires circuit parameters to be sized such that the design specifications are met. The increasing complexity of device models has led to a wider acceptance of simulation and optimization based design techniques and tools rather than hand calculations [1~6]. With reducing transistor sizes, the impact of process variations on analog design becomes significant and can lead to circuit performance degradation and yield falling below specification. This issue has led to the consideration of yield in the design process, generally known as design for yield (DFY) [7]. Most DFY approaches optimize through analytical and approximation methods rather than simulation due to the high computational costs involved.

In this paper, a new yield optimization technique is proposed that does employ simulation but avoids excessive computational cost. The approach uses a simulation based multi-objective optimization using a genetic algorithm to capture the optimal design points for a particular design. Monte Carlo simulation is then used for yield estimation, but only on a region of interest defined by the design specifications. Focusing on a small region means simulation time can be reduced whilst maintaining a high level of accuracy.

The paper is organized as follows. Section II provides a brief summary of multi-objective optimization. The proposed algorithm is given in detail in section III with example results in Section IV. Concluding remarks are given in section V.

II. MULTI-OBJECTIVE OPTIMIZATION

Circuit performance is a function of designable parameters. The design goal is to find a parameter set solution that meets all the performance functions and any imposed constraints. The optimization formulation for more than one objective function is called multi-objective optimization which can be generally stated as given in (1).

$$\begin{gathered} Minimize\,/\,Maximize\ f_m(x),\ m = 1,2...M \\ Subject\ to\ g_j(x),\ j = 1,2...J \end{gathered} \tag{1}$$

Where $f_m(x)$ is the set of M performance functions and $g_j(x)$ is the set of J constraints. In a design that involves multiple conflicting objectives there is not usually a single optimum solution which simultaneously optimizes all objectives. The outcome from multi-objective optimization is therefore a set of optimal solutions [8]. Multi-objective optimization corresponds to an objective space with number of dimensions equal to the number of objectives. Figure 1 shows the relationship between the parameter space and objective space. Each point in the parameter space is a solution that corresponds to a point in the objective space. The black curve on the objective space is called the Pareto front and all solution points lying on this curve are called Pareto-optimal solutions. Point B in the solution space is an example of a non-Pareto optimal point since a more optimal solution exists, point (A). The method used in this work to combine all performance measures into a single objective is a weighted summation, where W_m are the weightings for the performance functions as shown in (2).

$$\sum W_m f_m(x),\ m = 1,2...M \tag{2}$$

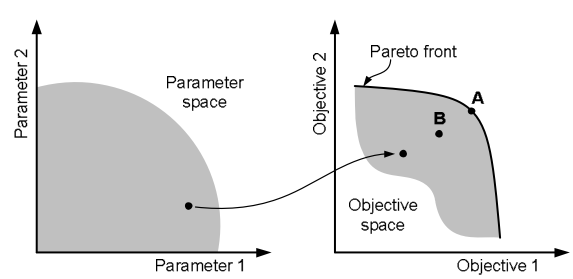

Figure 1. The relationship between parameter space and objective space.

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III. Proposed Algorithm

The key steps in the proposed algorithm are shown in Figure 2 and are discussed in deep in this section.

A. *Netlist and objective function generation*

The starting point for the proposed algorithm is a circuit topology, process models and a set of target specifications. The first step involves generating a transistor level netlist for the chosen circuit topology. From this netlist a set of designable parameters are derived which will be used to change the circuit's performance. Examples of designable parameters include a transistor's length and width or a bias current. Each parameter will have constraints imposed by the designer and once determined, these define the parameter space. The performance functions of the circuit are defined as the objective functions, for example open loop gain or phase margin. Spice testbench netlists are defined to simulate a performance for a certain set of parameters.

B. *Muti-objective optimization*

In this stage the parameter space is explored and the design improved with respect to the objective functions. The optimization, which is called multi-objective optimization (MOO), is based on an evolutionary algorithm known as weight-based genetic algorithm (WBGA) [9]. WBGA is a powerful and efficient approach that uses a genetic algorithm (GA) to determine the objective function weighting. This is unlike classical weighted optimizations which often suffer difficulties in determination of the weight vector.

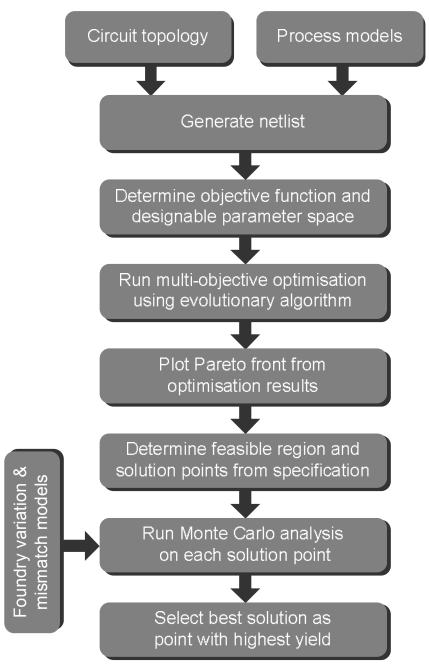

Figure 3. Novel yield targetted algorithm.

A GA string is constructed consisting of the weights for the objective functions and the designable parameters defined in the previous step. Figure 3 shows an example of a GA string for 4 designable parameters and 2 objective function weightings.

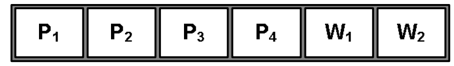

Figure 2. Construction of an example GA string.

P_1 - P_4 and W_1, W_2 are the designable parameters and performance weights respectively. The weights for the performance functions must be normalized as shown in (3).

$$w_i \leftarrow \frac{w_i}{\sum_{j=1}^{M} w_j} \tag{3}$$

During optimization, populations of individuals consisting of the GA string are randomly generated. Throughout the evolutionary algorithm, the individuals go through a process of crossover, mutation and selection from one generation to another [10]. The evolving designable parameter set replaces the existing designable parameters in the spice netlist. This new spice netlist is then simulated and the performance for each of the objective functions is determined. The performance functions are multiplied by their respective weights given by the GA string and added together to determine a total fitness score. This summation is normalized using the following formula given in (4).

$$O_{(x^{(i)})} = \sum_{j=1}^{M} w_j^{x_w^{(i)}} \frac{f_j(x^{(i)}) - f_j^{\min}}{f_j^{\max} - f_j^{\min}} \tag{4}$$

Where $f_j(x^{(i)})$ is the objective function and w_j^x is its weight. The optimization process optimizes the individual to improve its fitness score. This process will continue until the total number of generations is reached.

C. *Pareto front and feasible region*

In multi-objective optimization, where multiple conflicting objectives are important, there generally will not be a single optimum solution that optimizes all the objectives. The previous optimization step results in a number of optimal and non-optimal solutions. It is necessary at this point to determine the Pareto front which consists of the most optimal, non-dominated, solutions in the objective space. The two conditions below outline the procedure to establish these non-dominated solutions, thus giving the Pareto-front:

a) Any two solutions of the optimal set must be non dominated with respect to each other.

b) Any solution that does not belong to the optimal set is dominated by at least one member of optimal set

Having obtained the Pareto-front, the specifications of the performances are applied. The result is a set of optimal solutions that pass the specifications of the design.

D. *Monte Carlo analysis and solution selection*

The feasible region described in the previous step contains all the solutions that met the specifications. However, due to statistical variations, circuits made with these parameter sets may fall below specification when fabricated. Therefore a solution needs to be found that can provide the highest yield possible with the consideration of process variations. This is achieved using Monte Carlo analysis (MC). Monte Carlo analysis uses foundry variation models to simulate the effect of randomly selected parameter values on circuit performance [11]. Previously, MC analysis has not been a preferred method for yield analysis due to its computational cost. In the proposed approach, far fewer Monte Carlo analyses are required due to the small number of solutions in the feasible region, mitigating the computational overhead. During this step in the proposed algorithm, a Monte Carlo analysis is run for each parameter solution set that lies on the Pareto-front within the feasible region. The solution that gives the highest yield is then selected as the best solution for the design.

IV. DESIGN EXAMPLE: SYMMETRICAL OTA

This section presents a complete design example using a symmetrical operational transconductance amplifier (OTA) as the target circuit. OTAs are fundamental building blocks, employed in numerous analog circuit design applications. The OTA was selected as this has been used as the benchmark circuit in recent work in this area [7,12]. All following simulations are transistor level, using foundry BSim3v3 models for a 0.35µm AMS process and Cadence Spectre™.

A. *OTA design and objective functions*

The chosen circuit is a symmetrical OTA shown in Figure 4. The first step is to determine the designable parameters and objective function. In this example the lengths and widths of M3 to M10 make up a total of 8 designable parameters (M1 and M2 are fixed). The two performance functions for the OTA are open-loop gain and phase margin. The objective functions are given in the specification and shown in Table I.

TABLE I. OBJECTIVE FUNCTIONS

Objective function:	Specification:
Open loop gain	>50dB
Phase margin	>74deg
Area	minimized
Power	minimized

B. *Multi-objective optimization*

The designable parameters are constrained to a reasonable range and these are shown in Table II.

TABLE II. DESIGN PARAMETERS

Design Parameter:	Range:
W_1 (M5,M4)	10um - 60um
L_1 (M5,M4)	0.35µm - 4µm
W_2 (M7,M9)	10um - 60um
L_2 (M7,M9)	0.35µm - 4µm
W_3 (M10,M8)	10um - 60um
L_3 (M10,M8)	0.35µm - 4µm
W_4 (M3,M6)	10um - 60um
L_4 (M3,M6)	0.35µm - 4µm
W_{g1} (Gain weight)	0 – 1 (normalized)
W_{g2} (Phase weight)	0 – 1 (normalized)

Once the parameters have been determined, a GA string can be constructed consisting of these and the performance weightings. The corresponding string is shown in Figure 5. Due to the differences in range between the parameters, they were normalized into the same range of [0~1]. The weighting vectors have already been normalized between [0~1] using equation (3). Each individual generated by the GA will consist

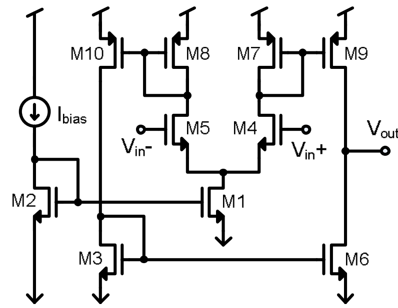

Figure 4. Symmetrical OTA topology.

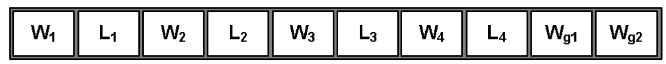

Figure 5. Construction of the GA string for this example.

of a set of designable parameters as defined by the GA String. The designable parameters are used for spice simulation and the weight vectors for the weight summation.

The same testbench netlist is used to determine both the open loop gain and phase margin for each individual. Power consumption is calculated by multiply the average supply current of the individual with the voltage supply. The area of the design is calculated by summation of the transistor active areas. The total fitness score for each individual is calculated using the normalized weighted-summation formula explained in the previous section. A total of 100 generations each with a population size of 100 are used in this case, giving the total number of samples for the optimization as 10,000. During the optimization, the GA generates and optimizes the designable parameters and weight vectors to achieve a higher fitness score, and hence optimizes the performance functions. The result of the optimization is a full set of designable parameters, weight vectors and performance functions.

C. *Pareto front and feasible region*

To illustrate the optimization, Figure 6 shows a plot of open loop gain and phase margin for the 10,000 individuals in the example. The Pareto front can be clearly seen and contains 1022 optimum solutions (circuit candidates) for the design.

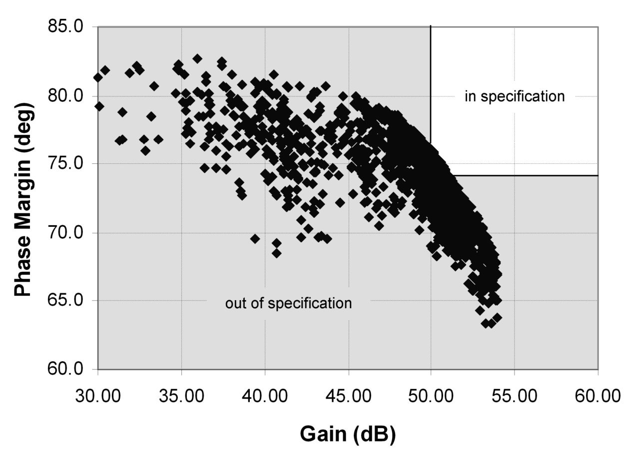

Figure 6. Gain and phase margin for the individuals.

The in-specification area is shown on the figure, which narrows down the solution space to a small feasible region. This reduced feasible region is shown in detail in Figure 7 where there are only 10 points on the Pareto front. It is these designs that are used in the next step.

D. Monte Carlo analysis and solution selection

Every optimal solution on the feasible region undergoes a Monte Carlo simulation using foundry process variation and mismatch models. 500 samples are chosen for the simulation and from these the yield percentage is calculated which is shown in Table III.

TABLE III. DESIGN POINT YIELD PERCENTAGE

Design Point:	Gain (dB):	Phase Margin (deg):	Yield (%):
1	50.05	75.9	75
2	50.17	75.8	98
3	50.35	75.5	100
4	50.46	75.3	99
5	50.54	75.2	98
6	50.57	75.1	97
7	50.72	74.9	94
8	50.81	74.6	91
9	51.04	74.2	58
10	51.06	74.1	55

The yield spread from 55% to 100% highlights the benefits of the proposed technique, for without knowledge of the yield for these optimum solutions, a designer may unwittingly choose a poor design point. Figure 7 has been shaded to indicate approximate gradients of yield. This plot is a useful tool to appreciate the design space and allows a design to be chosen that meets specification and also has maximum yield. Design point 3 would be suitable for this example design.

A summary of the parameters associated with this design example are shown in Table IV. A total of 10,000 simulations were run in the initial MOO step and from 1022 Pareto points, only 10 were in the feasible region. By concentrating only on the feasible region during the yield estimation, the computational overhead is reduced and the entire design cycle took only 48 minutes on a 1.2GHz Ultra Sparc 3 workstation. This cpu run-time compare well with previous work, for example in [7] which takes several hours of cpu time.

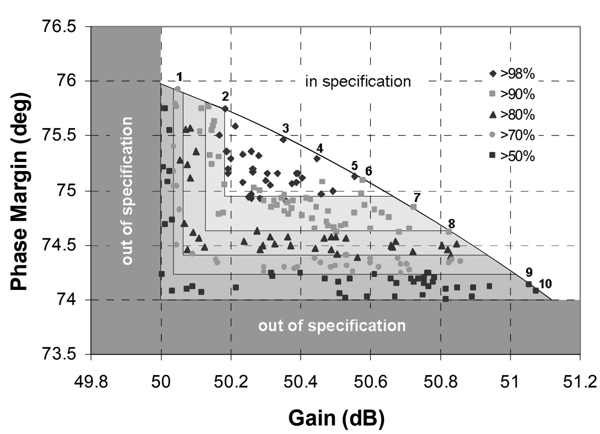

Figure 7. Gain and phase margin for individuals in the feasible region.

TABLE IV. DESIGN PARAMETER SUMMARY

Parameters:	Values:
No. Generations	100
Evaluation Samples	10,000
Pareto Points	1022
Region of Interest Points	10
CPU Time	48 minutes

V. CONCLUSIONS

In this paper a new yield characterization model has been proposed that achieves a yield optimized design from a set of optimal performance points on the Pareto front. Multi-objective optimization based on a genetic algorithm is used to explore the design space and Monte Carlo simulation is used only on the optimal solutions in the feasible region to find the design point producing the best yield percentage. The approach can be applied to any circuit topology and enjoys reduced computational overhead due to only focusing the yield simulation on a small feasible region.

VI. REFERENCES

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