Influence of nanocrystal size on the transport properties of Si nanocrystals

Xin Zhou,[1,a] Kouichi Usami,[1] M. A. Rafiq,[1,b] Yoshishige Tsuchiya,[1] Hiroshi Mizuta,[1,2] and Shunri Oda[1]

[1]*Quantum Nanoelectronics Research Center, Department of Physical Electronics, Tokyo Institute of Technology, O-Okayama, Meguro-ku, Tokyo 152-8552, Japan and SORST JST (Japan Science and Technology), Japan*

[2]*School of Electronics and Computer Science, University of Southampton, Highfield, Southampton SO17 1BJ, United Kingdom*

(Received 25 February 2008; accepted 29 April 2008; published online 30 July 2008)

In this study, we have investigated the carrier transport mechanism across silicon nanocrystals with the Al/p-Si/Si nanocrystals/Al structure. Sizes of silicon nanocrystals were controlled at diameters of ~6, ~8, and ~11 nm. It is shown that the conductivity σ of silicon nanocrystals, both as-grown and annealed, exhibits $\sigma \propto \exp[-(T_0/T)]^{1/2}$ behavior under low electrical fields and over a wide temperature range. The phenomenon of material constant T_0 increasing with the decrease of nanocrystal size has been observed. Considering nanocrystal size effect, experimental results can be explained by the hopping-percolation model. The influence of nanocrystal size on transport properties has been discussed. Based on this model, changes in T_0 after annealing treatment are attributed to an increase in effective decay length. © *2008 American Institute of Physics*.
[DOI: 10.1063/1.2952036]

I. INTRODUCTION

Semiconductor nanocrystals have attracted much interest in recent years due to their possible applications to Coulomb blockade devices, single electron transistors, and nonvolatile memories.[1–3] In order to use nanocrystals for these applications, detailed knowledge of transport mechanisms across these nanocrystals becomes necessary and is considered indispensable. Due to the diversity of the nanocrystal system, various charge-transport mechanisms have been proposed.[4] Among these are the SiO_2-embedded Si nanocrystals,[5] CdSe nanocrystal ensembles,[6] electrochemically doped PbSe nanocrystals,[7] and Ge nanocrystals contained in thin films.[8]

Most research focusing on semiconductor nanocrystal ensembles or nanocrystals embedded in an insulator matrix usually had the problem of controlling size variation within a small range. This being the case, it is difficult to investigate the influence of nanocrystal size on the conductivity of these systems. In a former report,[9] we demonstrated hopping conduction in size-controlled Si nanocrystals, 8 ± 1 nm in size, from 40 to 200 K. However, the effect of Si nanocrystals diameter variation on its transport properties still remains unexplained.

In this paper, we describe the effect of changing the diameter of Si nanocrystals in the thin layer of Si nanocrystals. In all samples with different nanocrystal sizes, we observed $\sigma \propto \exp[-(T_0/T)]^{1/2}$ dependence. This behavior can be explained well by the percolation-hopping conduction model. Based on this model, we discuss the influence of nanocrystal size on transport mechanism. We note that nanocrystal size plays a central role in the conduction process. In addition, the effect of annealing treatment has also been discussed.

II. EXPERIMENTAL DETAILS

Si nanocrystals were deposited on p-Si substrates with a resistivity of 0.02 Ω cm by very-high-frequency SiH_4 plasma cell.[10] Nanocrystal size was then varied by changing the flux of SiH_4 while keeping the flux of Ar at 90 SCCM (SCCM denotes cubic centimeter per minute at STP). The plasma power was controlled to be within 1.5–2 W. In this experiment, we prepared Si nanocrystals of diameters 6 ± 1, 8 ± 1, and 11 ± 1 nm for each sample. After Si nanocrystal deposition, a thin SiO_2 layer, about 1–2 nm in thickness, was deposited on the layer of nanocrystals by plasma-enhanced chemical vapor deposition. Because of the many voids in the nanocrystal film, this method prevents the unfavorable possibility of Al entering the nanocrystal film and touching the substrate, which can make the device short. Subsequently, electrodes that vary in size from 300×300 to 500×500 μm^2 were fabricated by Al evaporation through a metal mask. Al/p-Si/Si nanocrystals/Al device, a structure similar to that used in the previous study,[9] was fabricated. Figure 1(a) illustrates a schematic diagram of the fabricated structure. Holes are injected into the nanocrystals by applying positive voltage on p-Si substrate. A scanning electron micrograph of these nanocrystals is shown in Fig. 1(b). The size of nanocrystals has been well controlled. Each dot is covered by a SiO_2 shell 1.5 nm in thickness, which is formed by natural oxidation. Figure 1(c) demonstrates a cross-sectional view of the Si nanocrystal layer. Prior to electrode fabrication, one sample from each group was annealed in hydrogen atmosphere at a temperature of 430 °C. The detailed parameters of samples A, B, and C are listed in Table I.

[a]Electronic mail: xzhou@neo.pe.titech.ac.jp.

[b]Also at National Centre for Nanotechnology, Pakistan Institute of Engineering and Applied Sciences, Islamabad, Pakistan.

 © 2008 American Institute of Physics

Downloaded 14 Aug 2008 to 152.78.66.39. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp

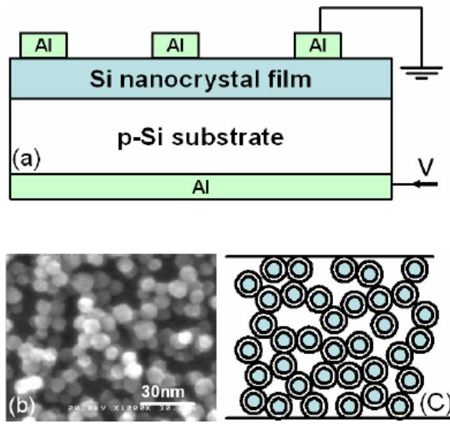

FIG. 1. (Color online) (a) Structure for the *I-V* measurements, (b) scanning electron micrograph of the Si nanocrystals, and (c) schematic cross-section view of Si nanocrystals.

III. RESULTS AND DISCUSSION

Figure 2 shows the current-voltage (*I-V*) characteristics of the Al/*p*-Si/Si nanocrystals/Al structure with different Si nanocrystal thicknesses and electrode sizes at 40 K. Curves A and C represent the *I-V* characteristics of samples A and C, respectively, having an electrode size of 500×500 μm^2. Curve B represents sample B having Si nanocrystals layer of 300 nm in thickness and 300×300 μm^2 electrode size. All curves exhibit rectifying behavior. In order to confirm whether the rectifying behavior originates from the Al/*p*-Si substrate or not, *I-V* characteristics of the Al/*p*-Si substrate/Al structure were measured at the same temperature, as shown in the inset of Fig. 2. The structure of Al/*p*-Si substrate is found to make Ohmic contact as verified by the linearity of *I-V* characteristics. The resistivity of the Si *p*-type substrate used in our device is 0.02 Ω cm, which is low enough to avoid influence from the substrate. Therefore, we assumed that the rectifying behavior originates either from Si nanocrystals/*p*-Si contact or Al/Si nanocrystals interface.

As shown in Fig. 2, the *I-V* characteristics do not scale with electrode size and reciprocal of the Si nanocrystal layer thickness. Both the voids in the nanocrystal film and the fluctuation of interface states make transport process much more complicated. In this kind of system, resistance is known to depend not only on the effective number of parallel current pathways (N_P) under electrode, the number of tunnel junction (N_S) in series, and the resistance of each junction (R_t) but also on the distribution of Si nanocrystal in lateral and vertical directions. This is also clear from scanning electron microscopy (SEM) micrograph of nanocrystals presented in Fig. 1(b). Usually, N_P and $R_i(R_t,N_S)$ scale with the density of Si nanocrystal in both vertical and lateral directions. With this in mind, we can describe it in simple formulas

TABLE I. Fabrication condition of Si nanocrystals.

Sample	Dot diameter (nm)	Thickness (nm)	Electrode size (μm^2)	Annealing temperature (°C)
A	6 ± 1	~150	500×500	430
B	8 ± 1	~300	300×300	430
C	11 ± 1	~150	500×500	430

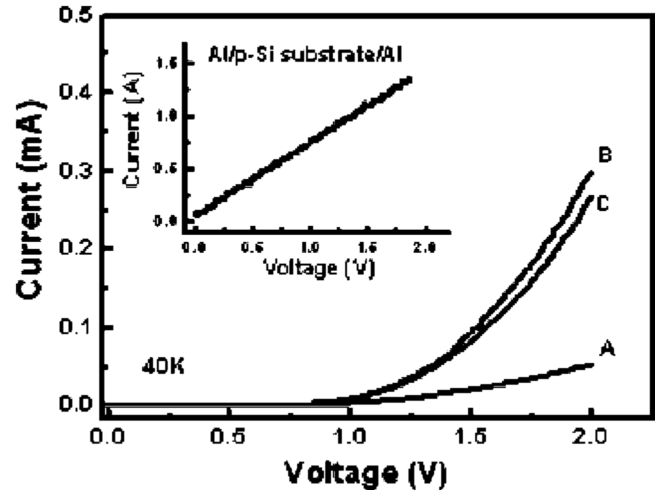

FIG. 2. *I-V* characteristics of the Al/*p*-Si/Si nanocrystals/Al structure for samples A, B, and C, measured at 40 K. The inset figure shows the *I-V* characteristics of the Al/*p*-Si substrate/Al structure also measured at the same temperature.

$$\frac{1}{R_{\text{film}}}=\sum_{i=1}^{N_P}\frac{1}{R_i}, \tag{1}$$

$$R_i=\sum_{t=1}^{N_S}R_t, \tag{2}$$

where R_i is the total resistance of each current path. For samples with the same thickness, which contain the smaller dot, R_t will be larger because of higher interface defects. Conversely, the effective number of both parallel current path (N_P) and tunnel junction (N_S) will be larger. Hence, the resistance of each sample will be mainly determined by the competition between N_P and $R_i(R_t,N_S)$. Compared with the other two samples, sample B may have a larger number of effective parallel current paths playing a more important deciding role in terms of the whole nanocrystal film's resistance.

Figure 3 illustrates the $\ln(\sigma)\propto T^{-1/2}$ plots for samples B and C from 40 to 200 K and for sample A from 60 to 200 K. The plots exhibit a linear behavior between $\ln(\sigma)$ and $T^{-1/2}$ for both as-grown and annealed samples. This indicates the same dependence of $\sigma\propto\exp[-(T_0/T)]^{1/2}$ similar to former reports.[9] We have observed an inverse relationship in this plot, that is, the slope of the $\ln(\sigma)\propto T^{-1/2}$ plot increases as nanocrystal size decreases. This $\ln(\sigma)\propto T^{-1/2}$ behavior has been frequently explained by the Efros–Shklovskii variable range hopping (ES-VRH), percolation-hopping model, and the Sheng model.[11–13] However, it has been determined that the ES-VRH model is not sufficient to explain reasonably the conduction mechanism in this kind of Si nanocrystal films.[9] In relation to this, Sheng[13] derived an $\ln(\sigma)\propto T^{-1/2}$ formula for granular metals. They proposed that s and d have some correlation. Based on that, sE_c is supposed as a constant

Downloaded 14 Aug 2008 to 152.78.66.39. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp

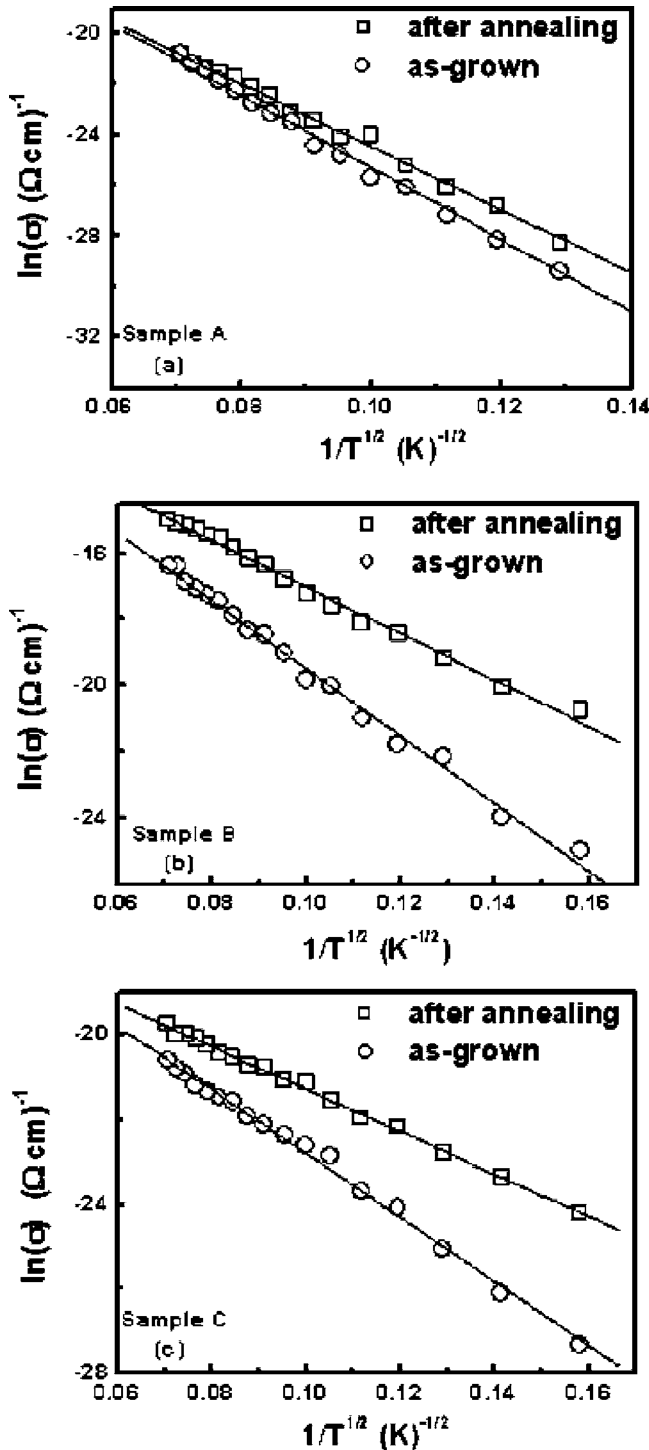

FIG. 3. $\ln(\sigma)$ as function of $T^{-1/2}$ for sample A measured from 60 to 200 K and samples B and C from 40 to 200 K, as-grown and after hydrogen annealing. The solid lines are at least squares fits to the data.

whose value depends only on the composition of the sample and the dielectric constant of the insulator. Here, s is the separation between grains, d is grain size, and E_c is charging energy. Thus, smaller E_c usually is associated with larger tunneling barrier by this rule. For our samples, there is no correlation between nanocrystal separation and size since the SiO_2 shell of each nanocrystal dot is caused by natural oxidation process. Therefore, to be able to quantitatively compare the experimental results with the theory, we used the percolation-hopping model in which T_0 is expressed by[11]

TABLE II. Estimated values of $\Delta E_{a,\max}$, T_0, α and experimental value of T_0.

Sample	$\Delta E_{a,\max}$ (meV)	T_0 (Calc.)	T_0 (Expt.)	α (Calc.)
A	121	2.11×10^4	2.24×10^4	0.093
B	62	1.07×10^4	1.04×10^4	0.103
C	32	5.22×10^3	5.33×10^3	0.105

$$T_0 = \frac{2P_c s_{\max} E_{a,\max}}{k_B \alpha}. \quad (3)$$

Here, P_c is the percolation threshold, $s_{\max}$ is the maximum separation of particles in the current path, k_B is the Boltzmann constant, and α is the effective decay length for the wave functions of carriers in the insulating region. According to this model, each nanocrystal semiconductor is characterized by (i) charging energy E_c and (ii) E_d, which is the degree of the conduction band edge shift from the bulk edge due to size quantization. Hence, if a nanocrystal is surrounded by many nanocrystals, the charging energy of the nanocrystal is expressed as[15]

$$E_c = \frac{e^2}{4\pi\varepsilon\varepsilon_0}\frac{1}{d}\left[\frac{s/d}{0.5+s/d}\right]. \quad (4)$$

The expression for E_d is elucidated by[16]

$$E_d = \frac{\hbar^2\pi^2}{2m^*}\frac{1}{(d/2)^2}. \quad (5)$$

Here, the maximum value of the activation energy is considered as $E_{a,\max}=E_{d,\max}+\Delta E_c$. $E_{d,\max}$ is the largest degree of conduction band edge shift. ΔE_c is the difference in charging energy between the large and small nanocrystals. P_c is then chosen as 0.25 as an approximation corresponding to a simple cubic lattice.[9] Employing the definition of nanocrystal separation as the distance between the edges of nanocrystals, the $s_{\max}$ in our sample is independent of dot size and can roughly be considered at a constant ~ 3 nm. Sheng *et al.*,[14] however, pointed out that the decay rate of electron wave function in the oxide can roughly be evaluated as $\chi \approx \sqrt{2m\Phi/(h/2\pi)^2}$, where m denotes the carrier effective mass, Φ is the effective barrier height, and h is the Planck constant. Using $\alpha=1/\chi$ with an average hole effective mass of $0.57m_0$ (Ref. 17) and a barrier height of $\Phi\sim 4.7$ eV (Ref. 18) for holes, α is approximately 0.1 nm. Using the values of the above parameters, T_0 was calculated by Eq. (3) and the results are summarized in Table II. From the experimental results, we have observed that T_0 is independent of the nanocrystal layer thickness but is dependent on dot size. It is evident from Eq. (3) that T_0 is dependent on $s_{\max}$, $E_{a,\max}$, and α. For our samples, there is nearly no change in $s_{\max}$ when the size of nanocrystals decreases. Since E_c and E_d are functions of d^{-1} and d^{-2}, respectively, the reduction of dot size makes significant increases in E_c and E_d. $E_{a,\max}$ increases and becomes much more sensitive to the size of the nanocrystal as its size decreases. Therefore, T_0 increases as nanocrystal size decreases, which supports experimental results. As for the decay length, due to higher surface states and interface defects, the barrier height of the smaller nanocrystals is

Downloaded 14 Aug 2008 to 152.78.66.39. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp

higher. Consequently, with a decrease in nanocrystal size, the effective decay length α for the holes in the SiO_2 region usually becomes smaller. The measurement result of T_0 and Eq. (3) is used to calculate α; the results are listed in Table II. We can easily perceive that α depends on the size of the nanocrystals.

After annealing treatment, the slope of the $\ln(\sigma) \propto T^{-1/2}$ plot for each sample decreases. The T_0 of samples A, B, and C changes to 1.54×10^4, 4.97×10^3, and 2.53×10^3, respectively. This can be seen from the above discussion that change of $E_{a,\max}$ and α can influence T_0. In order to determine the actual influence of hydrogen annealing treatment, some analyses based on Eq. (3) were performed. For sample B, let us consider $\alpha \sim 0.1$ nm. T_0 (after annealing) is gained from Fig. 3. Then, Eq. (3) gives the value $E_{a,\max} = 29$ meV, as the value of $E_{a,\max}$ has a direct relationship with nanocrystal size. Thus, with the comparison between the $E_{a,\max}$ of annealed sample B and as-grown sample C, it is reasonable to conclude that the nanocrystal size, after annealing, should increase to be larger than 10–12 nm. Verification of this change can be done by SEM. However, we did not find any change in the nanocrystal size after annealing treatment from SEM. Therefore, the change in slope is due to a decrease in α, as indicated by Eq. (3). This is attributed to hydrogen annealing treatments that reduce the interface defects of SiO_2/Si, especially the dangling bonds, due to the *H*-passivation effect. This change of α can also be roughly evaluated by Eq. (3).

IV. CONCLUSION

We have studied the transport mechanism across size-controlled Si nanocrystal films. We have investigated the influence of nanocrystal size on conduction mechanism. Samples with different dot sizes exhibited $\ln(\sigma) \propto T^{-1/2}$ dependence. Slopes of $\ln(\sigma) \propto T^{-1/2}$ increase with the decrease in nanocrystal size. The $\ln(\sigma) \propto T^{-1/2}$ dependence can be explained by the percolation-hopping model. Using this model, the change in slopes of $\ln(\sigma) \propto T^{-1/2}$ curves after annealing treatment is associated with a change in α.

ACKNOWLEDGMENTS

This work was partly supported by KAKENHI (Grant No. 19206035). M.A.R. is a JSPS postdoctoral fellow.

[1]Y. T. Tan, Z. A. K. Durrani, and H. Ahmed, J. Appl. Phys. **89**, 1262 (2001).
[2]M. A. H. Khalafalla, H. Mizuta, and Z. A. K. Durrani, Phys. Rev. B **74**, 035316 (2006).
[3]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[4]H. E. Romero and M. Drndic, Phys. Rev. Lett. **95**, 156801 (2005).
[5]I. Balberg, E. Savir, J. Jedrzeijewski, A. G. Nassiopoulou, and S. Gardelis, Phys. Rev. B **75**, 235329 (2007).
[6]D. Toker, I. Balberg, O. Zelaya-Angle, E. Savir, and O. Millo, Phys. Rev. B **73**, 045317 (2006).
[7]B. L. Wehrenberg, D. Yu, J. S. Ma, and P. Guyot-Sinonnest, J. Phys. Chem. B **43**, 109 (2005).
[8]S. Banerjee, S. Nozaki, and H. Morisaki, Appl. Phys. Lett. **76**, 445 (2000).
[9]M. A. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, S. Uno, Z. A. K. Durrani, and W. I. Milne, J. Appl. Phys. **100**, 014303 (2006).
[10]T. Ifuku, M. Otobe, A. Itoh, and S. Oda, Jpn. J. Appl. Phys., Part 1 **36**, 4031 (1997).
[11]E. Šimánek, Solid State Commun. **40**, 1021 (1981).
[12]A. L. Efros and B. I. Shklovaskii, J. Phys. C **8**, L49 (1975).
[13]P. Sheng, Phys. Rev. Lett. **31**, 44 (1973).
[14]P. Sheng and B. Abeles, Phys. Rev. Lett. **28**, 34 (1972).
[15]B. Abeles, P. Sheng, M. D. Coutts, and Y. Arie, Adv. Phys. **24**, 407 (1975).
[16]G.-F. Hohl, S. D. Baranovskii, J. A. Becker, F. Hensel, S. A. Quaiser, and M. T. Reetz, J. Appl. Phys. **78**, 7130 (1995).
[17]R. A. Smith, *Semiconductors*, 2nd ed. (Cambridge University Press, Cambridge, 1978).
[18]T. Feng, G. Miller, and H. A. Atwater, J. Appl. Phys. **102**, 034305 (2007).

Downloaded 14 Aug 2008 to 152.78.66.39. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp