Study of Single-Charge Polarization on a Pair of Charge Qubits Integrated onto Silicon Double Single-Electron Transistor Readout

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Abstract— **This paper reports on integration of two Si charge quantum bits (qubits) and series-connected double single-electron transistors (DSETs) as a readout for the first time. We design and fabricate the DSETs composed of double quantum dots (DQDs) connected in series with two side gates patterned on a silicon-on-insulator substrate. The individual SETs are sufficiently sensitive to detect single-charge polarization on the adjacent charge qubits. The fabricated DSETs are characterized at the temperature of 4.2 K by changing the gate voltages applied to two side gates. The measured Coulomb oscillation characteristics exhibit a clearly-defined hexagon pattern, manifesting that the patterned DQDs of the DSETs indeed act as interacting charging islands. These results agree very well with the results of equivalent circuit simulation combined with three-dimensional capacitance simulation. Furthermore, we simulate how single-charge configurations on two charge qubits are sensed with the DSETs by using the measured electrical characteristics for the DSET and the equivalent model. Finally, the scaling-up properties of the proposed system to multiple single-electron transistors (MSETs) is discussed by simulating Triple Single-Electron Transistors (TSETs) with triple qubits.**

Index Terms— **Double Quantum Dots, Qubit, Single-Electron Transistor, Double Single-Electron Transistor, Three-Dimensional Capacitance Simulation**

I.   INTRODUCTION

SOLID state quantum bits (qubits) are a promising candidate to realize practical quantum computers due to their scalabilities [1, 2]. Semiconductor based Double Quantum

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Dots (DQDs) have extensively been studied as desired charge qubits. Coherent operations of DQDs consisting of GaAs:AlGaAs hetero-structures have first been demonstrated, where the dots were realized with a two-dimensional electron gas depleted by using surface gates [3]. Coherent operations of Si based DQDs have also been reported with showing a much longer decoherence time [4]. The silicon based DQDs have been fabricated on the silicon-on-insulator (SOI) substrate using electron beam lithography and reactive ion etching technique. For achieving fault tolerant quantum computation, decoherence time of the qubits should be increased further, and it has also been examined to adopt double nanocrystalline silicon quantum dots deposited by VHF plasma deposition technique for realizing extremely downscaled charge qubits [5]. Furthermore, two qubits operations using electrostatic interaction have also been studied [6].

Another key issue to tackle is to establish the way to integrate multiple qubits with appropriate readout devices. To readout extremely-small charge polarizations on the DQDs, single-electron transistors (SETs) have often been used [4, 5] because of their ultra high charge sensitivity. The theoretical limit of charge sensitivity for a SET is about $1 \times 10^{-6} \ eHz^{-1/2}$ [7]. This enables us to detect very small changes in the charge distribution on the DQD capacitively-coupled to the SET. A pair of Al/AlOx SETs have also been adopted for reading charge polarization in Al/AlOx based quantum cellular automata (QCA) system [8,9] and Si:P QCA system [10]. A pair of SETs is definitely useful to detect single-charge polarizations in large dots in QCA system. However several single-island SETs are not proper to detect single-charge polarizations in several nanoscale DQDs because the lead electrodes connected to the SETs islands are relatively large. As for small qubits composed of DQDs, virtually no study has been reported on the architecture of suitable readout devices, which should be designed from the stand-point of total integration of all the key components. In this paper we propose multiple single-electron transistors (MSETs) as a readout for multiple qubits, where SETs are connected in series for sensing the charge polarization on multiple qubits. In the past studies, independent SETs were prepared for sensing the individual qubits, but this readout layout occupies a large area on the substrate. Advantage of using our MSETs readout is that it can
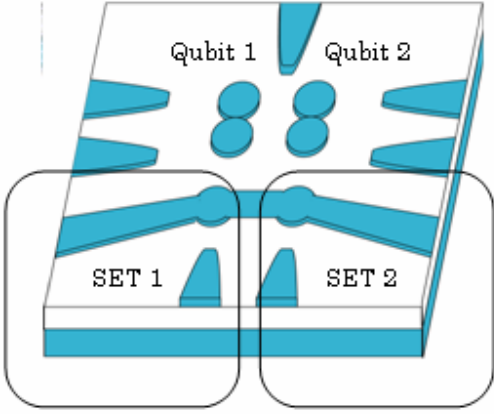
Fig.1 Schematic top view of the DSETs. SET 1 and SET 2 are sensitive to charge polarizations in Qubit 1 and Qubit 2.

easily be scaled-up along with increasing the number of qubits with keeping its occupation area to be minimized. In the present work, as a first step to realize multiple qubits readout, we fabricated double single-electron transistors (DSETs). A schematic top view of the DSETs, qubits and their control gates is shown in Fig.1. Individual SETs within the DSETs work to sense their adjacent qubits. Namely, SET 1 and SET 2 can be used to sense Qubit 1 and Qubit 2. In this paper, we fabricate and characterize the DSETs and demonstrate how single-charge polarization on two charge qubits integrated adjacent to the DSETs can be detected by using the DSETs.

In Section II, we fully describe a fabrication method of the DSETs and qubits. In Section III we report on the experimental characteristics for the DSETs at 4.2 K. We then analyze the DSETs characteristics by using the three-dimensional capacitance simulation and the single-electron equivalent circuit simulation. After that, we discuss detection of single-charge polarizations on a pair of qubits. Finally, the scaling-up to MSETs is studied by simulating Triple Single-Electron Transistors (TSETs) with triple qubits in Section IV.

II. DEVICE FABRICATION

All of devices reported in this paper were fabricated from the silicon on insulator (SOI) substrate. Initially, the SOI layer thickness and buried oxide (BOX) layer thickness were 100 nm and 200 nm respectively. Phosphors at concentration of 10^{19} cm^{-3} were doped into SOI layer. Repeated thermal oxidation and wet etching process was carried out to reduce SOI thickness to 40 nm. Schematic top view of the DSETs with qubits is shown in Fig. 1. The upper colored region indicates SOI layer, the bottommost colored region indicates the silicon substrate with phosphorous doping level of 10^{15} cm^{-3}, and the white region indicates the BOX region.

At first the negative resist RD-2000N of 60 nm thickness was coated for electron-beam (EB) direct writing. Although RD-2000N was primarily developed as a deep ultraviolet resist, it shows good sensitivity to EB exposure [11]. This resist also offers good endurance characteristic to reactive ion etching
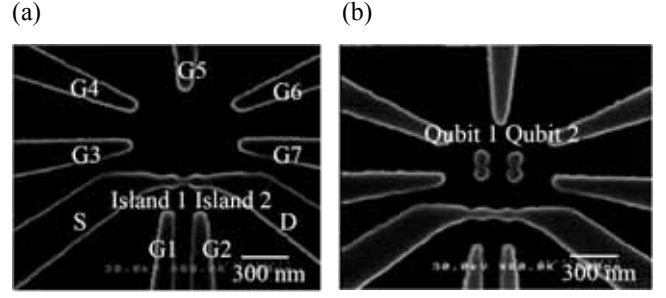
(a)   (b)

Fig.2 SEM image of the DSETs and qubits gates: (a) without qubits; (b) with qubits

(RIE), high-resolution and simple handling. Two charging islands connected in series, two SET-gates (G1 and G2) and five qubit control gates (G3-G7) were patterned using JBX-5FE made by JEOL and electron cyclotron resonance RIE (ECR-RIE). Fig. 2 (a) and Fig. 2 (b) indicate SEM images of the fabricated DSETs without qubits and with qubits respectively. SET gate G1 was positioned at the distance of 140 nm from SET Island 1, G2 at the distance of 130 nm from SET Island 2, shown in Fig. 2 (a) and Fig. 2 (b) and each individual qubit was positioned at the distance of approximately 190 nm from the most adjacent SET island, as it is shown in Fig.2 (b). The lithographically defined diameters of the islands were approximately 70 nm. The adjacent constrictions that act as tunnel barriers are 30 nm large. After that, the patterns were thermally oxidized at 1000 to passivate the surface states and reduce the effective thickness of the SOI down to approximately 30 nm. The final oxidation leads to effective islands diameter of approximately 45 nm.

III. MEASUREMENTS AND CHARACTERIZATION

A. Electrical Characterization for DSETs

All electrical measurements are carried out at the temperature of 4.2 K for the DSETs device. The equivalent circuit of the DSETs is shown in Fig. 3 (a). At first, electrical measurements for SET 1 and SET 2 are individually performed to characterize each SET in the DSETs. Figure 4 (a) and 4 (b) show the contour plots of differential conductance ($\partial I_D / \partial V_D$) as a function of V_{G1}, V_D and V_{G2}, V_D, respectively. Small and large
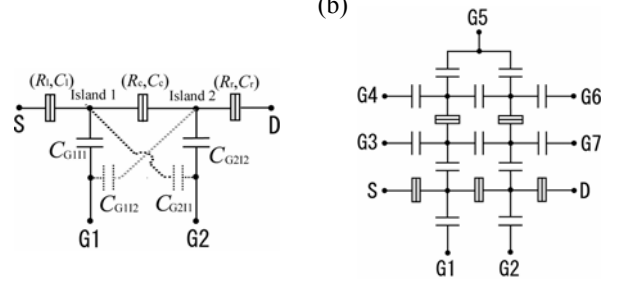
(a)   (b)

Fig3. Equivalent circuits of: (a) the DSETs; (b) the DSETs with qubits. Although cross-capacitances are not shown for clarity, they are included in the simulations.
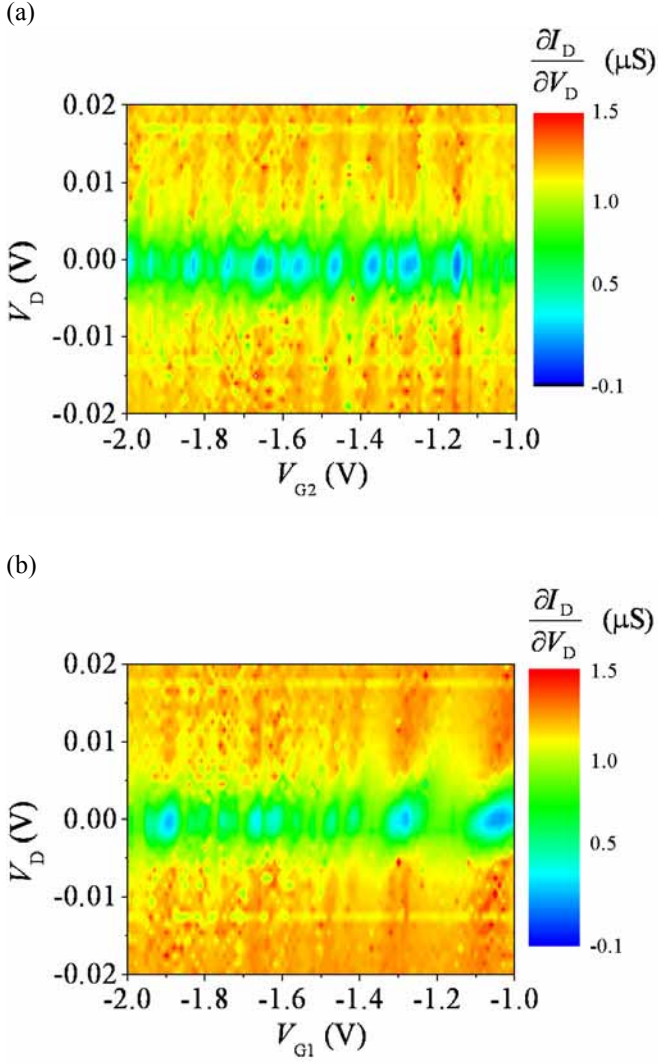
(a)

(b)

Fig. 4 Coutour plots of the measured differential conductance ($\partial I_D/\partial V_D$) a function of; (a) V_{G1} and V_D; (b) V_{G2} and V_D at 4.2 K.

were observed from the plots. That confirms that two islands are present in the fabricated structure. Contour plot of I_D as a function of V_{G1} and V_{G2} is shown in the Fig. 5 (a) for the source-drain bias of 500 µV. The current flowing in the off-triple-point regime can be ascribed to inelastic co-tunneling due to thermal energy on the present condition rather than elastic co-tunneling through virtual process. Capacitance values can be extracted from the experimental data shown in Fig. 5 (a). When cross-capacitances are not called into account, the capacitances are extracted by using equations given in [12]. To estimate capacitances properly including cross-capacitances, following equations are required:

$$C_{G1I1} = \frac{|e|}{\Delta V_{G1} + \dfrac{\Delta V_{G2}^{c}}{\Delta V_{G2}^{n}} \Delta V_{G1}^{m}} = \frac{|e|}{\Delta V_{G1}^{n} - \dfrac{\Delta V_{G2}^{c}}{\Delta V_{G2}^{n}} \Delta V_{G1}^{c}} \quad (1)$$
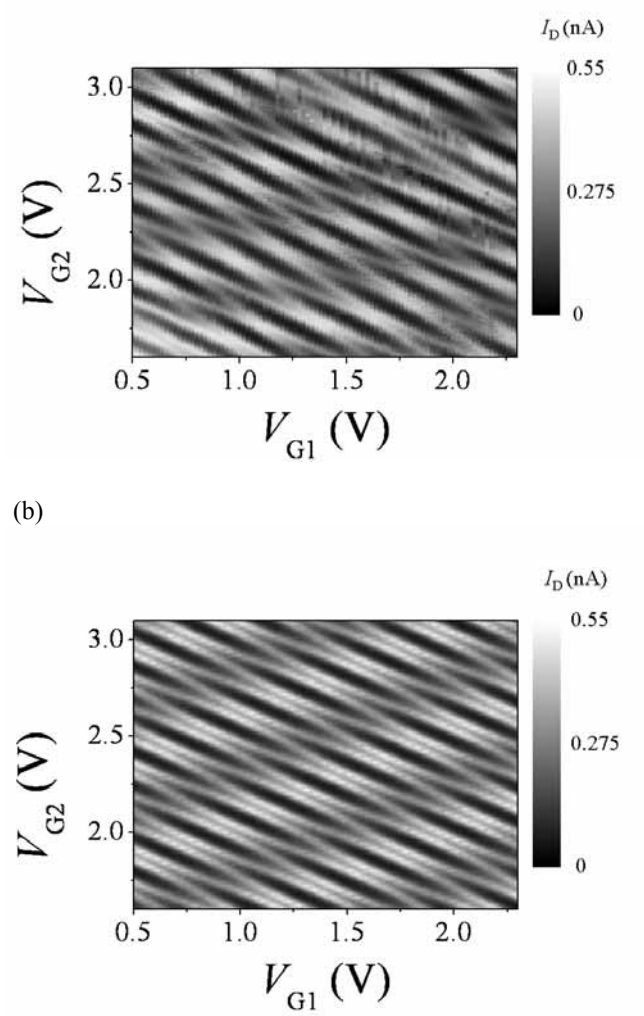
(a)

(a)

(b)

Fig. 5 Contour plots of; (a) the measured and; (b) the simulated I_D as a function of V_{G1} and V_{G2} with $V_D = 500$ µV at 4.2 K.

$$C_{G2I2} = \frac{|e|}{\Delta V_{G2} + \dfrac{\Delta V_{G1}^{c}}{\Delta V_{G1}^{n}} \Delta V_{G2}^{m}} = \frac{|e|}{\Delta V_{G2}^{n} - \dfrac{\Delta V_{G1}^{c}}{\Delta V_{G1}^{n}} \Delta V_{G2}^{c}} \quad (2)$$

$$C_{G1I2} = \frac{|e|}{\Delta V_{G1}^{m} + \dfrac{\Delta V_{G2}^{n}}{\Delta V_{G2}^{c}} \Delta V_{G1}} = \frac{|e|}{\dfrac{\Delta V_{G2}^{n}}{\Delta V_{G2}^{c}} \Delta V_{G1}^{n} - \Delta V_{G1}^{c}} \quad (3)$$

$$C_{G2I1} = \frac{|e|}{\Delta V_{G2}^{m} + \dfrac{\Delta V_{G1}^{n}}{\Delta V_{G1}^{c}} \Delta V_{G2}} = \frac{|e|}{\dfrac{\Delta V_{G1}^{n}}{\Delta V_{G1}^{c}} \Delta V_{G2}^{n} - \Delta V_{G2}^{c}} \quad (4)$$

where C_{G1I1}, C_{G2I2}, C_{G1I2}, and C_{G2I1} are capacitances between G1 and Island 1, between G2 and Island 2, between G1 and Island 2, and between G2 and Island 1, respectively, and ΔV_{G1}, ΔV_{G2}, ΔV_{G1}^{m}, ΔV_{G2}^{m}, ΔV_{G1}^{c}, ΔV_{G2}^{c}, ΔV_{G1}^{n}, ΔV_{G2}^{n}, ΔV_{G1}^{g} and ΔV_{G2}^{g} are voltage periods shown in Fig. 6, and e is the elementary charge. The extracted capacitance values are
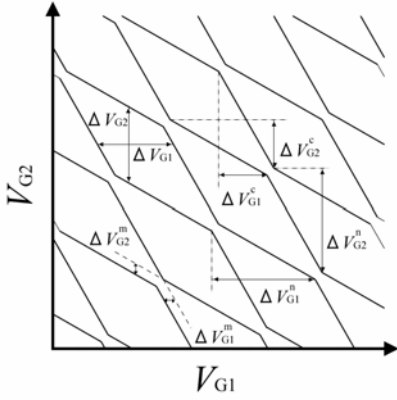
Fig.6 Schematic periodic structure of the phase diagram as a function of V_{G1} and V_{G2}. Capacitance values are extrated by using voltage periods, ΔV_{G1}, ΔV_{G2}, ΔV_{G1}^{m}, ΔV_{G2}^{m}, ΔV_{G1}^{c}, ΔV_{G2}^{c}, ΔV_{G1}^{n}, ΔV_{G2}^{n}, ΔV_{G1}^{g} and ΔV_{G2}^{g} shown in this figure.

C_{G1I1}=0.52 aF, C_{G2I2}=1.05 aF, C_{G1I2}=0.38 aF, and C_{G2I1} =0.75 aF.

To confirm the capacitance values, the simulation of the equivalent circuit shown in Fig. 3(a) is performed by using simulator CAMSET [13]. In this simulation electron tunneling rate through a barrier is expressed as the following equation from "Orthodox theory" [14, 15]:

$$\Gamma = \frac{1}{e^2 R_t} \frac{-\Delta F}{1 - \exp\left(\Delta F / k_B T\right)} \qquad (5)$$

where ΔF is the total energy variation related to the electron tunneling, R_t is the tunnel resistance of the junction, k_B is the Boltzman constant, and T is the temperature. Tunneling rates are computed at each step for all possible events, and then one of them is chosen, based on the relative probabilities. In this simulation, elastic co-tunneling through virtual process is not included, but inelastic co-tunneling due to thermal energy is treated. As the expected couplings between the islands and the electrodes are strong due to the bigger charging islands and the measurement temperature is 4.2 K, it is considered that the DSETs device meets the following conditions:

$$E_k \langle\langle k_B T \langle\langle E_c \qquad (6)$$

where, E_k is the quantum kinetic energy and E_c the charging energy of one island. Although this simulation does not account for the quantization of electronic energy, it is a suitable comparison method with the experimental results when the above condition is satisfied. By substituting the extracted capacitance values into the DSETs equivalent circuit, the simulation reproduces almost the same characteristic as the experimental result (Fig. 5(b)). In the present simulation we assumed the capacitance parameters are constant throughout the entire bias voltages of V_{G1} and V_{G2}. In reality, however, the capacitance parameters are expected to vary slightly with the applied gate voltages. Small discrepancy between the simulation and experimental results seen for lower V_{G1} and V_{G2} are attributed to our voltage-independent capacitance model.

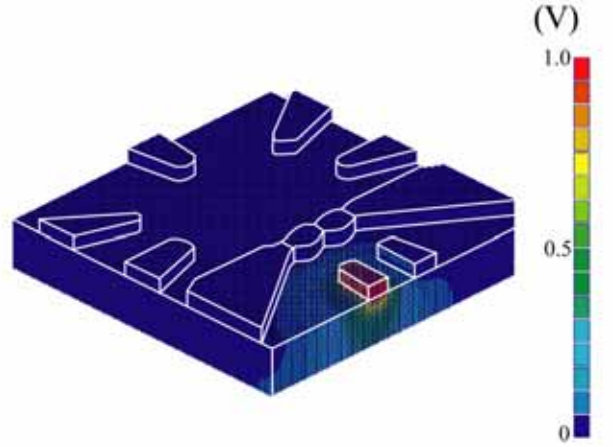To characterize the DSETs furthermore, three-dimensional

Fig. 7 The potential distributions on the condition of V_{G1}=1 V and the other electrodes grounded.

capacitance analysis is carried out by using simulator VOLT [16]. In this capacitance simulation, potential distributions are calculated by solving three-dimensional Poisson's equations on specific boundary conditions [5]. The capacitance matrix is extracted by computing the electric flux flowing into the SET islands. The simulated potential distribution regarding the DSETs structure is shown in Fig. 7. This figure, for example, depicts the potential distribution when voltage of 1 V is applied to G1 and the other electrodes are grounded. C_{G1I1} and C_{G1I2} are then estimated from this boundary condition. C_{G2I1} and C_{G2I2} can also be estimated in the same way by applying 1V to G2. The calculated capacitance values are C_{G1I1}=0.84aF, C_{G2I2}=0.94 aF, C_{G1I2}=0.50 aF, and C_{G2I1}=0.63 aF. These capacitance values are similar to the experimental results. This supports the islands were not formed by random fluctuations of dopant potential [17], but well defined geometrical confinements.

B. Detection of single-charge polarizations on double qubits

To estimate the effects of single-charge polarizations in qubits, capacitance values regarding the qubits and their control gates are also extracted by solving three-dimensional Poisson's equations. Here, each individual qubit is positioned at the distance of approximately 190 nm from the most adjacent SET charging island. By substituting the simulated capacitance values for qubits and their control gates, and the experimental capacitance values for the DSETs, into the equivalent circuit (Fig. 3 (b)), the effect of various charge polarizations in two qubits on the DSETs was characterized. Fig. 3 (b) shows the equivalent circuit of the whole device including a pair of qubits and their control gates. Although cross-capacitances are not shown for clarity in the figure, the capacitances are included in the simulation. Fig. 8 (a) and Fig. 8 (b) show simulated characteristics for charge configurations in the DQDs shown in inset figures. In the inset figure, Qubit 1 and Qubit 2 indicate left and right qubits, respectively. Fig. 8 (a) shows contour plot of I_D as a function of V_{G1}, V_{G2} and at V_D=500 μV when charge polarizations $-e$ and $+e$ are in the bottom and the top dot in
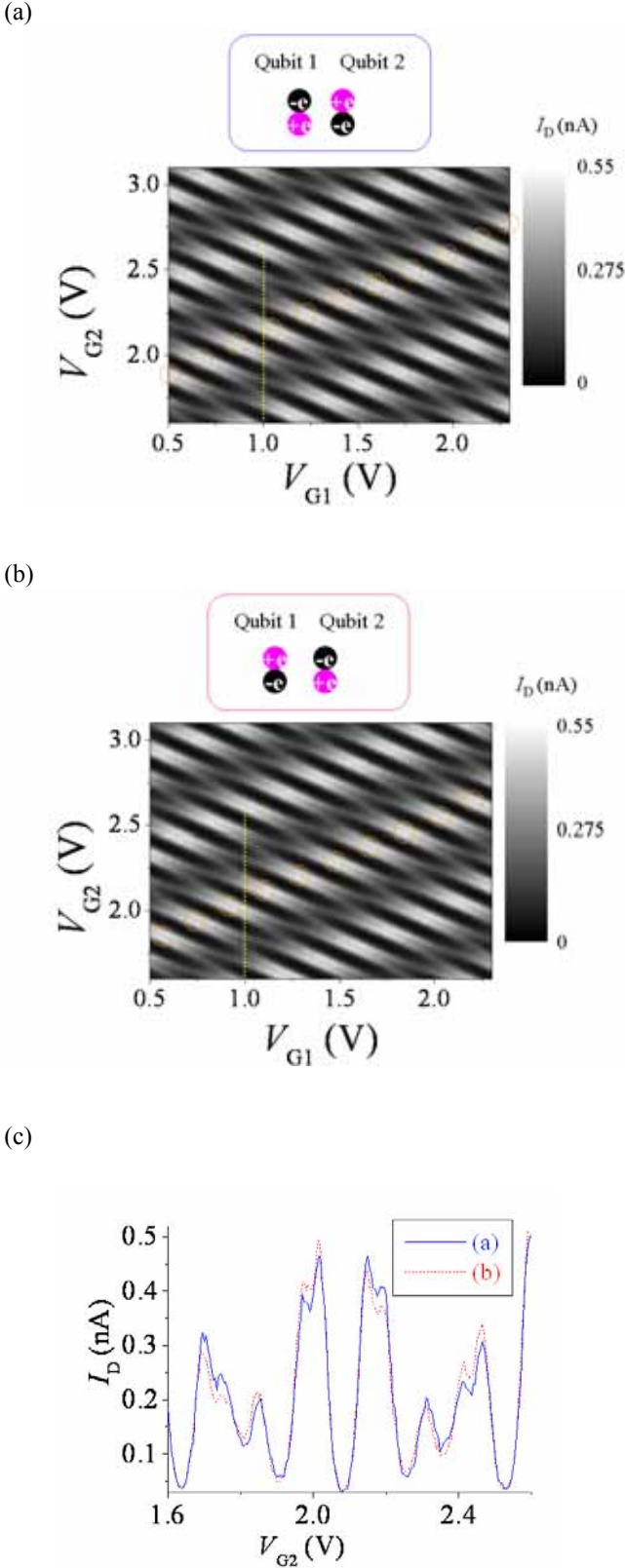
(a)

(b)

(c)

Fig.8 (a), (b): Contour plots of the simulated I_D as a function of V_{G2} with $V_D =$ 500 μV at 4.2 K for charge polarizations shown in inset figures. (c) I_D-V_{G2} at V_{G1}=1.0 V shown as dotted lines in (a) and (b)

Qubit 1, and $+e$ and $-e$ are in the bottom dot and the top dot in Qubit 2. Fig. 8 (b) shows the contour plot of I_D as a function of V_{G1}, V_{G2} and at V_D=500 μV when the opposite charge polarizations to Fig. 8 (a) are adopted. Triple points in Fig. 8 (b) are shifted toward right bottom direction as compared with the same points in Fig. 8 (a). Fig. 8 (c) shows I_D-V_{G2} characteristic at V_{G1}=1.0 V shown as dotted lines in Fig. 8 (a) and Fig. 8 (b). The effects of these polarization conditions on the DSETs can be easily understood from the plot. The results show the current difference of the order of several tens pA for two single-charge configurations over the maximum DSETs current of around 0.5 nA. Such current difference is certainly measurable experimentally by using the SET charge detectors as demonstrated by J. Gorman *et. al.* [4].

Similar kinds of analysis for the Al/AlOx based QCA systems [8, 9] support our characterization. However, it can be noted that the sizes of our islands and qubits, quite smaller than the islands in those QCA researches, enables us to characterize the DSETs at 4.2 K. Furthermore, instead of analyzing the single-charge polarizations in two dots connected to electrodes, we characterized single-charge polarizations in the isolated DQDs to be detectable by using the DSETs.

IV. DISCUSSION ON SCALING-UP PROPERTIES

For discussing the possibility of scaling-up the proposed qubit-readout structure, we also analyzed the system of triple qubits integrated with triple single-electron transistors (TSETs) (Fig. 9 (a)) by applying the same simulation method. Figure 9 (b) shows the contour plot of I_D calculated for the TSETs as a function of V_{G1} and V_{G2} with V_D=500 μV and V_{G3}=0 V. Figure 9 (c) shows I_D-V_{G2} characteristic with V_D=500 μV, V_{G1}=1 V and V_{G3}=0 V for the three charge configurations shown in the inset to Fig. 9 (c). We show, for clarity, only three charge configurations where one qubit is oppositely polarized to the other two qubits. These charge configurations are relatively difficult to be distinguished one another. The magnitude of the change in the peak currents seen in the figure can be detectable, and the ratios of the peak current changes to the overall current level are similar to those obtained for the DSETs.

In general, the dependence of tunnel currents on multiple gate voltages for our MSETs reflects the charge stability diagram for the multiple charging islands. As seen both for DSETs and TSETs, the single-charge polarization on the multiple qubits results in the shift of the entire current - voltage curve in a certain direction in the multi-dimensional current - voltage space. Rich domain structures seen for the current - voltages characteristics allow us to detect such current shifts in any directions. The characteristics for the DSETs and TSETs are indeed suited for detecting the double and triple charge qubits. If we detected the triple charge qubits by using a single SET (or the DSETs), we would certainly lose some information as the three-dimensional patterns in the I_D-V_{G1}-V_{G2}-V_{G3} space are projected into the one-dimensional I_D-V_{G1} space (or the two-dimensional I_D-V_{G1}-V_{G2} space). For clarifying this point, we show the results for the triple charge qubits with a single
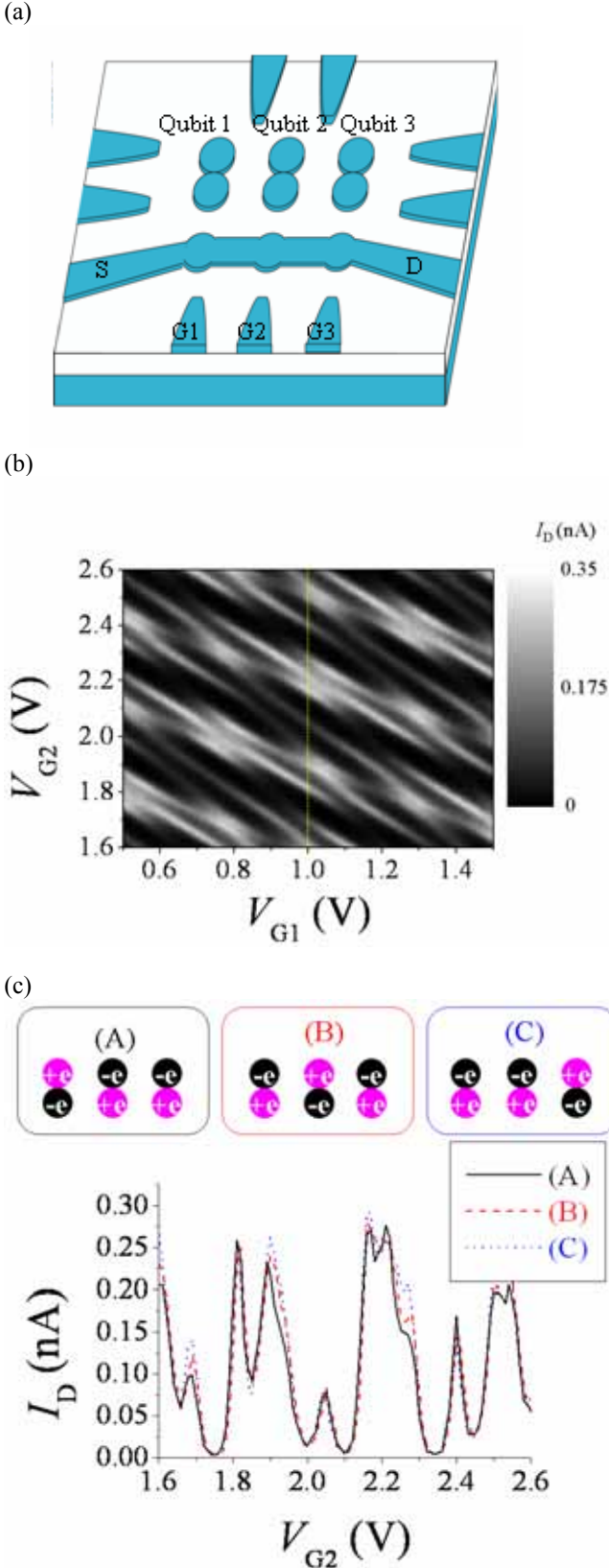
(a)

(b)

(c)

Fig. 9 (a): Schematic top view of the TSETs. (b) Contour plot of the simulated TSET$_S$ I_D as a function of V_{G1} and V_{G2} with V_D=500 μV and V_{G3}=0 V at 4.2 K for no charge polarizations in triple qubits. (c) I_D-V_{G2} at V_{G1}=1.0 V and V_{G3}=0 V. the inset figures show charge polarizations in triple qubits. The leftmost qubit, the central qubit and the rightmost qubit indicate qubit 1, qubit 2, and qubit 3, shown in Fig. 9(a), respectively.
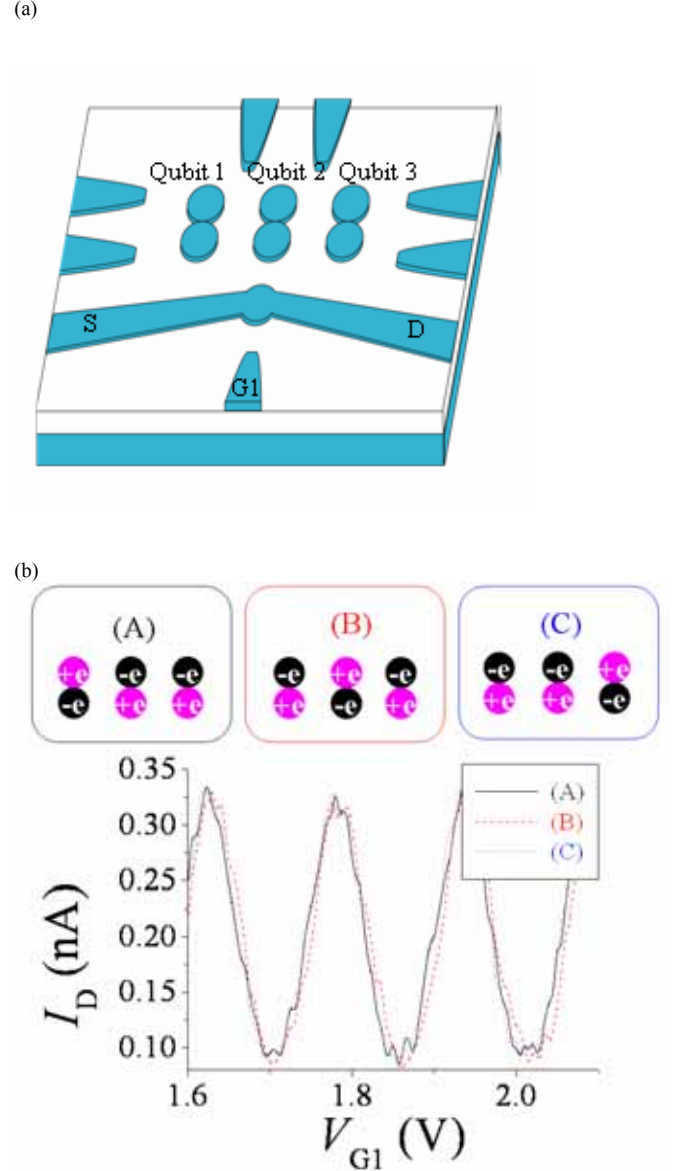
(a)

(b)

Fig.10 (a): Schematic top view of a single-SET (conventional SET) with three qubits, (b) I_D-V_{G1} with V_D=150 μV at 4.2 K for the device structure of Fig. 10 (a). The inset figures show the corresponding charge polarization configurations in three qubits.

SET readout (Fig. 10). For this plot, source-drain bias of 150 μV is chosen for the maximum drain current to be comparable with that of Fig. 9, because the resistance in the single SET is reduced by subtracting two tunnel barriers from the TSETs. In this structure, the impacts of Qubit 1 and Qubit 3 on the single SET characteristics are superposed with those of Qubit 2. As distances of three qubits relative to the charging island cannot differ a lot for maintaining good sensitivity, the different polarizations (A), (B) and (C) shown in the inset to Fig. 10 (b) are hardly discriminated individually. On the other hand, the rich characteristics of TSETs make it possible to produce the current difference of the order of several tens pA at the specific gate voltages among the charge polarizations of (A), (B) and (C). It should be noted that the advantage of the MSETs is quite universal and not affected by the existence of any

cross-capacitances, for example, the capacitance between Island 1 and Qubit 2 for the system of the DSETs with double qubit system. Furthermore, it will also be increasingly difficult to locate individual single-SETs close to multiple qubits in terms of their physical layout. If we do not have a readout allocated for a particular qubit in the system, we may transfer the information on the qubit to the nearest qubit with a readout, by conducting the SWAP gate operation. However, this requires three Controlled Not (CNOT) gate operations [18] and may cause the serious delay in computation.

V. CONCLUSION

We fabricated the DSETs to detect single-charge polarization on a pair of qubits independently. Operation of the individual SETs was successfully demonstrated, and the electrical characteristics measured for the DSETs were validated by comparing with the equivalent circuit simulations and three-dimensional capacitance simulations. We also found out by using the DSETs measured electrical characteristics and the equivalent model that single-charge configurations on a pair of qubits could be distinguished with the DSETs. Furthermore the TSETs simulation exhibits significant potential for the scaling-up to MSETs.

ACKNOWLEDGMENT

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