Detection of Single-Charge Polarisation in Silicon Double Quantum Dots by Using Serially-Connected Multiple Single-Electron Transistors

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***Abstract*—We investigate novel serially-connected multiple single-electron transistors (MSETs) as a single-charge polarisation readout for silicon integrated charge qubits. We first design and analyse the double single-electron transistors (DSETs) in which double quantum dots are connected in series with two side gates. We show that the DSETs are sufficiently sensitive to distinguish all the single-charge polarization states on the two charge qubits integrated adjacently. We also show the scalability of the MSETs by extending our analysis to a scaled-up system of serial triple single-electron transistors (TSETs) integrated with triple charge qubits. Finally we fabricate the DSETs with double charge qubits on the silicon-on-insulator substrate and observe hysteresis in the Coulomb oscillations of the tunnel current at temperature of 4.2K, which are attributable to the change of polarisation in the double charge qubits.**

I. Introduction

Semiconductor based Double Quantum Dots (DQDs) are a promising structure to use as a charge qubit [1] in future practical solid state quantum information processing (QIP) devices. Compared with the device formed by using GaAs:AlGaAs hetero-structures, silicon-based QIP device will have extreme advantages toward a highly-integrated structure with a great help of highly-developed CMOS integration circuits technologies. Coherent operation with decoherence time of up to 200 ns was reported in a single isolated Si based DQDs, which indicates that using silicon material would have an advantage to keep a state in the qubits coherent [2]. Motivated by this work, we have investigated on silicon-based QIP devices where isolated Si DQDs are used as the charge qubit. For realizing downscaled charge qubits and increasing decoherence time of the qubits further, we have demonstrated integration of double nanocrystalline silicon quantum dots grown by VHF plasma process in a bottom-up manner with a readout and operation gate electrodes fabricated on the silicon-on-insulator (SOI) substrate in a top-down manner by using electron beam lithography and reactive ion etching technique [3]. Toward the scaling up to two-qubits devices, we have proposed a double single-electron transistor (DSET) as a readout [4] and experimentally showed a clearly-defined hexagon pattern in its Coulomb oscillation characteristics [5]. In this paper we numerically study sensitivity of the DSETs to single-charge polarisation in double qubits adjacent to the DSETs. We also discuss a scaled-up system of triple single electron transistors (TSETs) integrating with triple qubits. Finally we report on experimental observation of hysteresis which might be due to the change of polarisation in double charge qubits system.

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II. Method of Simulation Study

Our novel serially-connected multiple single-electron transistors (MSETs) were designed and analysed in the following manner. First we designed the three-dimensional structures including qubits, readouts, and multiple gate electrodes. Three-dimensional (3D) capacitance analysis was carried out by using simulator VOLT [6] to estimate capacitance matrices among the DSETs, double qubits, and multiple gates. In this capacitance simulation, potential distributions were calculated by solving 3D Poisson's equations by applying bias voltage of 1 V to the multiple gates, individually. We show the Scanning Electron Microscope (SEM) image of the DSET readout and the multiple gate electrodes (without qubits, Fig. 1(a)) and the 3D potential distribution when the voltage was applied to G1 (Fig. 1(b)). The capacitance matrices were extracted by computing the electric fluxes flowing into the SET islands. Capacitance values regarding the qubits and their control gates were also extracted by this capacitance simulation where two qubits were positioned at the distance of approximately about 190 nm from the adjacent SET islands.

Next we calculated current-voltage characteristics for equivalent circuits of the devices by using simulator CAMSET [7]. In this simulation the electron tunneling rate through tunnel barriers was expressed as in the "Orthodox theory" [8], [9]. Tunneling rates were computed at each step for all possible events and we did not account for the quantization of electronic energy. By substituting the simulated capacitance values into the equivalent circuit, we calculated current-voltage characteristics of MSETs for each individual polarised states of multiple

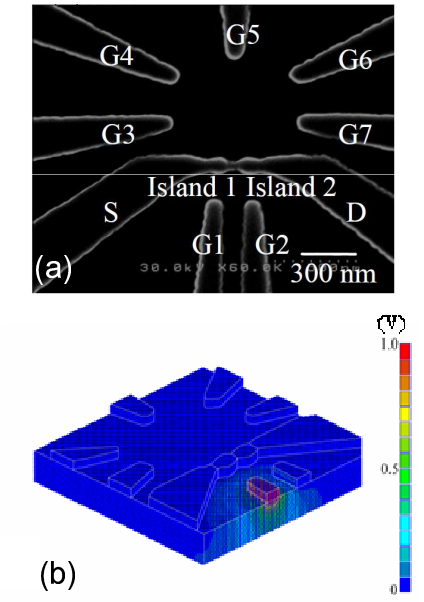

Fig. 1. (a)SEM image of the DSET integrated with operating gate electrodes without qubits. (b) The potential distributions of the DSET on the condition of V_{G1}= 1 V and the other electrodes grounded regarding.

qubits. We compared results of various polarised state with each other and discussed sensitivities of MSETs to single charge polarisations in qubits. We confirmed that calculated current-voltage characteristics of the DSETs were well agreed with the experimental results reported in ref. [4].

III. Simulation Results of Multiple Single Electron Transistor

Figure 2(a) shows schematic top view of the double qubits device with the DSET readout. The corresponding equivalent circuit is shown in Fig. 2(b). Although cross-capacitances are not shown for clarity in the figure, but are included in the simulation. In Fig. 2(c), we show a calculated contour plot of I_D of the DSET as a function of V_{G1}, and V_{G2} at the source-drain bias V_D of 500 μV for the state in which Both of Qubit L and Qubit R have no polarisation(State C in Fig. 2(d)). I_D-V_{G2} characteristic at V_{G1}= 1.95 V, the trace along with the line shown in Fig. 2(c), is plotted in Fig. 2(e) together with the results calculated for the states which has different polarisations (See Fig. 2(d) in detail). Clear shifts are identified for four individual states in which even only single charge was transferred in each individual qubit. More quantitatively, the results show the current difference of the order of several tens pA among four different configurations over the maximum DSETs current of around 0.5 nA. Such current difference is certainly measurable experimentally as demonstrated in Ref. [2]. If we choose the sense bias V_{sen1}= 2.96 V, we can distinguish state A or B from states C and D, while states C and D can be distinguished at V_{sen2} = 3.04 V. By using the DSET readout, therefore, we can clearly identified four different single-charge polarised states in the double qubits system.

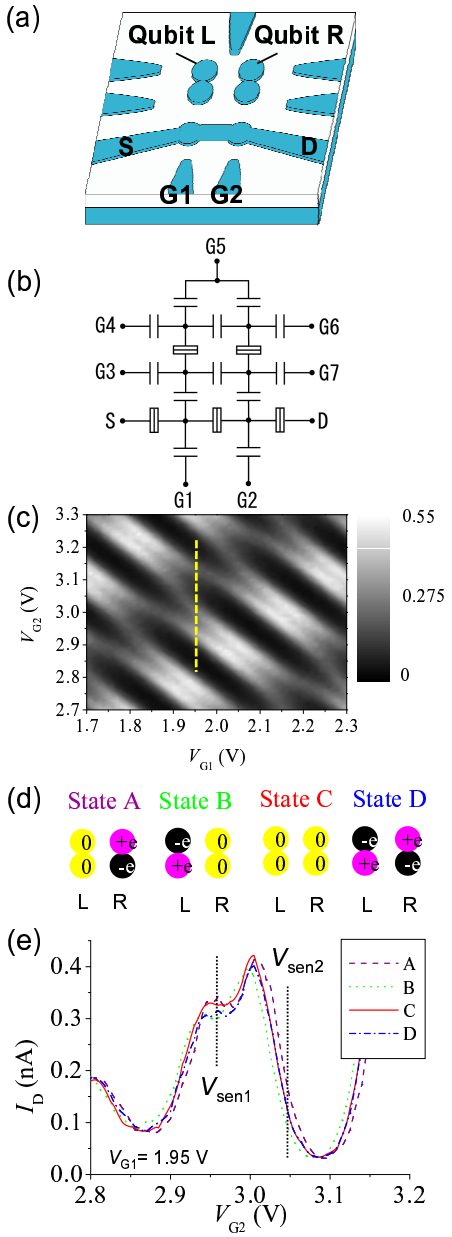

Fig. 2. (a) Schematic top view of the device with the DSET as a readout. (b) Equivalent circuit. (c) Contour plot of the simulated I_D as a function of V_{G1} and V_{G2} with V_D = 500 μV. (d) Schematics of possible single-charge polarised states on double qubits. (e) I_D-V_{G2} characteristics for four different polarised states at V_{G1}= 1.95 V.

We extend our analysis to the scaled-up system of the TSET which is schematically shown in Fig. 3(a). An equivalent circuit we used for TSETs is shown in Fig. 3(b). The contour plot of I_D calculated for the TSETs as a function of V_{G1} and V_{G2} with V_D = 500 μV and V_{G3}= 0 V is more complicated than than that of the DSET as is shown in Fig. 3(c). This is the results for State F in Fig. 3(d) where only the central qubit, Qubit C is polarised downward and the rests have no polarisation. We show in Fig. 3(e) I_D-V_{G2} characteristics with V_D= 500 μV, V_{G1} = 1.0 V and V_{G3} = 0 V for the three single-charge polarized configurations shown in Fig. 3(d), which

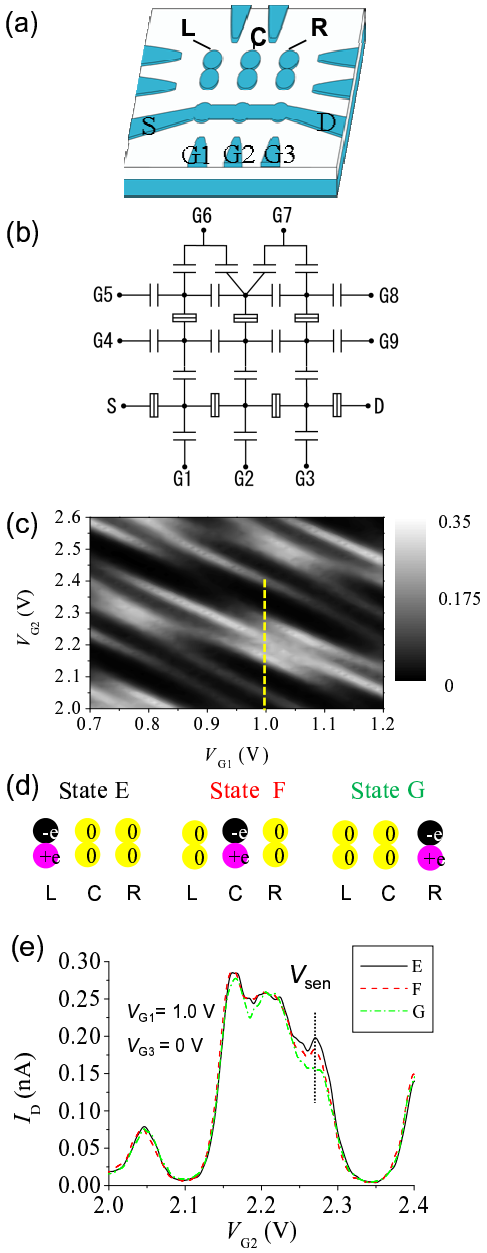

Fig. 3. (a) Schematic top view of the device with the TSET as a readout. (b) Equivalent circuit. (c) Contour plot of the simulated I_D as a function of V_{G1} and V_{G2} with V_D= 500 μV. (d) Schematics of three typical polarised states on triple qubits. (e) I_D-V_{G2} characteristics for three different polarised states at V_{G1}= 1.0 V and V_{G3}= 0 V.

are relatively difficult to be distinguished one another. The magnitude of the change in the peak currents is detectable, especially at V_{sen} = 2.27 V and the ratios of the peak current changes to the overall current level are similar to those obtained for the DSET.

In general, the dependence of tunnel currents on multiple gate voltages for our MSETs reflects the charge stability diagram for the multiple charging islands. As seen both for DSETs and TSETs, the single-charge polarization on the multiple qubits results in the shift of the entire current - voltage

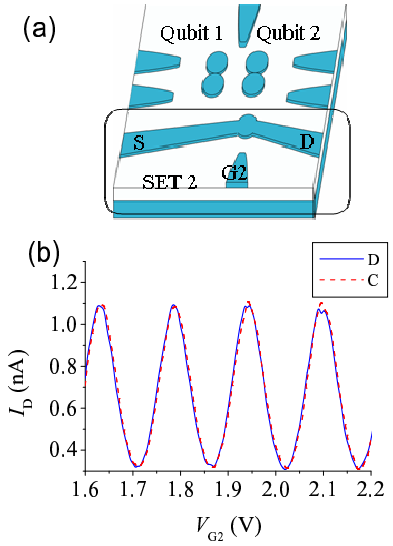

Fig. 4. ((a): Schematic top view of a single-SET (conventional SET) with two qubits, (b) I_D-V_{G2} characteristics with V_D= 500 μV.

curve in a certain direction in the multi-dimensional current - voltage space. Rich domain structures seen for the current - voltages characteristics allow us to detect such current shifts in any directions. The characteristics for the DSETs and TSETs are indeed suited for detecting the double and triple charge qubits. If we detected the triple charge qubits by using the DSETs, we would certainly lose some information due to reduction of dimensionality. Here we show the results for the double charge qubits with a single SET readout (Fig. 4). As distances of two qubits relative to the charging island cannot differ a lot for maintaining good sensitivity, the state D and C shown in Fig. 2(d) are hardly discriminated. This issue could not be solved even if another single-SET is introduced while our DSETs can distinguish them clearly. It should be noted that the advantage of the MSETs is quite universal and not affected by the existence of any cross-capacitances. Furthermore, it will also be increasingly difficult to locate individual single-SETs close to multiple qubits in terms of their physical layout. Our method to detect multiple qubits by using the MSETs structure may avoid the serious delay due to the multiple combination of Controlled Not (CNOT) gate in quantum computation [10].

IV. Observation of Hysteresis

Based on the design simulation, we fabricated devices in which double qubits and the DSET were integrated together. The devices were fabricated on the SOI substrate. Initially, SOI layer thickness and buried oxide (BOX) layer thickness were 100 nm and 200 nm respectively. Phosphors at concentration of 10^{19} cm^{-3} were doped into SOI layer. Repeated thermal oxidation and wet etching process was carried out to reduce the SOI thickness to 40 nm. Negative resist RD-2000N with thickness of 60 nm was coated for electron-beam (EB) direct writing. Two islands connected in series, two SET-gates (G1 and G2) and four qubit control gates (G3-G6) were patterned

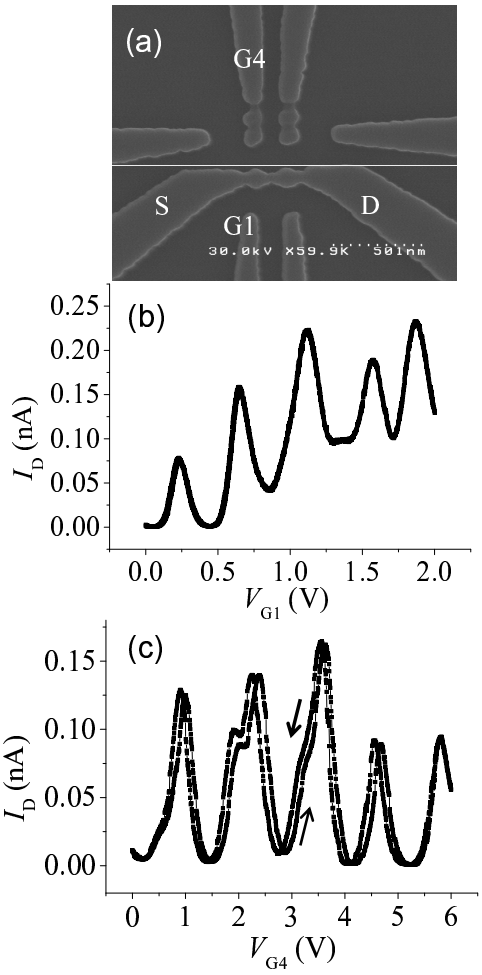

Fig. 5. (a) SEM image of the device in which the DSET readout was integrated with double qubits and operational gates (b) I_D-V_{G1} characteristics with V_D = 5 mV. (c) I_D-V_{G4} characteristics with V_D= 5 mV.

using JBX-5FE made by JEOL and electron cyclotron resonance RIE (ECR-RIE). Figure 5(a) shows the SEM image of the fabricated device. When we swept one of the SET-gate V_{G1}, clear Coulomb oscillation and no hysteresis were observed at T = 4.2 K as shown in Fig. 5(b). In contrast, we observed very clear hysteresis and Coulomb oscillation in Fig. 5(c) by varying the qubit control gate, V_{G4}. We also found several discontinuous steps in I_D-V_{G4} characteristics, which might be due to charge transfer in the qubit. It should be noted that we observed neither hystereses nor discontinuous steps in I_D-V_{G4} characteristics when no qubits were placed between G4 and the islands in the DSETs. The results strongly suggest that the change of charge states in the double qubits can be detected by the DSET.

V. Conclusion

We discussed the DSETs to detect single-charge polarisation on a pair of qubits independently in numerical calculation. Furthermore, we discussed the scaled-up TSETs for integrating with three qubits system. We found out by using the DSETs measured electrical characteristics and the equivalent model that single-charge configurations on a pair of qubits could be distinguished with the DSETs. The TSETs simulation exhibits significant potential for the scaling-up to MSETs. We finally showed the first experimental results on the electrical readout characteristics for the DSETs by comparing the DSETs with and without charge qubits. We found that hysteresis in the Coulomb current oscillations was remarkable only for the DSET with the double charge qubits and there likely to show the change of their charge polarisation.

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