Suspended Gate Silicon Nanodot Memory

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***Abstract*— This paper proposes a new non-volatile semiconductor memory which features a suspended gate integrated with silicon nanocrystals dots as a floating gate and the MOSFET as a readout. Performing three-dimensional finite element simulations combined with an analytical plate-capacitor model, we clarify the pull-in/pull-out operation of the suspended gate. We also show the dependence of the hysteresis cycle characteristics on material and structural parameters.**

I. Introduction

Flash memory has driven the market of non-volatile semiconductor memories since it was invented more than 20 years ago. However, it is getting increasingly difficult to continue downscaling the device dimensions as the tunnel oxide thickness cannot be reduced to less than 6-7 nm [1]. One of the crucial issues for the scaled Flash memory is the leakage current caused by the defect states in the tunnel oxide, after repeating the programming/erasing (P/E) cycles. To overcome this issue an alternative structure was proposed [2]–[4], which introduces silicon nanocrystal (Si-nc) dots as a floating gate (FG). In the silicon nanocrystal memory, only electrons stored in the Si-nc dots adjacent to the leakage path may escape, the leakage current is supposed to decrease to some extent. However, this issue is not solved completely as far as the tunnel oxide is used in common for the P/E operations and for data storage.

In this paper, we propose a new suspended-gate silicon nanodot memory (SGSNM) to overcome the above mentioned issue. Our memory features hybrid co-integration of a nanoelectromechanical (NEM) gate electrode with the silicon nanodots FG on the MOSFET channel. The NEM gate is pulled-in onto the FG only for the P/E operation and otherwise kept separate from the FG. This enables us to shut out the leakage current thanks to the air gap and to realize long data retention as well as fast P/E operation.

II. Suspended Gate Silicon Nanodots Memory

Figure 1 shows a schematic diagram of the proposed SGSNM. A suspended gate (SG) [5]–[7] is placed above the Si-nc dots FG and MOSFET with a finite air gap. The Si-nc dots FG is sandwiched between the lower and upper oxide layer, and the lower gate oxide is designed to be thicker than the upper gate oxide. Such device structure may be fabricated in the following method. After the thermal gate oxide is formed on the Si substrate, the Si-nc dots are deposited by using the VHF plasma CVD technique [4]. The upper thin gate oxide is then deposited, and a sacrificial layer of amorphous silicon (α-Si) is then deposited. Finally, a thin gate metal is deposited over the stacked layers. After patterning the top gate by using electron beam lithography, the α-Si sacrifice layer is selectively etched out, and the air gap is formed between the SG and the FG layer.

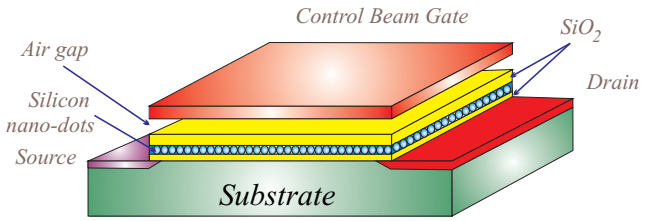

Fig. 1. A schematic diagram of a suspended gate silicon nanodot memory (SGSNM).

Our SGSNM uses a dynamic motion of the SG for the P/E operations. When a negative voltage is applied to the SG, it bends downwards and finally reaches the upper gate oxide surface. Electrons are then injected into the Si-nc dots via the upper gate oxide. By increasing the voltage back to zero, the SG is pulled out and returns to flat. While the electrons are stored in the FG, the SG is kept separate from the FG with an air gap. Figure 2 shows the sequence of the SG mechanical motions for the programming operation.

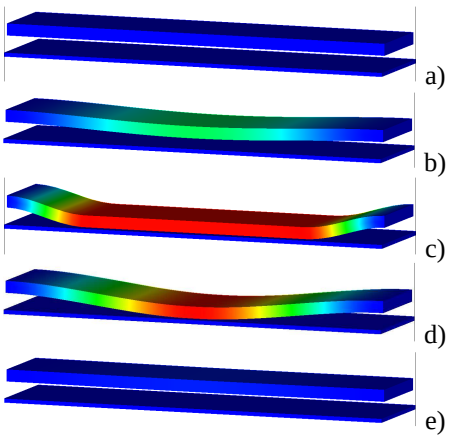

Fig. 2. 3D sequence obtained by conducting a simulation for an aluminium suspended gate and gate oxide layer.

By applying a negative voltage to the SG, it initially bends slowly downwards (Fig. 2(b)), but it is suddenly pulled in at

a certain voltage. By further decreasing the gate voltage, the contact area of the SG onto the FG increases (Fig. 2(c)). At this point electrons are injected from the SG into the Si-nc dots through the upper gate oxide layer by tunnelling. When the SG voltage is increased, the SG is pulled out suddenly at a certain voltage (Fig. 2(d)). It should be noted that the pulled-out voltage generally differs from the pull-in voltage because of the finite stiction between the metal SG and the upper gate oxide.

For erasing operation, a positive voltage is applied to the SG. Although the bias polarity and the direction of the electric field is reversed between the SG and the substrate, the pull-in / pull-out sequences of the SG are the same as those for the above mentioned programming process, except that electrons are extracted from the Si-nc dots back to the SG when the SG is pulled-in. In order to design the SGSNM, one of the key issues is to reduce the pull-in (and also pull-out) voltage as it determines the P/E voltages, which depend on several structural and material parameters. We therefore derive analytical formulae of the pull-in / pull-out voltages in the following.

The pull-in voltage obviously depends on the SG parameters such as Youngs modulus, Poisson's ratio, stiffness, thickness and area and a dielectric constant (κ) of the gate oxide. There are several analytical models to derive the pull-in voltage: some are quite complex and require numerical computation, and others are simpler, such as a parallel-plate capacitor model depicted in Fig. 3.

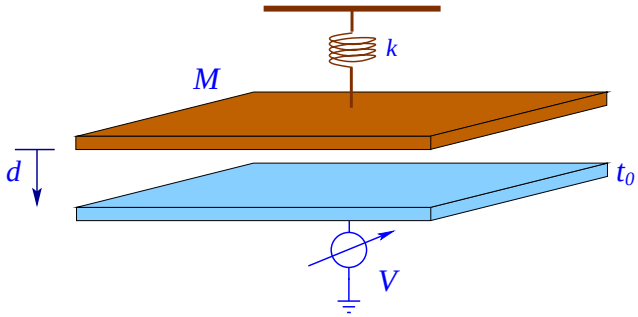

Fig. 3. A plate capacitor model.

For this simple model the following equation can easily be derived for the pull-in voltage:

$$V_{pull-in} = \sqrt{\frac{8kd^3}{27\epsilon_0\kappa A}} \tag{1}$$

where k is the spring constant, ϵ_0 is the free space permittivity, A is the overlap area, d is the initial air gap between the plates.

By using the plate-capacitor model depicted in Fig. 4, the pull-out voltage can also be calculated by taking account of the stiction, k, oxide layer thickness, and SG parameters.

$$V_{pull-out} = \sqrt{\frac{2kdt_{ox}^2}{\epsilon_0\kappa A}} \tag{2}$$

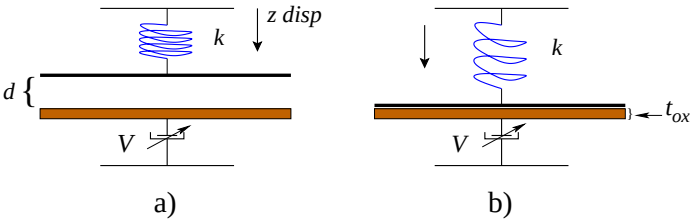

Fig. 4. A plate capacitor model to calculate Pull-out operation.

The derived two equations enable to estimate the magnitude of the hysteresis associated with the pull-in / pull-out phenomena.

III. Numerical Simulations Method

In order to analyze the full pull-in and pull-out operations of the SG, we need to perform three-dimensional FEM simulation. There are various commercial packages of the finite element method (FEM) simulators: some of them are developed for general purposes, and others are designed to simulate specific phenomena. In the present study we adopted CoventorWare dedicated to MEMS analysis and also more general-purpose Comsol package combined with the MEMS module. Table 1 summarizes the materials used for the SG and associated material properties used in the present work.

TABLE I

Parameters used to model the structure.

Material	Young's Modulus GPa	Dielectric	Dimensions nm
Aluminium	77		
Copper	128		
Poly-Si	160		1000×250
Silicon	169		
SiO_2	73	3.8	
Si_3N_4	222	7	

Those materials are commonly used in the CMOS and MEMS fabrication processes. Table 2 shows the thickness of the individual layers used for the SG, the air gap, the gate oxide and the Si substrate. Note that the Si-nc dots FG layer is not taken into consideration in the present simulation for simplicity. Figure 5 shows an example of the 3D model structures visualized with CoventorWare.

TABLE II

Device materials

Material	Thickness
SG	30 nm
Air Gap	30 nm
gate oxide	10 nm
Si	100nm

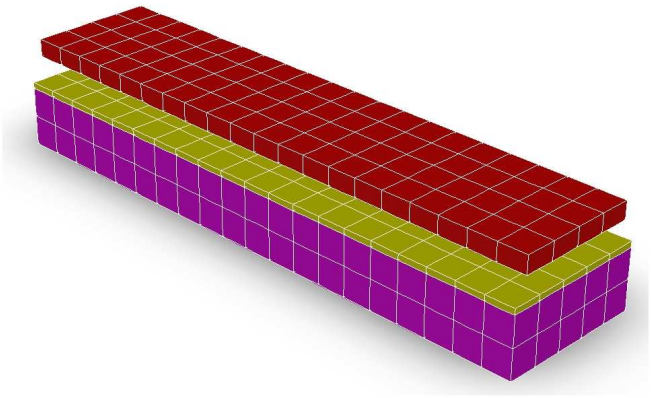

Fig. 5. A 3D solid model of the SG structure on the MOS substrate.

IV. Numerical Analysis of Pull-in/Pull-out Characteristics for SG.

First, in order to find the dependence of the material parameters on the pull-in voltage, several numerical simulations were performed. Figure 6 shows the pull-in characteristics simulated for aluminium, copper and poly- Si as a suspended gate material and silicon dioxide (SiO_2) as a dielectric material.

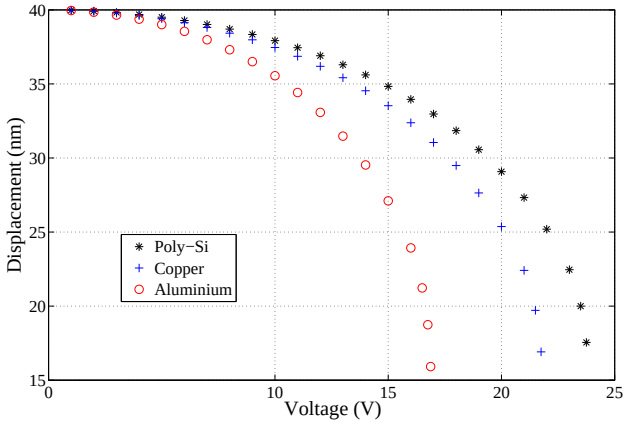

Fig. 6. Comparison of the pull-in voltages obtained for three SG materials.

According to the simulation, the relation between aluminium and SiO_2 generates the pull-in effect at 17 V @ 15.3 nm. For copper and SiO_2, the pull-in effect appears at 21 V @ 15.7 nm and for poly-Si this appears at 24.2 V @ 16.3 nm. The different pull-in voltages are primarily determined by the stiffness of the individual materials.

Next we studied the effects of the gate oxide materials, SiO_2 (κ = 3.8) and Si_3N_4 (κ = 7), on the full pull-in / pull-out characteristics. Figure 7 shows the results obtained by sweeping the gate voltage from zero to 25 V and then back to zero. The hysteresis cycle caused by the stiction between the SG and the gate oxide is clearly seen for those simulations. While the pull- in phenomenon occurs at virtually the same voltage of 17 V, there is a remarkable difference for the pull-out voltages. The difference between pull-in/pull-out windows obtained for the SiO_2 and Si_3N_4 insulators is approximately 2 V. Figure 8 compares the full pull-in / pull-out characteristics simulated for three different SG materials with the same SiO_2 gate insulator. Three SG structures show different hysteresis cycles: copper has a hysteresis window of 11.5 V and poly-Si shows that of 12 V.

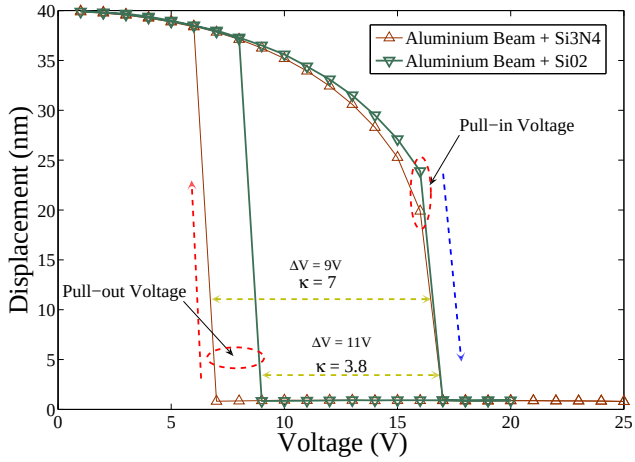

Fig. 7. Comparison of the hysteresis cycles for two SG materials.

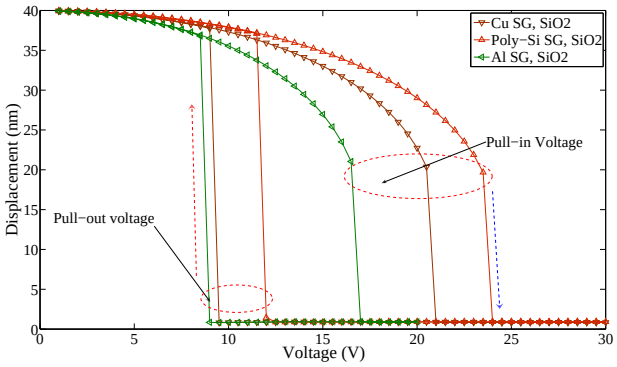

Fig. 8. A comparison of the hysteresis cycles for three different SG materials.

V. Discussion on Full Nonvolatile Memory Operation of SGSNM

As discussed in Section II, negative and positive voltages are applied to the SG for performing the programming and erasing processes, individually. Figure 9(a) shows the pull-in / pull-out characteristics simulated by sweeping the gate voltage in both bias directions. We also show a sketch of the current-voltage characteristics associated with the SG motions (Fig. 9(b)). When the SG pull-in occurs with the negative gate voltage, electrons are injected into the FG and the inversion layer is formed in the MOSFET, resulting in an increase in the current. As the gate voltage is increased, the high current state (ON state) is maintained even after the SG is pulled out until the SG is pulled in with the positive gate voltage and the electrons are extracted from the FG. After that the low current

state (OFF state) is kept until the electrons are injected again with the negative pull-in voltage is applied to the SG.

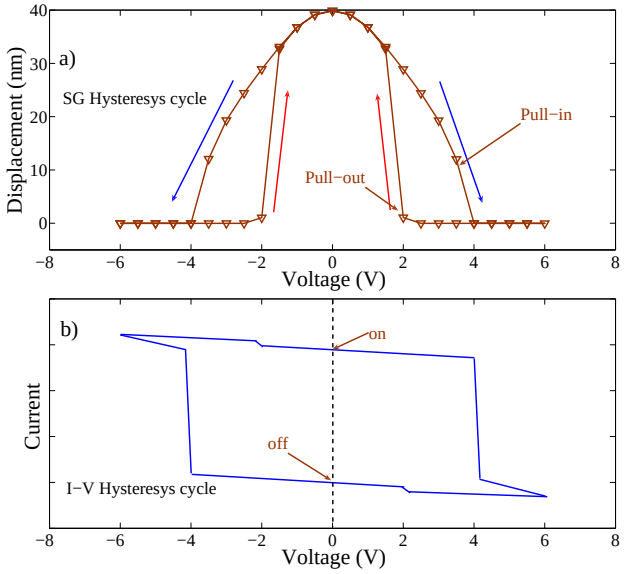

Fig. 9. A full programming/erasing cycle for the SGSNM. When a positive and negative voltage are applied to the SG, it shows the double hysteresis curve as (a) shows. (b) shows a schematic I-V curve assosiated with the SG hysteresis in (a).

It should be noted that the characteristics in Fig. 9(a) look virtually symmetric, indicating the same absolute values of the P/E voltages. This is true as far as the change in the potential caused by the charge stored on the FG is relatively small. It is however expected that the entire curve may shift by a finite voltage once electrons are injected into the FG. For analyzing this phenomenon quantitatively, we need to simulate the SG and the FG with MOSFET simultaneously.

A hybrid simulation is in progress by using the COMSOL with the MEMS module taking account of the entire memory device structure: a preliminary result is shown in Fig. 10.

In such hybrid simulation both the electromechanical equations for the SG and the carrier transport equation for the MOSFET are solved in a synchronized manner. Figure 10 shows the SG just before the pull-in operation and the associated MOS inversion layer formation. Further details of the hybrid simulation will be presented at the conference as well as more numerical results.

VI. Conclusion

A new suspended-gate silicon nanodot memory (SGSNM) was proposed by combining silicon nanocrystal materials and NEMS technology. The SGSNM can be manufactured within the conventional silicon technology and may achieve fast P/E operation as well as long data retention time without introducing any exotic materials. Performing 3D numerical simulations the impacts of materials and structures of the suspended gate and oxide layer were investigated. An analytical model was also presented for the pull-in/pull- out voltages.

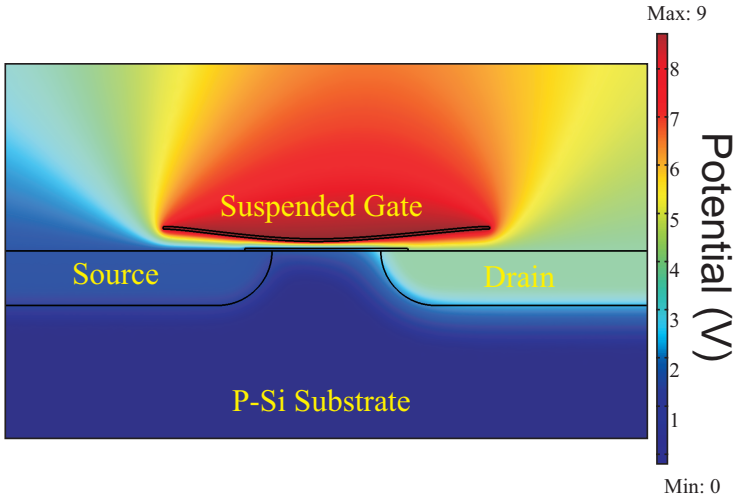

Fig. 10. Potential distribution obtained for the SG with a MOSFET with the source-to-drain voltage of 3 V and the SG voltage of 9 V.

Acknowledgment

The authors wish to thank Prof. S. Oda and his laboratory members at Tokyo Institute of Technology for valuable discussions. One of the authors (M.A.Garcia-Ramirez) would like to thank the Consejo Nacional de Ciencia y Tecnologia (CONACyT), Estados Unidos Mexicanos (Mexico). Under the scholarship 181944 in the UK.

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