Hybrid Silicon Nanotechnologies for *More-than-Moore* and *Beyond-CMOS* Domains

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The dawn of the silicon nanoelectronics was seen when the physical gate length of high-performance of CMOS got shorter than 100 nm in 1999 after continuous down-scaling over the last few decades under Moore's Law. The latest *International Technology Roadmap for Semiconductors* [1] predicts that such top-down approach will be pursued further in the nanoelectronics regime - known as 'More Moore' approach - and the CMOS gate length will reach 9 nm in 2016. However, maintaining such aggressive top-down trend is getting increasingly difficult both technologically and economically because a number of new "technology boosters" should be introduced for the next few years. Under these circumstances present nanoelectronics research is characterized by the migration of research from pure down-scaling to the quest for new functionalities beyond CMOS and hybridization of CMOS and other heterogeneous technologies. Nanoelectronics research may therefore be divided into three main research domains: 'More Moore', '*More than Moore*' and '*Beyond CMOS*' as shown in Fig. 1. 'Beyond CMOS' domain covers novel device principles which are not based on the CMOS operation and circuit architecture, which may include, spin-based memory and logic devices, quantum information processing (QIP), and other advanced infromation processing devices by using inorganic/organic 'bottom-up' materials such as carbon nanotubes and organic molecules. On the other hand, the 'More than Moore' domain deals with hybrid co- integration of conventional Si CMOS technology and various other technologies such as micro- and nano-electromechanical systems (MEMS/NEMS), nanophotonic devices, sensor devices and RF devices in order to meet certain needs and specifications of advanced system applications. Massive efforts are therefore made now on studying emerging research materials and devices for exploring the new 'More than Moore' and 'Beyond CMOS' domains. In this paper we present our recent attempts to introduce novel silicon nanotechnologies for developing advanced information devices in these two new nanoelecrtonics domains.

For the 'More than Moore' domain, we discuss co-integration of nanoelectromechanical (NEM) structures with conventional silicon devices for advanced memory, logic and sensing applications. Two types of novel high-speed and nonvolatile NEM memory are presented to go beyond conventional Flash memory. The first one features a buckled SiO_2 floating gate (FG) with embedded nanocrystalline Si dots as single-electron storage (see Fig. 2) [2],[3]. The FG is switched electrically between its upward- and downward-bent stable forms with applied gate electric fields, and the beam states are detected via a change in the drain current of the MOSFET underneath. The second one features a suspended gate (SG) over the Si nanodot FG (see Fig. 3). The SG is pulled in onto the FG only when we programme and erase the information and otherwise kept pulled out. In both NEM memories, the stored electrons are secured by shutting off leakage currents with the air gap. We then present hybrid NEMS-SET (single-electron transistor) logic devices [4]. In the SG-SET structures, a suspended gate integrated onto the SETs works as a binary capacitive switch and results in unique device characteristics which cannot be realized with

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conventional SETs. The SG-SETs, therefore, enable to switch the period of Coulomb current oscillation of SETs, and this may be utilized for signal encoding in the periodicity realizing the offset charge independent SET logic. We also discuss new operating principles of NEMSETs (see Fig. 4) in which a suspension quantum dot provides an ideal 'laboratory' to study the interactions between single-electrons and nanophonons confined in the quantum dot cavity, free from the influences of the substrate [5].

For the 'Beyond CMOS' domain, we discuss the recent progress of silicon-based quantum information processing (QIP) technologies in terms of hybrid nanofabrication technologies for integrating single and multiple charge qubits with a single-charge detector. Among a number of potential candidates as a physical implementation of solid-state quantm bits (qubits), we adopt the electron charge states in Si double quantum dots (DQDs) for various reasons such as inherent scalability, existence of a variety of initialization and readout methods, and compatibility with conventional silicon technologies. By using both top-down and bottom-up nanofabrication techniques, we fabricate experimental double qubit structures integrated with a novel single-charge detector consisting of series-connected double SETs (DSETs) (See Fig. 5) [6]. The DSETs enable a small footprint and ensure that the qubit-readout spacing can be downscaled together with the qubit-qubit spacing. We show that four different single-charge polarization configurations on the double qubits are detected as remarkable shifts of the Coulomb oscillation current-contour patterns of the DSETs [7].

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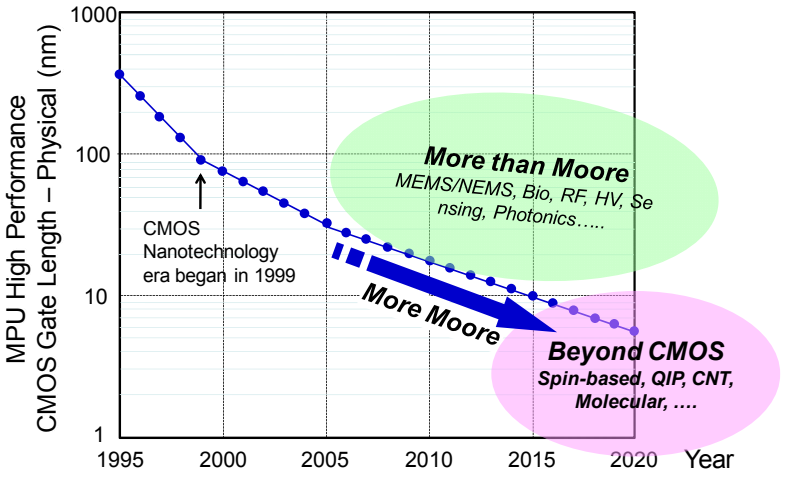

Fig. 1 'More than Moore' and 'Beyond CMOS' domains in silicon nanoelectronics.

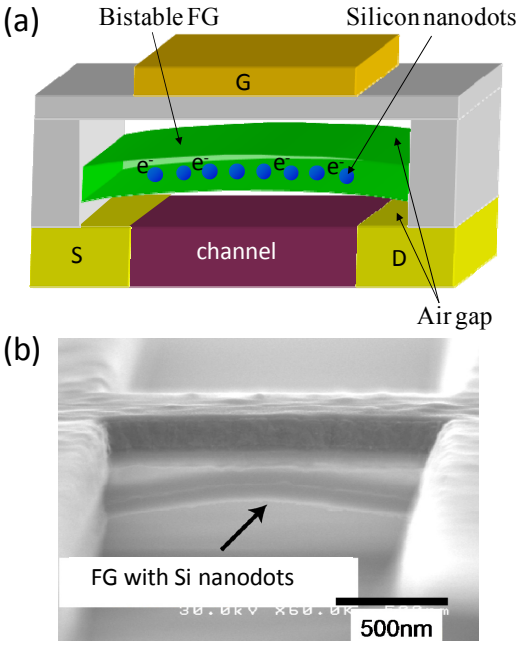

Fig. 2 Schematics of (a) a NEM memory with a mechanically-bistable FG and (b) a suspended-gate nanodot memory.

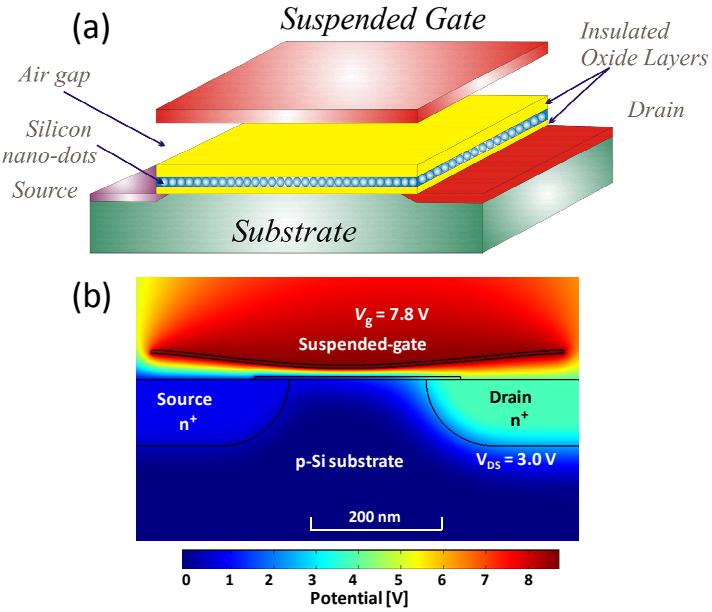

Fig. 3 (a) A prototype NEM memory and (b) Electrostatic potential distribution calculated for a SG nanodot memory under pull-in operation.

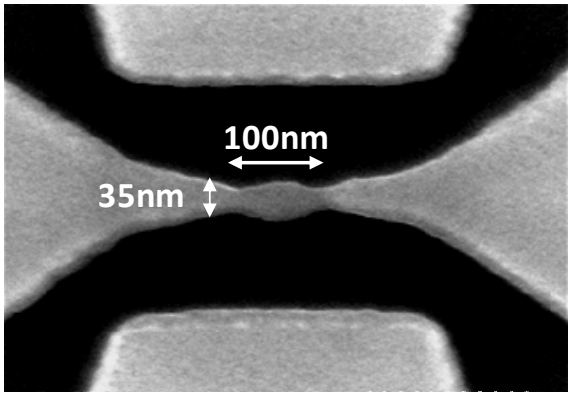

Fig. 4 A NEMSET with a suspension QD.

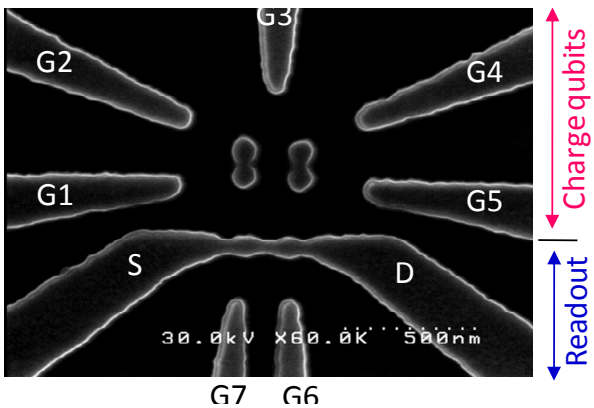

Fig. 5 Double charge qubits integrated with a DSET readout.