Silicon radio frequency single-electron transistors operating at above 4.2 K

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1. Introduction

Silicon detectors are widely used as tracking detectors in high-energy particle physics, astronomy, and medical fields. In X-ray imaging, it is also used in crystallography, and medical imaging and mechanical engineering for alignment. They have also found applications in detection of photons in medicine and astrophysics [1]. But, charge sensitivity of the readout electronics often limits the sensitivity of these detectors. Requirement of the readout electronics are high charge sensitivity, wide bandwidth, and high temperature operation. Other requirements are, the read out electronics should not suffer from charge offset problem, and should be stable against long term operation. High sensitivity and wide bandwidth can be realized using the demonstrated Radio Frequency Single Electron Transistor (RF-SET) based on Al SET [2]. Other conditions have already been realized by the SOI based Silicon SET [3-5]. So, silicon RF-SET will be the only solution to meet all these requirements to realize the high sensitive silicon detector readout electronics.

Operation of the RF-SET based on 2-DEG in intrinsic silicon is reported at 100 mK [6]. Main difficulty in realizing silicon RF-SET is high resistance of the silicon SET, which degrades the response severely [7]. In this paper, we report the successful operation of RF-SET above 4.2 K based on laterally defined single dot in heavily doped SOI silicon channel. Silicon RF-SET will also be used in a single-electron electrometer and, more widely, as a detector for charge qubits, single electron dynamics, millimeter-wave single-photons, and quantum dynamics of nano-mechanical resonators. The high temperature silicon RF-SET will make it possible to realize high sensitivity pixel detectors that will benefit many other research applications as well.

2. Fabrication Process

We used an SOI wafer with a 40-nm-thick Si layer (P-doped of $\sim 10^{19}$ cm^{-3}) and a 200-nm-thick buried-oxide (BOX) layer. Lateral constrictions in the channel were patterned by using the electron beam lithography and subsequent reactive ion etching. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of SOI. An SEM image of the typical fabricated device structure is shown in Fig. 1. The bright and dark regions indicate SOI and BOX layers, respectively. Two gates in the channel constriction regions can be used to control the potential distribution across the channel. In the reported measurement results, this operation was not carried out.

3. RF-SET measurement setup

Schematic of the RF measurement setup is shown in Fig. 2. An RF carrier signal was applied to the drain of the SET through the directional coupler and the reflected signal was amplified by the low noise amplifier at low temperature. Low noise amplifier had a 17 K noise temperature and 42 dB gain at 77 K. A surface-mount inductor L = 560 nH was used. The parasitic capacitance C_{Pad} of the SET to ground was determined to be ~ 0.5 pF based on the resonant frequency measurement. Electrical transport measurements were performed in a He pumping measurement setup for the temperature of 4.2 K and above. DC measurement of the SET was done through the bias tee.

4. Measurement Results and Discussion

Fig. 3 shows the contour plot of the measured drain current differential conductance as a function of V_{d} and V_{G1}. A virtually uniform oscillation period manifests that a single charging island is responsible for the Coulomb oscillation. The sensitivity of the RF-SET was determined by applying 1 MHz sinusoidal signal of 0.025 e_{rms} amplitude superimposed onto the dc gate voltage, producing amplitude modulation of the carrier signal. Fig. 4(a) shows the resulting amplitude modulation (AM) spectrum with sidebands symmetric about the carrier. The charge sensitivity of the RF-SET is calculated by

$$\delta q = \frac{\Delta Q}{\sqrt{2RBW} \times 10^{\frac{SNR}{20}}},$$

where ΔQ is the value of the gate signal measured in electrons (rms), RBW is the resolution bandwidth used for the spectrum analyzer, and SNR is the signal to noise ratio for the side peak, measured in dB. The best charge sensitivity was found to be 36.6 $\mu e/\sqrt{\mathrm{Hz}}$ at 4.2 K. The dependence of the charge sensitivity on the carrier frequency [Fig. 4(b)] reveals the bandwidth of the resonant circuit of 14 MHz. Fig. 4(c) shows the charge sensitivity as a function of the carrier amplitude at the source, which is consistent with calculated values. Fig. 4(d) shows the gate frequency dependence of the charge sensitivity. These measurements were done at 5 K. Also, RF-SET was successfully operated up to 12.5 K [Fig. 4(e)].

5. Conclusion

We showed the Si-based RF-SETs operating at $T > 4.2$ K for the first time. This clearly indicates that RF-SETs with high sensitivity and wide bandwidth can be realized at liquid nitrogen temperature, which will pave the way for realization of high sensitivity silicon detector and many other sensitive measurements.

References

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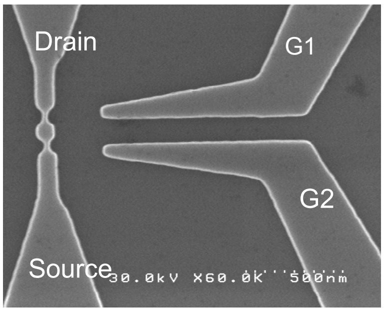

Fig. 1. SEM image of the fabricated silicon SET.

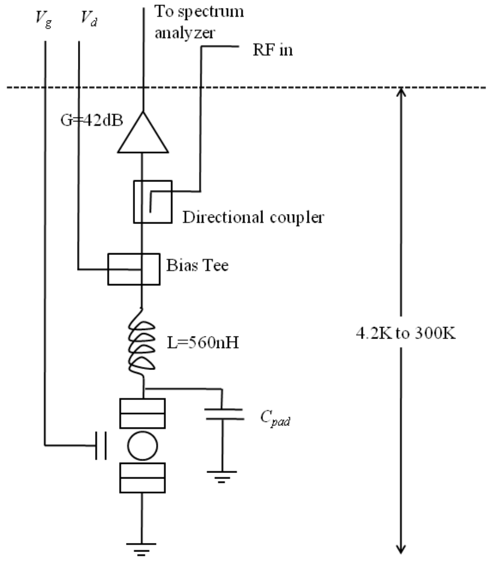

Fig. 2. Schematic of the rf-measurement setup.

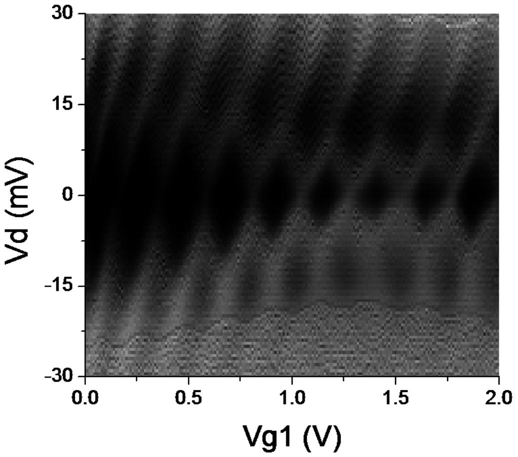

Fig. 3. Differential conductance plot of the SET as a function of V_d and V_{G1} with $V_{G2} = 0$ V at 5 K.

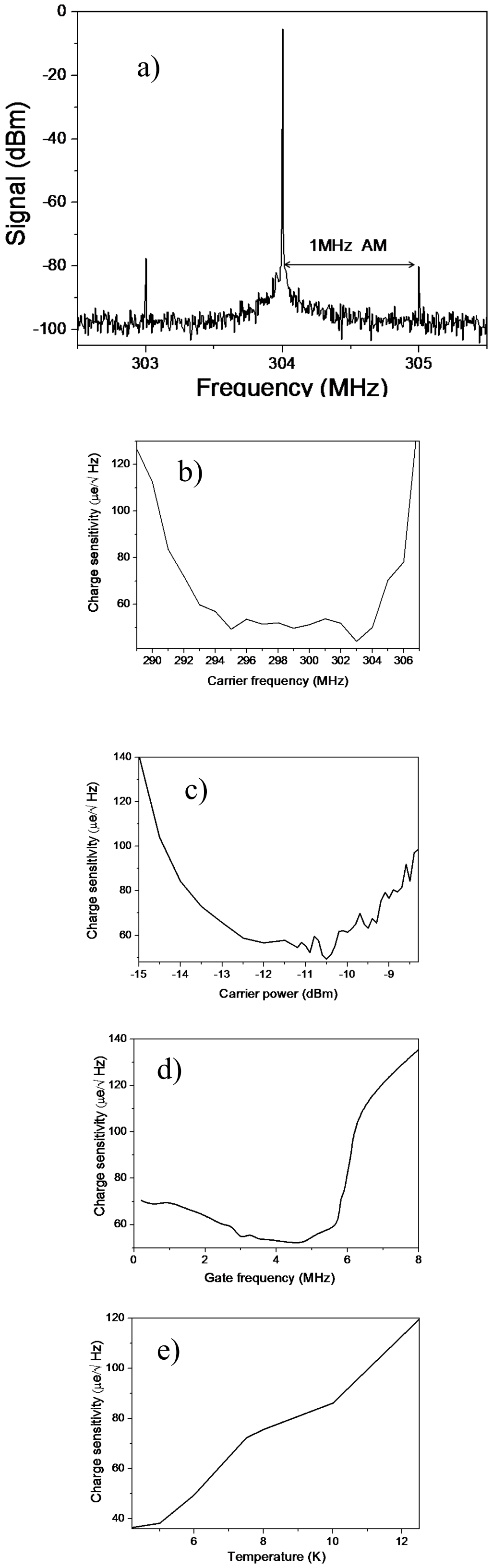

Fig. 4. a) AM response of the silicon RF-SET to 1 MHz gate modulation; charge sensitivity as a function of b) carrier frequency, c) carrier power, d) gate frequency and e) temperature.