Co-integration of Silicon Nanodevices and NEMS for Advanced Information Processing

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Abstract

In this paper we present our recent attempts at developing the advanced information processing devices by integrating nano-electro-mechanical (NEM) structures into conventional silicon nanodevices. Firstly, we show high-speed and nonvolatile NEM memory which features a mechanically-bistable floating gate is integrated onto MOSFETs. Secondly we discuss hybrid systems of single-electron transistors and NEM structures for exploring new switching principles.

1. Introduction

The dawn of the silicon nanoelectronics was seen when the physical gate length of high-performance of CMOS got shorter than 100 nm in 1999 after continuous down-scaling over the last few decades. The latest *International Technology Roadmap for Semiconductors* [1] predicts that such top-down approach will be pursued further in the nanoelectronics regime - known as 'More Moore' approach - and the CMOS gate length will reach 9 nm in 2016. However, maintaining such aggressive top-down trend is getting increasingly difficult both technologically and economically because a number of new "technology boosters" should be introduced for the next few years. Under these circumstances present nanoelectronics research is characterized by the migration of research from pure down-scaling to the quest for new functionalities beyond CMOS and hybridization of CMOS and other heterogeneous technologies. Nanoelectronics research may therefore be divided into three main research domains: 'More Moore', 'More than Moore' and 'Beyond CMOS'. 'Beyond CMOS' domain covers novel device principles which are not based on the CMOS operation and circuit architecture, which may include, spin-based memory and logic devices, quantum information processing and other advanced information processing devices by using inorganic/organic 'bottom-up' materials such as carbon nanotubes and organic molecules. On the other hand, the 'More than Moore' domain deals with hybrid co-integration of conventional Si CMOS technology and various other technologies such as micro- and nano-electromechanical systems (MEMS/NEMS), nanophotonic devices, sensor devices and RF devices in order to meet certain needs and specifications of advanced system applications. In this paper we present our recent attempts of introducing NEMS technology for developing advanced information devices for the emerging research domains.

2. Co-integration of NEM structures and MOSFETs – Fast and nonvolatile NEM memory

It is widely known that microfabrication technologies matured with the silicon VLSI development in the past decades have opened another vast technology area of MEMS/NEMS. It is expected that the MEMS market will grow with the rate of 30 – 40 % per annum and will reach ten billion dollers in 2015. Along with such rapid expansion in MEMS business, there has also been continuous efforts at making the MEMS smaller for raising their operation frequency. For example, the oscillation frequency of over 1 GHz has recently been demonstrated for the 1.1-μm-long SiC based beam [2]. The characteristic lengths (such as the resonator length) of the semiconductor-based MEMS structures reported for the past decade are plotted in Fig. 1: the MEMS technology has entered the sub-μm regime and is now proceeding towards the nanoscale regime.

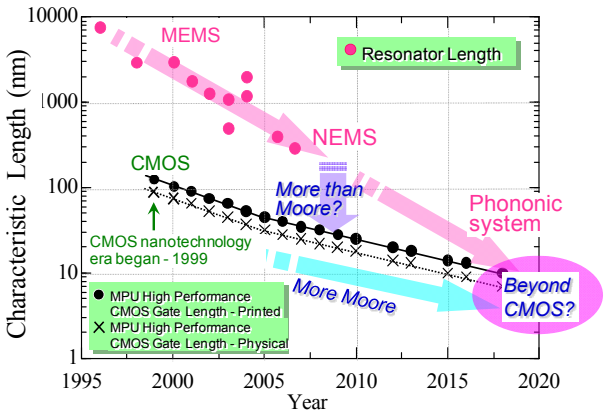

Figure 1 NEMS downscaling trend superposed on the 'More Moore' trend of CMOS from ITRS.

The appearance of high-speed NEMS was tempting enough for us to consider co-integration of the NEMS components into the conventional silicon electron devices for giving extended performance and exploring novel functionalities. As the first attempt, we proposed a new nonvolatile NEM memory in which a mechanically bistable floating gate (FG) is integrated onto the conventional MOSFET (Fig. 2(a)) [3][4]. The FG consists of SiO_2 matrix with the array of the nanocrystalline (nc-) Si dots as single-electron storage and has two structurally-stable states – upward- or downward-bent states. The FG may be flip-flopped via the gate electric field, and its structural states are sensed via a change in the drain current of the MOSFET underneath. Owing to its operating principle, the NEMS memory possesses various tangible advantages over the conventional Flash memory. For example, it is seriously non-volatile as programming / erase operation does not use charge tunneling via the gate oxide, and no gate oxide degradation is therefore anticipated. Programming /erase time can be much shorter than Flash memory by making the beam dimensions into the submicron regime.

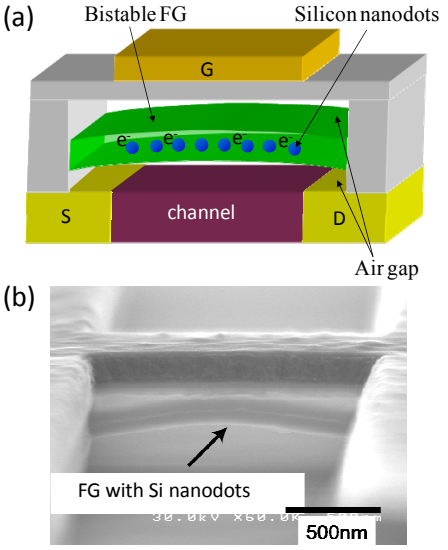

Figure 2 (a) A schematic structure of a nonvolatile NEM memory and (b) a fabricated prototype FG with embedded Si nanodots.

A prototype device structure was fabricated by developing the following process: A 50-nm-thick SiO_2 layer was first formed by oxidizing the surface of a 200-nm-thick SOI. Second, the nc-Si dots of approximately 10 nm in diameter were deposited using the VHF plasma CVD [5] with the areal density of about 5 x 10^{11} cm^{-2}. A 50-nm-thick SiO_2 layer was then deposited by using CVD to sandwich the SiNDs between the double SiO_2 layers. After that a 150-nm-thick amorphous Si layer, a 50-nm-thick SiO_2 layer and a 100-nm-thick Cr layer were deposited sequentially. The control gate was patterned using EB lithography, and the top SiO_2 layer was etched anisotropically. The underneath Si sacrifice layer was then etched out using isotropic dry etching. Figure 2(b) shows the fabricated FG with the embedded nc-Si dot layer. All the fabricated FGs were bent upward by approximately 50 nm. The FGs were buckled as the stress at the SOI / thermal SiO_2 interface was released by removing the sacrificial Si layer. Degree of bending may be altered by changing the ratio of the stress-free CVD-grown SiO_2 thickness to the thermal SiO_2 thickness.

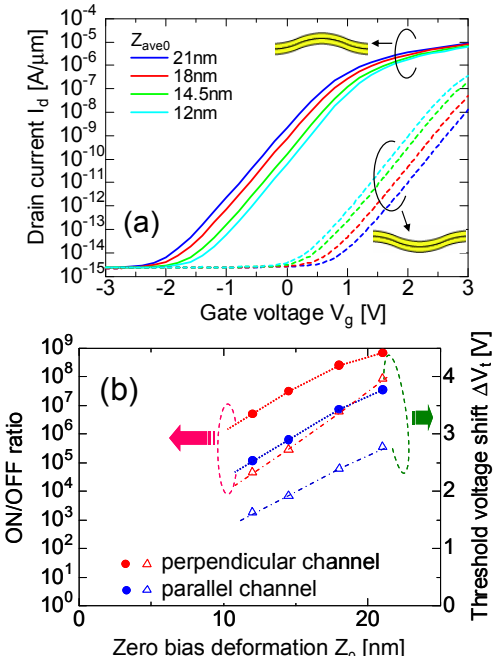

Figure 3 (a) Readout characteristics calculated for various values of initial FG displacement and (b) current ON/OFF ratios and threshold voltage shifts.

The electrical readout characteristics were studied by performing 3D hybrid simulation. One of the key issues for designing the NEMS memory is to meet two requirements of reducing the switching voltage and maintaining the current ON/OFF ratio large enough for readout simultaneously. Overall optimization is therefore needed for the structural and material parameters of not only the FG but also outer cavity. Figure 3 shows I_d-V_g characteristics calculated for the bistable states of the FG with various values of the zero-bias bending Z_0. The results indicate that our NEMS memory may exhibit the ON/OFF ratio as high as 10^5 and the threshold voltage shift ΔV_t of over 2 V. The associated switching voltage is made less than 10 V.

The switching speed of our NEMS memory was also studied by performing transient analysis by taking account of damping phenomena. The simulated results showed that the switching time shorter than 50 nsec is

achieved for the NEMS memory with a 1-µm-long FG while it can further be decreased by optimizing the applied gate voltage.

We have also proposed an alternative NEM memory recently by combining a suspended gate (SG) and the Si nanodot FG embedded in the gate oxide (see Fig. 4(a)). Basic operation of the SG is explained by using a simple model of parallel plates: a movable top plate suspended by using a spring above a fixed bottom plate with a gap of t_0. By increasing a voltage between the plates, the suspended plate starts to move downwards gradually under the influence of the attractive electrostatic force which is in equilibrium with the elastic force of the spring.

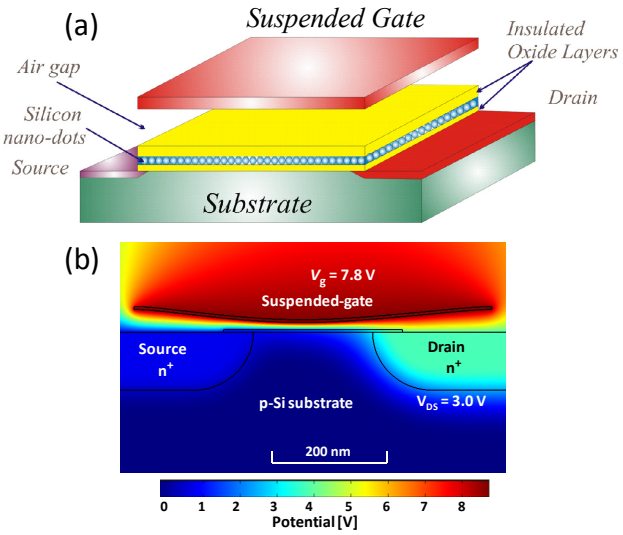

Figure 4 (a) A prototype NEM memory and (b) Electrostatic potential distribution calculated for a SG nanodot memory under pull-in operation.

When the gap between the plates is reduced to about $2/3t_0$, the equilibrium is broken, resulting in the snap of the two plates: the phenomenon called the pull-in effect (Fig. 4(b)).

The pull-in voltage is approximately given by the following equation

$$V_{pull-in} = \sqrt{\frac{8k}{27\varepsilon_0 S} t_0^3}$$

and is therefore controlled via the spring constant k, the initial gap t_0 and the area S of the SG (see Fig. 5). The SG is then pulled out by decreasing an applied voltage with a finite hysteresis due to stiction of the two plates (see the inset to Fig. 5).

In our new NEM memory such pull-in / pull-out operations of the SG are used for injecting electrons into and for removing electrons from the Si nanodots in the FG through a top tunnel oxide. Namely, a negative pull-in voltage is applied to SG for programming, and a positive pull-in voltage is applied for erasing.

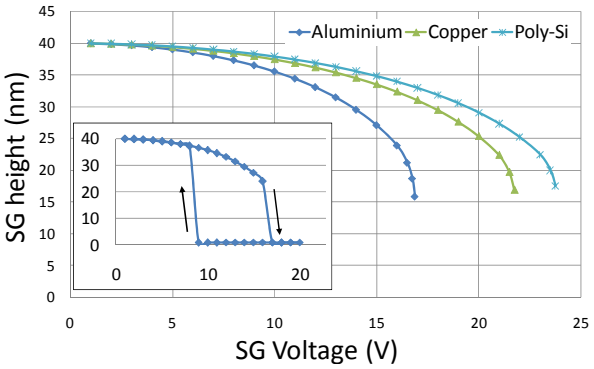

Figure 5 Pull-in characteristics simulated for three different SGs: Aluminum, Copper and Poly-Si. The inset is a full pull-in / pull-out characteristics for Al.

The SG is pulled in onto the FG only when we programme and erase the information and otherwise kept pulled out. Therefore there is no chance of stored electrons leaked out back to the SG in contrast to conventional nanodot memory. The bistable charge states of the FG are detected electrically via the MOSFET in the same manner as the nanodot memory.

Apparently further design optimization is needed for these NEM memories in order for competing with other candidates of emerging nonvolatile RAMs such as MRAM, FRAM and PCRAM. However, it is certainly an advantage for the NEM memories in contrast with the other candidates that it can be manufactured within the conventional Si technologies without introducing any exotic materials.

3. Hybrid NEM – SET systems for exploring new nanoelectromechanical and phoninc properties

Downscaling the structures into a-few-hundred-nanometer regime, we may explore a variety of new hybrid systems of NEMS and Si nanodevices. As one of such novel devices we studied the single-electron transistors (SETs) strongly coupled with NEMS. We hereafter define two types of the SET – NEMS hybrid devices: one is a SG-SET which features a suspended gate is integrated into the SETs and the other one is a NEMSET in which the channel of the SET is formed with an electromechanical resonator (see Fig. 6).

As discussed in Section 2, the pull-in motion of the SG works as a two-state capacitive switch [6]: a low gate capacitance for the pulled-out SG and a high gate capacitance for the pulled-in SG. Thanking to this abrupt change in the gate capacitance, the SG-SET enables to switch the period of Coulomb oscillation between two states with long and short periodicity (Fig. 7).

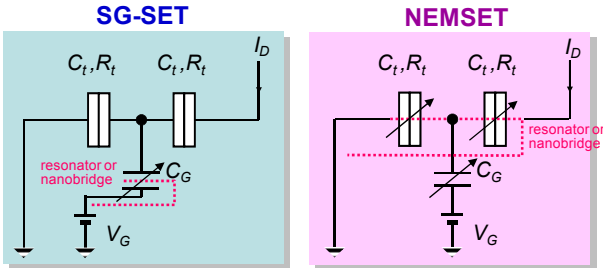

Figure 6 Two types of hybrid system of SET and NEMS: SG-SET (left) and NEMSET (right).

We may use these two different states of periodicity as binary data rather than voltage or current. This approach may solve the offset charge issue which is an inherent drawback of the SET logic circuits and may realize the offset charge independent circuits. Also a very abrupt pull-in / pull-out operations of the SG-SET result in very sharp subthreshold slopes beyond the theoretical limit for CMOS.

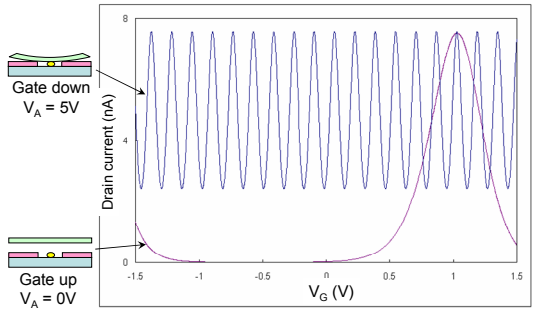

Figure 7 Switching of the Coulomb oscillation periodicity simulated for the SG-SET.

On the other hand, there are lots of new transport physics to explore for the NEMSETs associated with strong coupling of single-electron transport with low-dimensional phonons, which may lead to novel switching principles. Figure 8(a) shows an example of NEMSETs which features a suspended quantum dot (QD) built on a 400-nm-long bridge channel formed on a 50-nm-thick SOI substrate [7]. One of advantages of this structure is the fact that QD is free from the influences of the substrate, and the stray capacitance between the QD and substrate is largely reduced. In addition, the QD can be oxidized from the surrounding surface, and the effective size of the QD can be reduced easily. Clear Coulomb diamonds were observed for a wide range of temperature (Fig. 8(b)). We have also fabricated the NEMSETs with multiple QDs successfully. New switching mechanisms such as phonon blockade and electromechanical modulation of single-electron tunneling current are currently under investigation by further optimizing the channel structures.

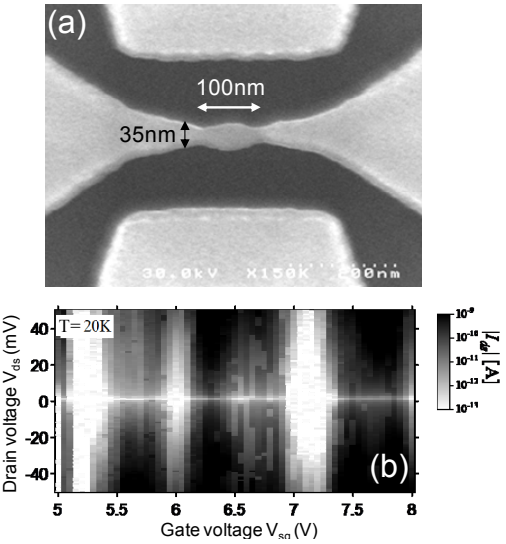

Figure 8 A NEMSET with a suspended quantum dot and observed Coulomb diamond characteristics.

4. Conclusion

We have overviewed our current attempts of co-integrating the NEM components into the conventional CMOS and SETs. Unique NEM phenomena such as mechanical bistability of the buckled floating gate and extremely abrupt and nonlinear switching of the suspended gate may provide extended performance and new functionalities beyond the limitations of the conventional devices.

Acknowledgments

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