High-Quality Schottky Contacts for Limiting Leakage Currents in Ge-Based Schottky Barrier MOSFETs

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Abstract—Schottky barrier (SB) Ge channel MOSFETs suffer from high drain-body leakage at the required elevated substrate doping concentrations to suppress source–drain leakage. Here, we show that electrodeposited Ni–Ge and NiGe/Ge Schottky diodes on highly doped Ge show low off current, which might make them suitable for SB p-MOSFETs. The Schottky diodes showed rectification of up to five orders of magnitude. At low forward biases, the overlap of the forward current density curves for the as-deposited Ni/n-Ge and NiGe/n-Ge Schottky diodes indicates Fermi-level pinning in the Ge bandgap. The SB height for electrons remains virtually constant at 0.52 eV (indicating a hole barrier height of 0.14 eV) under various annealing temperatures. The series resistance decreases with increasing annealing temperature in agreement with four-point probe measurements indicating the lower specific resistance of NiGe as compared to Ni, which is crucial for high drive current in SB p-MOSFETs. We show by numerical simulation that by incorporating such high-quality Schottky diodes in the source/drain of a Ge channel PMOS, a highly doped substrate could be used to minimize the source-to-drain subthreshold leakage current.

Index Terms—Electrodeposition, leakage current, Schottky barrier (SB) MOSFET.

I. Introduction

FOR FUTURE high-speed CMOS technology, Ge channel MOSFETs are considered as promising devices as they offer high carrier mobilities suitable for large drive current. Schottky barrier (SB) source/drain MOSFETs overcome the problems faced by the conventional transistor scaling caused by the stringent conditions required for doping with low series resistance [1]–[3]. The Ge-based SB p-MOSFETs, however, suffer from increased leakage currents due to their narrow bandgap and low SB height [4]–[6]. We have recently shown that Ni–Si diodes prepared by electrodeposition exhibit superior properties to physical-vapor-deposition-prepared diodes [7], [8]. In this paper, we show that electrodeposited Ni–Ge and NiGe–Ge Schottky diodes on highly doped Ge exhibit near-ideal SB behavior with low off current. The experimental data of the diodes are used to calibrate numerical simulations of the Ge SB MOSFET. At short channel lengths, SB MOSFETs

suffer from source-to-drain leakage currents. We show that a highly doped Ge substrate is the key to limiting source-to-drain subthreshold leakage currents. The low off current of the electrodeposited SBs on highly doped substrate might make this possible without increasing the junction leakage current at the drain/body of SB p-MOSFETs.

II. Experimental Techniques

For the fabrication of Ni–Ge SBs, Antimony-doped Ge (100) wafers were taken as the starting materials. Square patterns of sizes from 10 to 400 μm were transferred to the photoresist-coated substrates by conventional lithography. The back ohmic contacts were defined by Au–Sb evaporation and annealing the samples in an H_2/N_2 inert atmosphere. Subsequently, a 20:1 buffered HF dip for 30 s, followed by DI water dip, was performed to remove any native oxides. For electrodeposition, a Ni sulphate bath and an Autolab AUT72032 potentiostat three-electrode system with a Pt counter electrode and a saturated calomel reference electrode (SCE) were used. The deposition potential ranged from 1.10 to 1.15 V (against the SCE) for the various Ge substrates. The film thickness was monitored during electrodeposition by observing the charge accumulated at the cathode. Current (I)–voltage (V) and capacitance (C)–voltage (V) characteristic measurements were performed using a Hewlett Packard 4155A semiconductor parameter analyzer and a Hewlett Packard 4280 A, 1 MHz, C Meter/C–V plotter. Germanidation of the Ni films was performed for 20 min in the anneal chamber at temperatures ranging from 300 °C to 500 °C. The various film thicknesses were measured using scanning electron microscopy (SEM) on a cross section of the electrodeposited film.

III. Experimental Results

Typical current density (J) versus applied voltage (V) characterisics of electrodeposited Ni–Ge SBs for the three different substrate resistivities ($\rho1 = 2-2.4~\Omega \cdot$ cm, $\rho2 = 0.13-0.15~\Omega \cdot$ cm, and $\rho3 = 0.005-0.02~\Omega \cdot$ cm) and of 10-μm^2 contact area are shown in Fig. 1.

A high-quality rectifying behavior is observed for the SBs. For the highly resistive ($\rho1$) Ge, excellent SBs are achieved with very low reverse bias current, being five orders of magnitude smaller than the forward bias current at 1-V bias. Tunneling effects of this SB are negligible in the reverse bias. SBs on the medium resistive ($\rho2$) Ge showed similar rectifying
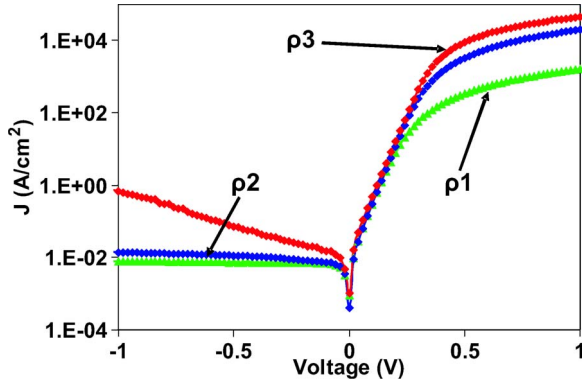
Fig. 1. $J-V$ characteristics of the Ni/Ge Schottky diodes (10-μm^2 contact) as a function of Ge resistivities ($\rho 1 = 2-2.4\ \Omega \cdot$ cm, $\rho 2 = 0.13-0.15\ \Omega \cdot$ cm, and $\rho 3 = 0.005-0.02\ \Omega \cdot$ cm).

TABLE I
EXTRACTED ϕ_n, η, R_s (FROM $J-V$ METHOD) AND ϕ_n, N_d, SUBSTRATE
RESISTIVITY ($C-V$ METHOD) OF THE Ni/Ge SCHOTTKY DIODES

Resistivity Label $\Rightarrow$	$\rho 1$	$\rho 2$	$\rho 3$
η	1.12	1.04	1.09
R_s (Ω)	30.77	16.05	11.72
ϕ_n (eV) (from J-V)	0.52	0.53	0.52
ϕ_n (eV) (from C-V)	0.56	0.53	0.53
N_d (cm^{-3})	8.7×10^{14}	1.45×10^{16}	2.9×10^{17}
Resistivity (Ω-cm) (nominal)	2-2.4	0.13-0.15	0.005-0.02
Resistivity (Ω-cm) (from C-V)	1.84	0.11	0.006

behavior with a little tunneling current in the reverse direction. On the lowly resistive substrate ($\rho 3$), Ni/Ge SB showed increased tunneling effects in the reverse bias. However, even these diodes showed excellent rectifying behavior with the reverse bias current of the diodes at the lowly resistive ($\rho 3$) substrate, still being five orders of magnitude smaller than the forward bias current. All currents can be explained by standard thermionic emission (TE) and, additionally, thermionic field emission (TFE) theory for the reverse bias. We will show in the following section by numerical simulation that both forward and reverse bias currents are dominated by electron transport. This is a significant improvement over a similar work done in literature [9], [10] where Schottky diodes grown by evaporation technique exhibited rectification of only 2–3 orders even on highly resistive Ge substrates. Breakdown of the diodes was not observed up to −3-V bias, indicating that edge effects are suppressed as explained in our previous work [11].

From the $J-V$ curves in Fig. 1, the Ni/Ge Schottky electron barrier height (ϕ_n), ideality factor (η), and series resistance (R_s) can be extracted, assuming the TE model in the forward bias [12]. The calculated SB parameters are shown in Table I for all types of substrates. For these calculations, Richardson constant (A^*) of 50 A $\cdot$ cm$^{-2} \cdot$ K^{-2} [13], [14] was used. It is seen from Table I that the SB heights are virtually constant for the Ge substrates of various resistivities. The low ideality factors indicate TE to be the dominant current conduction mechanism in the forward bias for the SBs on different substrates.
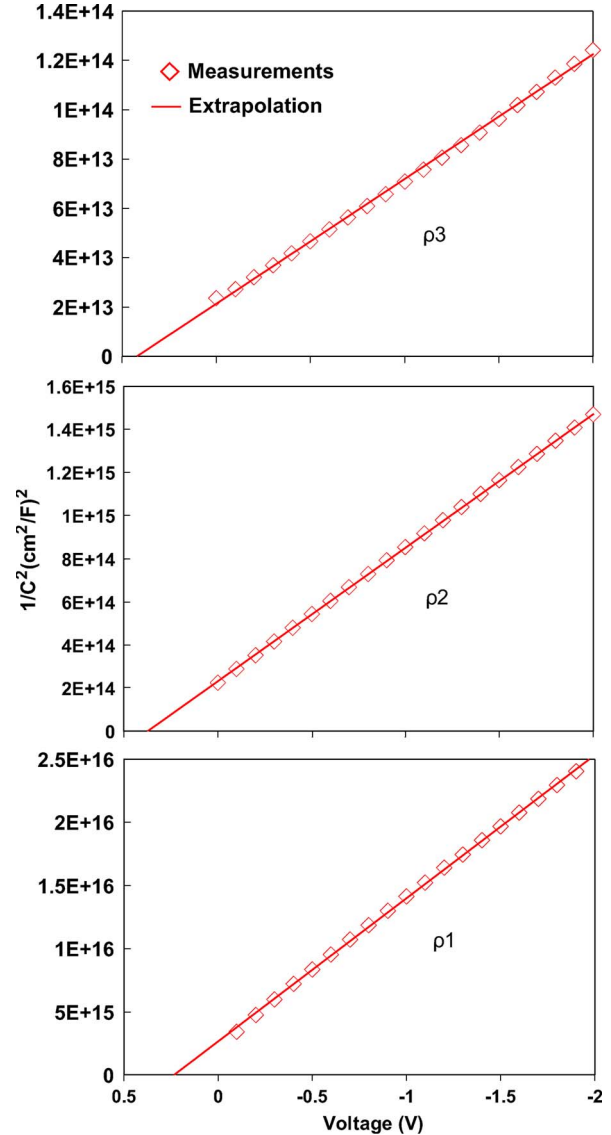

Fig. 2. $C^{-2}-V$ curve of an electrodeposited Ni–Ge contact (400 μm^2) for various substrate resistivities ($\rho 1 = 2-2.4\ \Omega \cdot$ cm, $\rho 2 = 0.13-0.15\ \Omega \cdot$ cm, and $\rho 3 = 0.005-0.02\ \Omega \cdot$ cm).

$C-V$ measurements of SBs on Ge were performed for A^*-independent measurement of the SB height. Inverse square capacitance versus voltage characteristics are shown in Fig. 2 for SBs on Ge substrates of various resistivities and having a contact area of 400 μm^2. As expected, a straight line is observed, and from its intercept on the voltage axis, the SB height (ϕ_n) is calculated [15]. Furthermore, from the slope of this characteristic, the Ge doping concentration (N_d) can be determined. For example, a value of 2.9×10^{17} cm^{-3} for N_d is obtained corresponding to a resistivity of 0.006 $\Omega \cdot$ cm, which matches the specification of the Ge substrate. Similar $C-V$ measurements were performed on SBs on the medium (0.13–0.15 $\Omega \cdot$ cm) and highly (2–2.4 $\Omega \cdot$ cm) resistive Ge and barrier heights (ϕ_n) of 0.53 and 0.56 eV, respectively, and substrate doping densities of 1.45×10^{16} and 8.7×10^{14} cm^{-3} were obtained. The barrier heights obtained are in good agreement with those obtained from the $I-V$ measurements as observed in Table I.
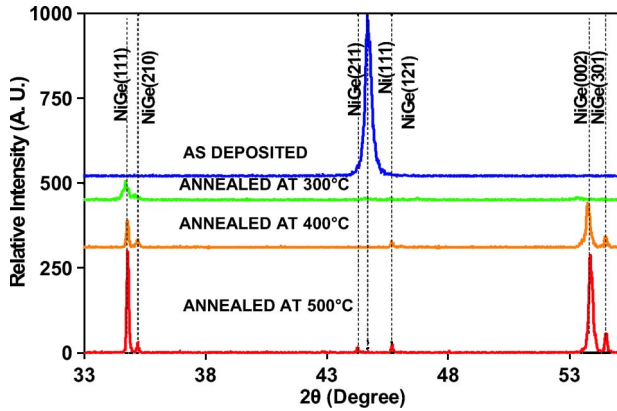
Fig. 3. XRD spectra for the as-deposited and annealed Ni/Ge samples showing transformation from Ni to NiGe.
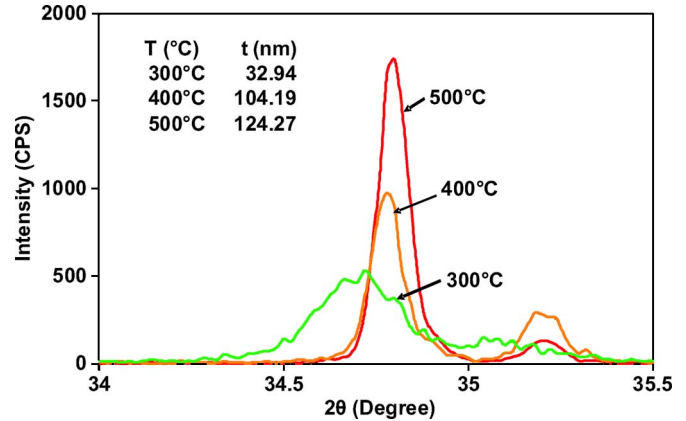

Fig. 4. XRD spectra showing the NiGe(111) peak of the Ni(70 nm)/Ge samples when annealed at various temperatures. The calculated crystallites are presented in the inset.

The electrodeposited Ni films on Ge (0.005–$0.02 \ \Omega \cdot cm$) were annealed for 20 min at temperatures ranging from 300 °C to 500 °C to investigate their Germanidation mechanism. Phase identification and crystallographic structure determination were carried out using XRD with Cu Kα radiation ($\lambda = 1.5418$ Å) in a θ–2θ geometry. Fig. 3 shows the XRD spectra for as-deposited and annealed Ni/Ge samples for initial Ni thicknesses of 70 nm. The initial Ni (111) peak at 44.68° completely disappears after annealing, indicating complete reaction of the Ni film with Ge. Peaks at 34.8°, 35.2°, 44.2°, 45.7°, 53.8°, and 54.4° are observed when the sample was annealed at 500 °C. These peaks are in excellent agreement with the θ–2θ pattern of the NiGe JCPDS standard. The peaks were identified as NiGe(111), (210), (211), (121), (002), and (301). No peaks corresponding to other Ni-Germanides, e.g., Ni_2Ge, $NiGe_2$, etc., are observed. This clearly shows only polycrystalline Ni-mono-Germanide (NiGe) phase forms at the annealing temperatures. The lattice constants of the formed NiGe are determined to be $a = 5.81$ Å, $b = 5.37$ Å, and $c = 3.40$ Å from the XRD spectra, in agreement with the reported values [16], [17].

For the 300-°C annealed samples, the NiGe peaks are very weak, while after 400-°C annealing, the peaks become quite strong. The crystallite size (t) of the grown NiGe(111) was investigated by taking further XRD scan within close intervals surrounding the peak. These are shown in Fig. 4 as a function of annealing temperature (T). The crystallite sizes are calculated from the peaks using the Scherrer relation

$$t = \frac{0.9\lambda}{d \cos \theta} \qquad (1)$$

where d is the broadening of the peaks due to the crystallite size. It was observed that t increases with increasing T.

The variation of thickness of the Ni and Ni–Ge films as a function of annealing temperature (T) was determined by SEM as shown in Fig. 5. This thickness is seen to increase with increasing T. Theoretically, the ratio of the atomic volume of NiGe and Ni is 2.44. As shown in Fig. 5, the ratio of the film thickness of NiGe at 500 °C to that of Ni is 2.53. This confirms complete reaction of the 70-nm Ni and formation of NiGe at that temperature.

In order to further exploit the Germanidation mechanism, the sheet resistance ($R_{\rm sh}$) of the grown films was measured using the four-point probe method. The obtained $R_{\rm sh}$ values were multiplied by the film thicknesses to calculate the film resistivities (ρ). The results are plotted as a function of annealing temperatures in Fig. 6. It is observed that $R_{\rm sh}$ decreased with increasing T. The measured $R_{\rm sh}$ of NiGe is $0.23 \ \Omega/sq$ when annealed at 500 °C. The low $R_{\rm sh}$ could be attributed to the increase in crystallite size at 500 °C as shown in Fig. 4. The resistivity of Ni–Ge also decreased when the films were annealed above 300 °C.

Typical current (I) versus applied potential (V) characteristics of the grown Ni(70 nm)/Ge Schottky diodes under the as-deposited and annealed conditions on lowly resistive (0.005–$0.02 \ \Omega \cdot cm$) Ge are shown in Fig. 7 for a contact pad size of 20 μm^2.

A high-quality rectifying behavior (4–5 orders in magnitude) is observed for all annealing conditions. Again, ϕ_n, η, and R_s are calculated, assuming the TE model in the forward bias region, and are presented in Table II. The values of ϕ_n are virtually constant at 0.52 eV. Assuming a Ge bandgap of 0.66 eV, the corresponding hole barrier height (ϕ_p) is 0.14 eV. This value is low enough to guarantee a large on current in SB MOSFET. At low forward bias, there is a considerable overlap of the current curves of the nonannealed Ni–Ge and NiGe–Ge samples as shown in Fig. 7. This indicates both thermal stability and Fermi-level pinning in the Ge bandgap as the barrier height is independent of the metal work function. The reverse current at 1-V bias is 1 μA for the various annealed diodes. This is a significant achievement as this value is more than an order of magnitude smaller than the reported value in literature [10] for NiGe/Ge diodes formed by evaporation on highly resistive (4–$6 \ \Omega \cdot cm$) Ge.

The low values of ideality factor for the Schottky diodes presented in Table II indicate TE to be the dominant current conduction mechanism in the forward bias. The series resistance decreases with increasing T (see the inset of Fig. 7), indicating a lower specific resistance of NiGe than Ni. This is consistent with the four-point probe measurement shown in Fig. 6.
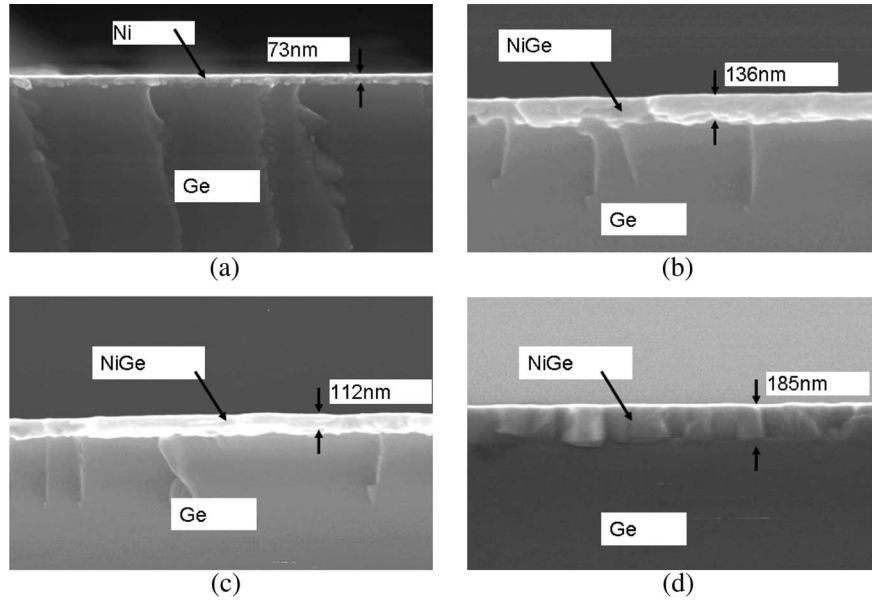
Fig. 5. Cross-sectional SEM images of the various Ni/Ge samples: (a) As-deposited, (b) annealed at 300 °C, (c) annealed at 400 °C, and (d) annealed at 500 °C.
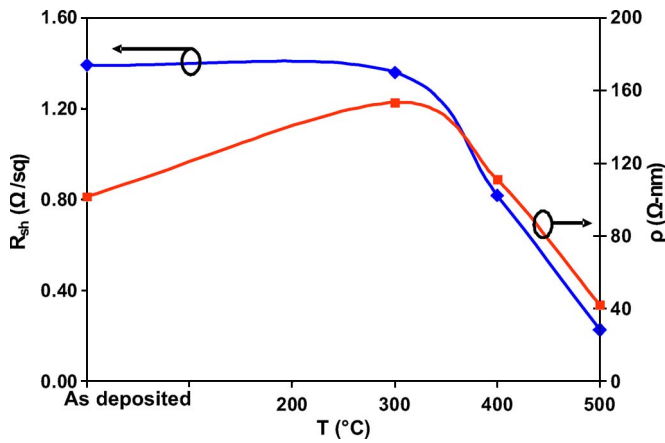

Fig. 6. R_{sh} and ρ of Ni and Ni–Ge films at various anneal temperatures. The initial Ni thickness was 70 nm. The substrate resistivity was 0.005–0.02 $\Omega \cdot$ cm.

Fig. 7. I–V characteristics of the Ni/Ge Schottky diodes, having a contact area of 20 μm^2, as a function of annealing temperatures. Ge resistivity was 0.005–0.02 $\Omega \cdot$ cm. The high forward bias region is magnified in the inset.

IV. SB MOSFET SIMULATION

The commercial TCAD simulator Sentaurus Device from Synopsys has been used for the simulation work that provided a self-consistent and fully coupled implementation of nonlocal tunnelling models of both electrons and holes. The devices were generated using Sentaurus Structure Editor and its Meshing engine. The simulator was, at first, calibrated by using the SB heights and the various experimental doping densities (N_d) of the substrates obtained by the C–V methods which were presented in Table I. To account for the substrate series resistances in the experimental results, systematic 3-D simulations of the actual substrate size and thicknesses were performed for a 10-μm^2 pad. The corresponding calculated J–V curves for the various substrate doping densities are shown in Fig. 8 along with the experimental curves. Separation of the electron and hole currents in the simulation (not shown) indicates that holes play a negligible role in the reverse and forward bias currents. The concordance of the experimental and simulated
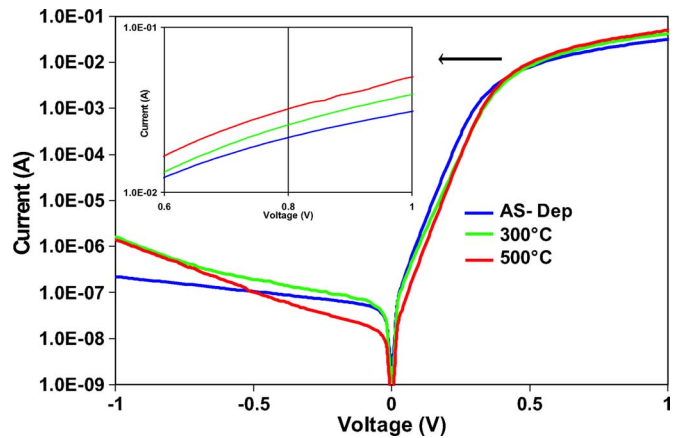
TABLE II
EXTRACTED ϕ_n, η, AND R_s OF THE Ni/Ge SCHOTTKY DIODES WITH 20-μm^2 CONTACT AREA AS A FUNCTION OF ANNEALING TEMPERATURE (T)

T(°C)	ϕ_n (eV)	η	$R_s(\Omega)$
None	0.52	1.1	21.32
300	0.52	1.27	14.79
400	0.55	1.13	11.83
500	0.55	1.08	10.85

current density curves at the various conditions confirms the full calibration of the simulator tool to both TE and TFE.

To accurately model the SB MOSFET, a fully coupled 2-D simulation was performed that included physical models, e.g., bandgap narrowing effect and dependence of mobility to normal electric field. The drain current (I_d) versus gate voltage (V_g) characteristics for a bulk SB PMOS with channel length (L_g) of 30 nm and gate oxide thickness (t_{ox}) of 0.7 nm are calculated as a function of various substrate doping densities
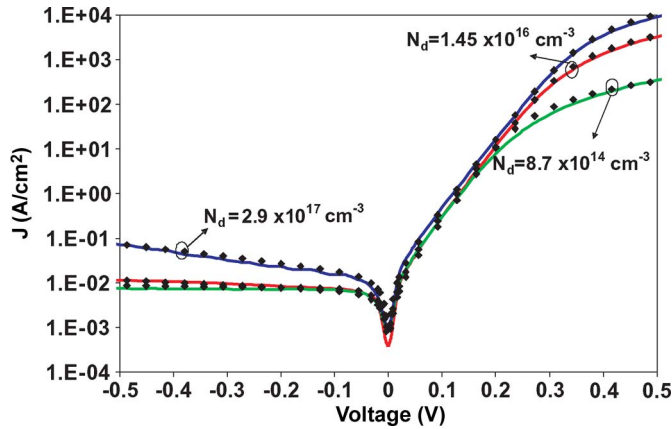
Fig. 8. $J-V$ characteristics (dotted lines) for 10-μm Ni/Ge contacts for various doping density modeled by Sentaurus Device simulator tool. The corresponding experimental curves (solid lines) are also presented for reference.
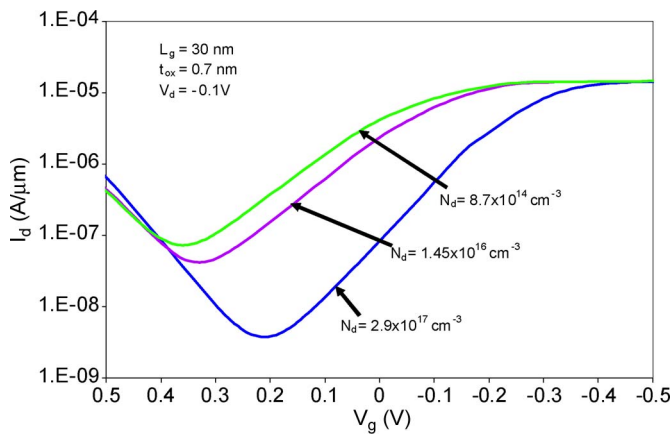

Fig. 9. Simulated transfer characteristics of 30-nm Ge channel bulk SB PMOS devices showing the effect of increasing substrate doping density on leakage currents.

Fig. 10. (a) Schematic representation of the SB PMOS structure with gate offset. X_d is the length of offset region from the drain. (b) Transfer characteristics of 30-nm Ge channel bulk SB PMOS devices for various X_d showing the effect of gate offset on leakage currents.

(N_d) and are shown in Fig. 9. The source-to-drain subthreshold leakage current can be readily obtained from the curves at $V_g = 0$. It is found that for a fixed drain bias (V_d) of -0.1 V, the leakage current is 4.5×10^{-6} A/μm when Ge n-type doping density of 8.7×10^{14} cm^{-3} was used. However, the leakage currents decreased to 2.1×10^{-6} and 8.1×10^{-8} A/μm when the substrate doping densities were increased to 1.45×10^{16} and 2.9×10^{17} cm^{-3}, respectively. Therefore, we propose that a highly doped Ge substrate could be used for a low-leakage SB MOSFET. At higher positive gate voltages, the leakage current is observed to increase for the various substrate doping densities. This is attributed to the ambipolar behavior typical of an SB MOSFET that results in a gate-induced-drain-leakage (GIDL)-like current. For higher drain voltages, e.g., $V_d = -1$ V, this leakage current is very high.

There are several methods available to suppress the GIDL-like leakage in SB MOSFETs. One method uses a field-induced drain extension [18] located between the channel and the Schottky drain. This leakage current could also be alleviated by using a recessed channel and asymmetric source/drain Schottky contacts [19]. As an alternative to these methods, an offset gate structure shown in Fig. 10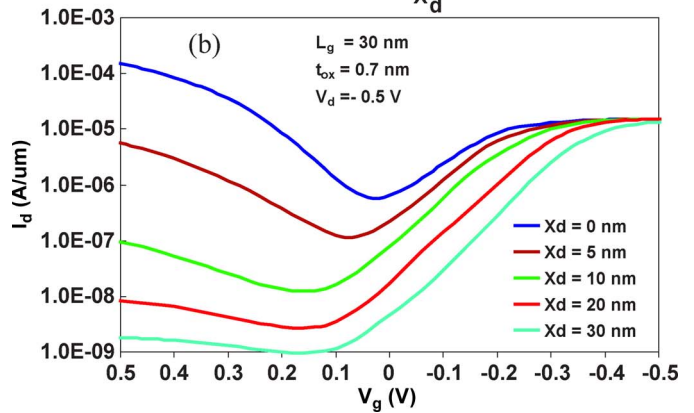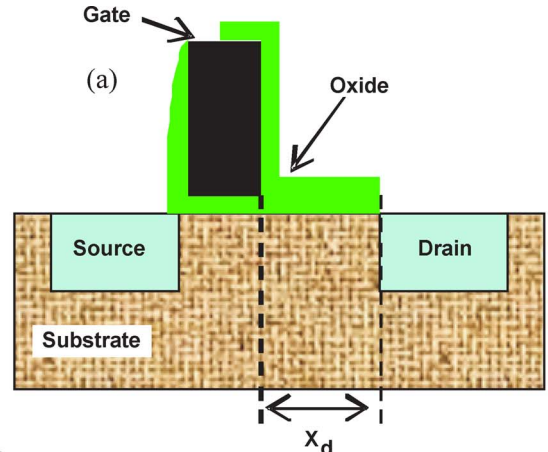(a) could be used for a 30-nm gate length device. Here, the effect of the gate bias responsible for the hole conduction is reduced by increasing the distance (X_d) between the edges of the gate and the drain.

Here, we perform numerical simulation to investigate the effect of the offset gate structure in the bulk SB PMOS. I_d versus V_g characteristics, with $L_g = 30$ nm, $t_{ox} = 0.7$ nm, and $N_d = 2.9 \times 10^{17}$ cm^{-3}, are calculated for $V_d = -0.5$ V as a function of various X_d and are shown in Fig. 10(b). It is observed that for the highly doped substrate, the leakage current is extremely high for a conventional bulk SB PMOS $(X_d = 0)$. As the gate offset from the drain is increased, superior p-channel device performance is realized on the Ge SB MOSFET. It can be seen that not only the hole conduction is gradually eliminated but also the OFF-state source–drain subthreshold leakage current is also decreased with increasing X_d. The parasitic resistance with increasing X_d, however, has not decreased the on current. This is due to the domination of the source-to-channel tunnel resistance over the resistances in the current conduction path. Therefore, by using the offset-gate structure, the off current of the SB MOSFET could be significantly reduced without affecting the on current of the device.

V. Conclusion

We report that Ni/Ge SBs formed by electrodeposition on highly doped substrate show high rectification with low leakage

current in reverse bias. The fabricated Ni/Ge diodes transformed into NiGe/Ge diodes upon annealing at 500 °C. Despite the compositional change, the SB properties were virtually unaltered due to Fermi-level pinning. The series resistances of NiGe decreased with annealing temperature which is important for high drive current in SB MOSFETs. By numerical simulation, we are able to show that the source-to-drain subthreshold leakage current could be minimized by using a highly doped Ge substrate. Therefore, we propose that electrodeposition could be used for source–drain formation of a highly doped Ge-based SB MOSFET to achieve low subthreshold leakage current.

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