Diagnosis of Multiple-Voltage Design with Bridge Defect

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***Abstract*—Multiple-voltage is an effective dynamic power reduction design technique, commonly used in low power ICs. To the best of our knowledge there is no reported work for diagnosing multiple-voltage enabled ICs and the aim of this paper is to propose a method for diagnosing bridge defects in such ICs. Using synthesized ISCAS benchmarks, with realistic extracted bridges and a parametric fault model, the paper investigates the impact of varying supply voltage on the accuracy of diagnosis and demonstrates how the additional voltage settings can be leveraged to improve the diagnosis resolution through a novel multi-voltage diagnosis algorithm. In addition it also identifies the most useful voltage settings to reduce diagnosis cost by eliminating tests at certain voltage setting using the proposed multi-voltage diagnosis approach thereby achieving high diagnosis accuracy at reduced cost.**

***Index Terms*—Logic based Diagnosis, Multiple-Vdd designs, Resistive Bridge Faults, Hard-Shorts**

I. Introduction

DIAGNOSIS is a systematic way to uniquely identify the defect causing malfunction in the circuit. It is critical to silicon debugging, yield analysis and for improving subsequent manufacturing cycle. There has been extensive work on modeling, detection and diagnosis of bridge defects [1]–[10]. However these works implicitly consider only designs using a single supply voltage Vdd. Many modern processors allow use of multiple Vdds which can be dynamically selected to reduce power consumed and still meet the computational requirements [11] and [12]. Thus it is important to investigate the effect and potential advantage of using multiple Vdd settings to improve diagnosis accuracy for such designs.

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A bridge is defined as an un-wanted metal connection between two lines of the circuit, which may deviate the circuit from its ideal behavior. In considering diagnosis of bridge defects we used a cause-effect diagnosis procedure which uses dictionaries [13]. The amount of information stored in a dictionary is a trade off between storage space and diagnostic resolution. A study reported in [14] compares these parameters for full response dictionary (that holds the detailed output response for each fault per test vector), pass-fail dictionary (which stores one bit, indicating pass or fail of a test, per test per fault) and frequency based dictionary (that holds the detection count of each fault over the entire test set). The study shows that pass-fail dictionary provides high diagnostic power (much higher than frequency based dictionary but slightly lower than full response dictionary) and higher space compaction (much higher space compaction than full response dictionary). Therefore in order to conserve storage requirements for the dictionaries we used a pass-fail dictionary [4]. However conclusions drawn through the experiments reported in this work are expected to hold if other diagnosis procedures are used (including full response dictionary or effect-cause diagnosis procedure [1], [13]).

A study comparing between better fault models or better diagnosis algorithms revealed that using a simple diagnosis algorithm on a better fault model achieves higher diagnosis accuracy [15]. It was shown by Zou *et al.* [7] that using an advanced parametric bridge fault model [16], [17], diagnosis resolution can improve over algorithms that use simpler fault models. This work also uses the same parametric fault model [17].

The nature of bridge defects in multi-Vdd designs is such that they manifest themselves at one or more voltage settings [18]–[20]. Existing diagnosis techniques use a single Vdd setting and therefore diagnosis for multi-Vdd designs imposes a challenge as bridge defects exhibit supply voltage dependent behavior. Single Vdd diagnosis for multi-Vdd designs may lead to imprecise diagnosis as shown by experimental results (Section V) of this work. Furthermore, it raises the following questions: 1) Is diagnosis resolution affected by different voltage settings? 2) If so, what voltage setting achieves the best level of diagnosis? 3) Is it possible to improve diagnosis resolution further by carrying out diagnosis at more than one

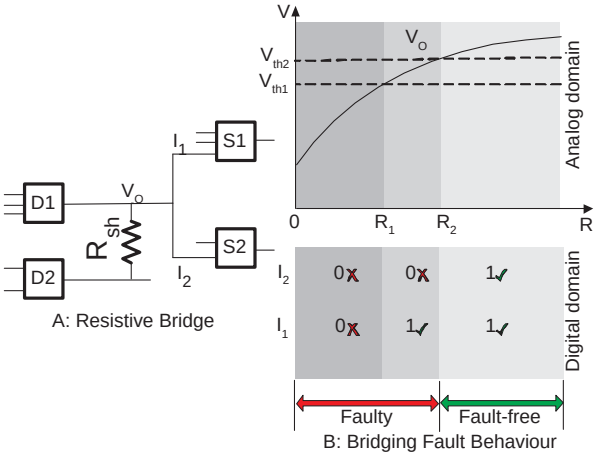

Fig. 1. Bridge fault example

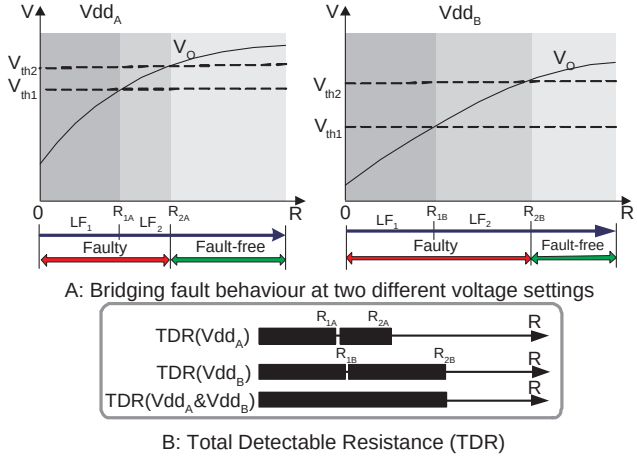

Fig. 2. Effect of supply voltage on bridge fault: Analog/Digital domain

voltage setting? To the best of our knowledge, the work reported here is the first to consider diagnosing bridge defects in multi-Vdd designs and present results to show that the lowest supply voltage provides the best resolution for single voltage diagnosis. This work further exploits the additional information from other voltage settings to improve the diagnosis accuracy up to 72% over single voltage diagnosis. In addition this work also analyses hard-shorts (bridges with 0 Ω resistance) and experimental results show that diagnosis accuracy has little variation across different voltage settings for this class of defects.

For Multi-Vdd designs that operate at more than one voltage setting, it is desirable to reduce diagnosis cost by achieving the minimum possible Test Application Time (TAT), while achieving high diagnosis accuracy. Therefore, it is important to investigate the most useful Vdd settings or combination of Vdds, which may yield the desired outcome by omitting tests at some voltage settings. In this work, we show experimental results using different Vdd pairs and identify the most useful Vdd pair, such that high diagnosis accuracy is achieved using reduced TAT, thereby reducing diagnosis cost.

The paper is organized as follows: Section II gives an overview of resistive bridge defects and their behavior in the context of multi-Vdd design. The motivation for multi-Vdd diagnosis is discussed in Section III. In Section IV we present a multi-Vdd diagnosis algorithm for bridge defects. Experimental setup and results are reported in Section V, and finally Section VI concludes the paper.

II. Preliminaries

A typical bridge fault behavior is illustrated in Fig. 1. Fig. 1-A shows a resistive bridge, D1 and D2 are the gates driving the bridged nets, while S1 and S2 are successor gates, i.e., gates having inputs driven by one of the bridged nets. Let us consider the case when the output of D1 is driven high and the output of D2 is driven low. The dependence of the voltage level on the output of D1 (V_O) on the equivalent resistance of the physical bridge is shown in Fig. 1-B (based on Spice simulation with 0.12μm library and the well-known behavior of resistive bridge for different resistance values). The deviation of V_O from the ideal voltage level (Vdd) is highest for small values of R_{sh} and decreases for larger values of R_{sh}. To translate this analog behavior into digital domain, the input threshold voltage levels V_{th1} and V_{th2} of the successor gates S1 and S2 have been added to the V_O plot. For each value of the bridge resistance R_{sh}, the logic values read by inputs I_1 and I_2 can be determined by comparing V_O with the input threshold voltage of the corresponding input. These values are shown in the second part of Fig. 1-B (marked as "digital domain"). Crosses are used to mark the faulty logic values and ticks to mark the correct ones. It can be seen that, for bridges with $R_{sh} > R_2$, the logic behavior at the fault site is fault-free (all inputs read the correct value), while for bridges with R_{sh} between 0 and R_2, one or more of the successor inputs are reading a faulty logic value. The R_{sh} value corresponding to R_2 is normally referred to as "critical resistance" as it represents the crossing point between faulty and correct logic behavior. Methods for determining the critical resistance have been presented in [21].

A number of bridge resistance intervals can be identified based on the corresponding logic behavior. For example, bridges with $R_{sh} \in [0, R_1]$ exhibit the same faulty behavior in the digital domain (all successor inputs read the faulty logic value), similarly, for bridges with $R_{sh} \in [R_1, R_2]$, successor gate S2 reads the faulty value, while S1 reads the correct value, and finally for $R_{sh} > R_2$ all the successor gates read the correct logic value. Consequently, each interval $[R_i, R_{i+1}]$ corresponds to a distinct logic behavior occurring at the bridge fault site.

Next, we provide an analysis of the effect of varying supply voltage on bridge fault behavior, which explains why defects behave differently at different voltage settings [17], [18]. Fig. 2-A show the relation between the voltage on the output of

gate D1 (Fig. 1-A) and the bridge resistance for two different supply voltages Vdd_A and Vdd_B. Fig. 2-A also shows how the analog behavior at the fault site translates into the digital domain. Using similar explanation (as for Fig. 1-B), we can see that two distinct Logic Faults LF1 and LF2 can be identified for each Vdd setting. However, because the voltage level on the output of D1 does not scale linearly with the input threshold voltages of S1 and S2 when changing the supply voltage, the resistance intervals corresponding to LF1 and LF2 differ from one supply voltage setting to another [19], [20]. Fig. 2-B shows the Total Detectable Resistance (TDR) for the LFs detected at two voltage settings separately and combined as well. This Vdd behavior of defect also means that a test pattern targeting a particular logic fault will detect different ranges of physical defects when applied at different supply voltage settings. For example, at Vdd_A, a test pattern targeting LF2 will detect bridges with $R_{sh} \in [R_{1A}, R_{2A}]$, while at Vdd_B it will detect a much wider range of physical bridges ($R_{sh} \in [R_{1B}, R_{2B}]$). Furthermore, this means that same defect can be covered at more than one voltage setting.

A sub-class of resistive bridging faults is hard-short, which is observed when the nets connected with one another are at 0 Ω. The behavior of hard-shorts in the context of multiple voltage settings can be understood from Fig. 1 and Fig. 2. In Fig. 1, since the value of R_{sh} is 0 Ohms, the logic behavior at the fault site does not vary at two different Vdd settings (LF1 at both Vdd settings). In general, this similarity in logic behavior at two Vdd settings suggests that fault detection (for hard-shorts) may have lesser dependence on voltage setting used, in comparison to bridges with higher resistance values.

From diagnosis point of view it is interesting to analyze the impact of covering the same defect (specially, bridges with higher resistance values) at more than one voltage setting and to analyze its effect on diagnosis resolution, i.e., can it help to improve the diagnosis resolution over single voltage diagnosis? The next section uses illustrative examples to show that combining the information gathered by diagnosing at different voltage settings may help improve the diagnosis accuracy over single voltage diagnosis.

III. Motivations for Multi-Vdd diagnosis

This section presents two illustrative examples to highlight the possible improvement in diagnosis by carrying it out at multiple voltage settings, using a simple pass/fail test. As discussed in section II, defects caused by a resistive bridge consists of resistance interval(s) detectable at one or more voltage settings. The resistance range (at each voltage setting) corresponds to a faulty logic behavior in digital domain. Total detectable resistance for the bridge comprises of union of resistance intervals detectable at each voltage setting. This is further elaborated in Fig. 3, which shows two bridge locations (BL-A and BL-B) in a circuit structure similar to the one shown in Fig. 1-A and is found by using the same mechanism as for Fig. 2 using three voltage settings. Fig. 3 shows the V_o behavior of bridges at three different voltage settings in analog domain and corresponding logic faults marked by TDR(V_1), TDR(V_2), and TDR(V_3) respectively. It should be noted that two logic faults exist for each bridge at each voltage setting (shown by TDR(V_1) etc), but only one is assumed to be detectable. Logic faults shown in Fig. 3 are magnified and re-drawn in Fig. 4, which shows the total detectable resistance for the two bridges by combining information from all three voltage settings. For instance, in case of BL-A, resistance range marked by interval-A is detectable at V1 only, similarly resistance range marked by interval-B is detectable at both V1 and V2.

TABLE I
Resistance intervals exposed by single failing test at different voltage settings

	Bridge Location-A					Bridge Location-B				
	A	B	*C*	D	E	A	B	*C*	D	E
V1	D	D	*D*	ND	ND	D	D	*ND*	ND	ND
V2	ND	D	*D*	D	ND	ND	D	*D*	D	ND
V3	ND	ND	*D*	D	D	ND	ND	*ND*	D	D

The illustrative examples show the possible improvement by multiple voltage diagnosis over single voltage diagnosis. The two examples inject two different defects and are based on the following assumptions: 1) Single defect can be active at a given time. 2) There is only one Failing Pattern (FP) in the diagnostic test set, which detects the two defects. Fig. 4 shows all the intervals that are detectable at different supply voltages by the same FP. Table I maps the Detected/Not-Detected (D/ND) status of all intervals shown in Fig. 4 for the two bridges.

A. Combining Diagnosis Information

In the first case, we inject a defect consisting of resistance value from interval *C* of bridge-A (Fig. 4). In this scenario the diagnostic test applied at each voltage setting would result in the following response: (V1, V2, V3) = (D, D, D), i.e., the defect is detected at all three voltage settings.

We first carry out diagnosis at each voltage setting separately and then at all three voltage settings, using the information provided by Table I and the tester response. As mentioned earlier Table I shows the (D/ND) status of each interval of the two bridges, as detected by the only FP. The tester response at V1 is “D”, which means that the diagnosis callout at V1 is: bridge-A (intervals A, B, C) and bridge-B (intervals A, B). At V2 the tester response is “D”, which means that the diagnosis callout at V2 is: bridge-A (intervals B, C, D) and bridge-B (intervals B, C, D) and finally at V3 the tester response is “D”, and the diagnosis callout is: bridge-A (intervals C, D, E) and bridge-B (intervals D, E). Next, we take into account the tester response at all three voltage settings, which is (D, D, D) and by combining the diagnosis callout at each voltage setting, we can identify the bridge and resistance interval that is common

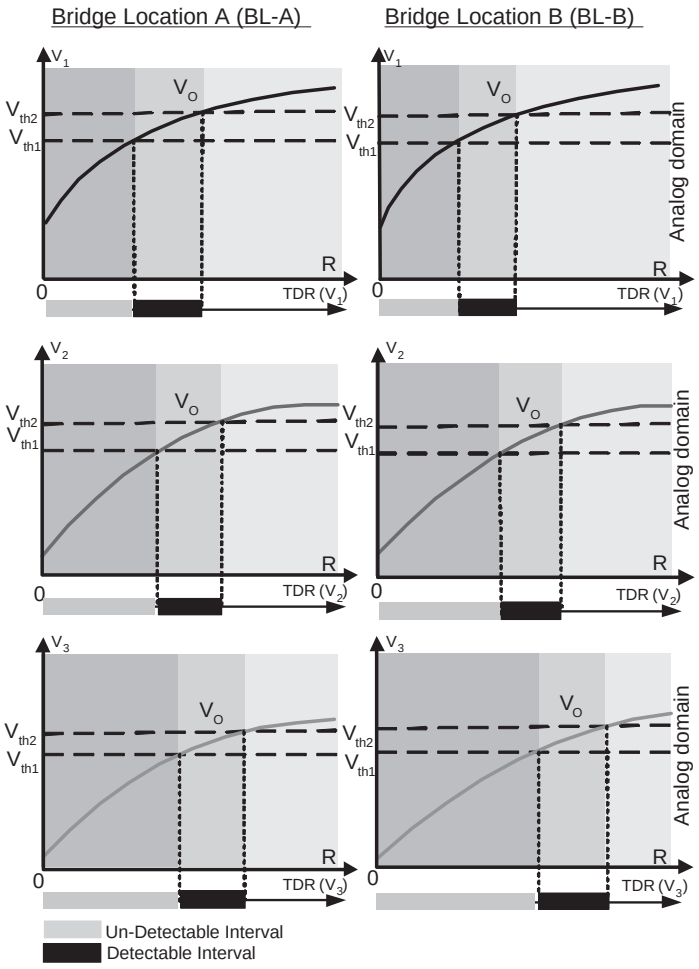

Fig. 3. Analog behavior of resistive bridges at three different voltage settings

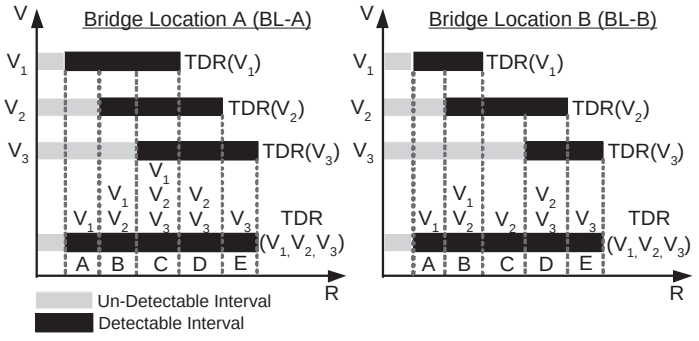

Fig. 4. Two bridges detected by the same test pattern

across all three voltage settings, i.e., bridge-A (interval C), which is indeed the actual inserted defect.

From this example, we can see that it is possible to improve the diagnosis callout by combining the information obtained from diagnosing the defect at three different voltage settings.

B. Passing Resistance Interval

This step further exploits the additional information, which is only available by diagnosing the design using multiple voltage settings. The diagnostic test applied at multiple voltage settings may detect a defect at one voltage setting but it may not detect it at another voltage setting. This concept is shown in Fig. 2-B, a resistance range $R_{sh} \in [R_{2A}, R_{2B}]$ of Total Detectable Resistance (TDR) (Vdd_A & Vdd_B) can only be covered at Vdd_B. This means that a test pattern can detect this defect at Vdd_B only and will not be able to detect it at Vdd_A. Such test patterns that show a Detected "D" status at one voltage setting and Not-Detected "ND" status at other(s) are referred to as Partially Passing (PP) patterns.

The following example shows the effect of using PP patterns to improve diagnosis resolution. For this example we assume that interval *C* of bridge-B is causing malfunction and only one test pattern is a failing test pattern (FP). In this case, the tester response at three voltage settings (V1, V2, V3) is (ND, D, ND). The diagnosis is carried out using the information available in Table I and the tester response. Table II shows the progressive reduction in the list of suspected bridges as a result of each diagnosis step. The left most column shows the voltage setting, the next column shows the Bridges (Resistance Intervals) detected by the FP at the particular voltage (as shown in Table I) and the last column shows the D/ND status, using the Tester Response (TR). We first carry out diagnosis at V2 as that has the detected status alone. The tester response at V2 is "D", which means that the diagnosis callout at V2 is: BL-A (intervals B, C, D) and BL-B (intervals B, C, D). Next, we take into account the resistance intervals for the two bridges that are detectable at other voltage settings, i.e., V1 and V3. At V1, the detected bridges (resistance intervals) by the FP are: BL-A (intervals A, B, C) and BL-B (intervals A, B), but since the tester response is "ND", this means that all these intervals for the two bridges can not be causing malfunction in the circuit, and therefore the common intervals (for each bridge) can be removed from the suspected bridge list. As shown in Table II, after removing the common intervals, the remaining intervals for the two bridges are: BL-A (interval D) and BL-B (interval C, D). Next, we carry out the same procedure at V3 and remove the common interval for the two bridges from the suspected bridge list, i.e, interval D for both BL-A and BL-B. This gives BL-B (interval C) alone as the suspected candidate list, which in turn is the exact diagnosis. Furthermore it is an improvement over single-Vdd diagnosis (at V2: BL-A (intervals B, C, D) and BL-B (intervals B, C, D)).

TABLE II
IMPROVEMENT BY REMOVAL OF PASSING RESISTANCE INTERVALS

Vdd	Bridges (Resistance Intervals)		TR
V2	BL-A (B, C, D)	BL-B (B, C, D)	D
V1	BL-A (A, B, C)	BL-B (A, B)	ND
Suspected Bridges: BL-A (D), BL-B (C, D)			
V3	BL-A (C, D, E)	BL-B (D, E)	ND
Suspected Bridges: BL-A (Ø), BL-B (C)			

The above example shows the usefulness of Partially Passing patterns in improving diagnosis, which are not available at single voltage setting.

IV. MULTI-VDD DIAGNOSIS ALGORITHM

This section presents the diagnosis algorithm that carries out diagnosis at single/multiple voltage settings using a simple pass/fail (D/ND) test. The algorithm uses dictionary and tester response; the flow is shown in Fig. 5. The dictionary holds the resistance range of each bridge, which is detected by a Test Pattern (TP) when it is applied at a certain voltage setting V_i, where V_i could be V_1, V_2, or V_3. From now onwards, we will refer to it as (TP, V_i) pair. Every bridge with its complete resistance range is fault-simulated separately by each one of the (TP, V_i) pair. The detected resistance interval(s) of each bridge is stored in the dictionary, against the (TP, V_i) pair that detects it. Fault simulation is performed using the procedure outlined in [19], [20]. The tool flow for generating dictionaries is shown by Fig. 8 and further explained in section V. The diagnosis algorithm also uses emulated tester response using the fault simulator presented in [19], [20]. It provides all the Failing Patterns (FP), corresponding voltage setting V_i on which the defect is detected, and the observed primary output response of the design, i.e., all (FP, V_i, PO) tuple(s). This diagnosis algorithm consists of three types of intersection and primary output matching scheme, which are explained next:

A. Bridge Intersection (BI)

The diagnosis algorithm starts by reading all the (FP, V_i) pairs generated by the tester. Using the dictionary and each (FP, V_i) pair, it retrieves all the bridges along with their resistance intervals that are detected by the particular (FP, V_i) pair. It then identifies the common bridges that each one of the (FP, V_i) pair detects. The list of common bridges across all the (FP, V_i) pairs gives the "first suspected candidates list".

B. Resistance Range Intersection (RRI)

The size of "first suspected candidates list" can be further reduced by using the fact that resistive bridge defects manifests themselves at a single resistance value. This means that a defect should show a common resistance interval across all the failing patterns, otherwise it can be removed from the suspected candidate list. This idea is illustrated by Table III. The table lists the two bridges (BL-A and BL-B) and their respective resistance intervals, detected by each one of the (FP, V_i) pair. It can be seen that only resistance interval "C" of BL-A is common to all three (FP, V_i) pairs and there is no resistance interval of BL-B that is common across all FPs. This means BL-B can be removed from the suspected candidates list. RRI removes the bridges with inconsistent resistance intervals and returns the "second suspected candidates list".

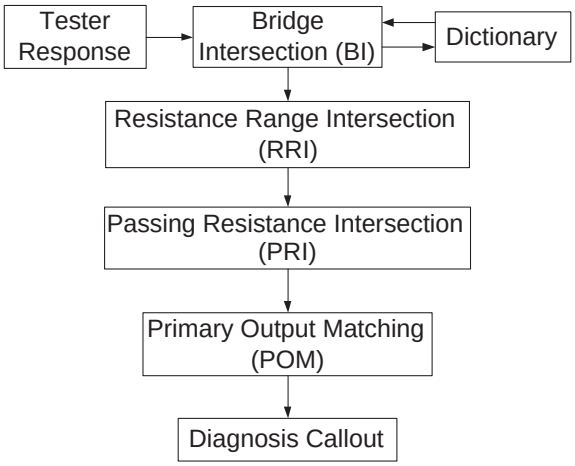

Fig. 5. Flow of proposed Multi-Vdd Diagnosis Algorithm

TABLE III
DIAGNOSIS IMPROVEMENT BY RESISTANCE RANGE INTERSECTION

	Suspected Bridges (Resistance Intervals)	
(FP, V1)	BL-A (A, B, C)	BL-B (C, D, E)
(FP, V2)	BL-A (B, C, D)	BL-B (A, B, F)
(FP, V3)	BL-A (A, C, D)	BL-B (A, E)
RRI	BL-A (C)	

C. Passing Resistance Intersection (PRI)

The purpose of Passing Resistance Intersection (PRI) is to remove the resistance interval(s) (for each bridge in the "second suspected candidate list"), which is not causing malfunction in the circuit, thereby narrowing the suspected list of bridges. This is achieved by using the PP Patterns (test patterns that pass at one voltage setting but fail at another), dictionaries and the "second suspected candidate list". Dictionaries hold the detectable resistance interval(s) of all bridge locations, detected by a test pattern when applied at a certain voltage setting. Test patterns that pass at a certain voltage setting are referred as (PP, V_i) pair. This means that (PP, V_i) pair holds the resistance interval(s) (for respective bridges) that is not causing malfunction in the circuit and can be safely removed from the resistance range of suspected bridges. Bridges with empty list of resistance intervals can be removed from the suspected candidates, thereby improving diagnosis accuracy. The algorithm for this diagnosis step is outlined in Fig. 6.

Input: List of (FP, V_i) pairs, Suspected Bridge List
1: Using the (FP, V_i) pair, compile the list of (PP, V_i) pair.
2: **for all** (PP, V_i) pairs **do**
3: Fetch the detected resistance interval for each bridge from the dictionary.
4: **end for**
5: PP Bridge List = Compute the overall passing resistance interval(s) for each bridge in all of (PP, V_i) pairs.
6: **for all** $BL_i \in$ Suspected Bridges **do**
7: $RI_i =$ Resistance Interval(s) of BL_i
8: **for all** $BL_j \in$ PP Bridge List **do**
9: **if** $BL_i = BL_j$ **then**
10: $RI_j =$ Resistance Interval(s) of BL_j
11: $ORI = RI_i \bigcap RI_j$
12: $RI_i = RI_i - ORI$
13: **end if**
14: **end for**
15: **if** $RI_i = \emptyset$ **then**
16: Remove BL_i from Suspected Bridge List
17: **end if**
18: **end for**
19: **return** Suspected Bridge List

Fig. 6. Passing Resistance Intersection

Input: List of (FP, V_i, PO) tuple, Suspected Bridge List
Output: Final Bridge List
1: **for all** $BL_i \in$ Suspected Bridges **do**
2: **for all** $RI_k \in$ Resistance Interval of BL_i **do**
3: **for all** $FP_j \in$ (FP, V_i, PO) tuple **do**
4: fault simulate RI_k using (FP_j, V_i)
5: OR = Output of DUT in presence of RI_k
6: **if** OR $\neq$ PO of FP_j **then**
7: Remove RI_k from BL_i
8: Move to next RI of BL_i (k=k+1)
9: break /* go to line 3 */
10: **end if**
11: **end for**
12: **end for**
13: **if** $BL_i = \emptyset$ **then**
14: Remove BL_i from Suspected Bridge List
15: **end if**
16: **end for**
17: Final Bridge List = Suspected Bridge List
18: **return** Final Bridge List

Fig. 7. Primary Output Matching

The algorithm starts by first finding the passing voltage(s) for all the (FP, V_i) pairs and storing the corresponding (PP, V_i) pairs. It then fetches the list of all detected bridges with their corresponding resistance interval(s), for all the (PP, V_i) pairs, from the dictionary. These two steps are shown in lines 1-4. In line 5, the algorithm compiles the "PP Bridge List" by combining the resistance interval(s) of each bridge, detected by (PP, V_i) pair, i.e., "PP Bridge List" holds the non-faulty resistance interval(s) of each bridge.

The algorithm goes over each bridge in Suspected Bridge list (one-by-one) and identifies the overlapping resistance interval(s) of the same bridge in PP Bridge list. This overlapping resistance interval(s), marked as ORI, is removed from the list of resistance interval(s) of the particular bridge in Suspected Bridge list. This process is repeated for all the bridges in Suspected Bridge list and is shown by lines 6-14. Next, it removes bridges with empty list of resistance intervals, from Suspected Bridge list. This step is shown by lines 15-17. Finally, the algorithm returns the "Final Bridge List", which holds all the bridges with their resistance intervals.

D. Primary Output Matching (POM)

Primary Output Matching (POM) improves diagnosis accuracy further by removing resistance intervals (for each suspected bridge), which produce a different output response than produced by the defect. The improvements achieved by this step are demonstrated by experimental results, as discussed in section V. As mentioned earlier, the emulated tester response stores the primary output values for each failing pattern in the form of (FP, V_i, PO) tuple. POM is accomplished by applying failing pattern(s) in presence of each resistance interval (of every bridge) and comparing the observed output response with the one recorded by the tester for the particular (FP, V_i, PO) tuple. The resistance intervals, which deviate from the expected output response (stored in the tuple) are removed from the resistance intervals of the suspected bridge. In this way suspected resistance intervals are reduced (from respective bridges); finally bridges without any suspected resistance interval are completely removed from the suspected bridge list. The procedure is outlined in Fig. 7.

The algorithm starts by fault simulating (using the procedure in [19], [20]) each resistance interval of the suspected bridge list using the (FP, V_i, PO) tuple and compares the output response of the DUT (marked by OR on line 5) with PO member of the tuple. It removes resistance interval from suspected bridge in case of a mismatch and moves to the next resistance interval, otherwise it applies next failing pattern, this is shown by lines 6-10. Finally the algorithm removes those bridges from the suspected bridge list which have no resistance interval, as shown by line 13-15. This process is repeated for all the suspected bridges.

It should be noted that proposed diagnostic flow outlined in Fig. 5 applies POM as the last step. The suspected bridge list is greatly reduced by first three intersection procedures (BI, RRI, PRI) and POM is applied on reduced number of suspected bridges, which restricts the computation time of the algorithm, as fault simulation is applied only on the remaining resistance intervals of suspected bridges.

V. Experimental Results

Five experiments are conducted to analyze and validate the proposed Multi-Vdd diagnosis algorithm and to analyse the trade-offs between diagnosis cost and accuracy. These experiments use ISCAS'85 and '89 full scan circuits. The benchmark circuits are synthesized using ST Microelectronics 0.12μm cell library. The tool flow to generate dictionaries is shown by Fig. 8. For each design, non-feedback bridges are identified from the circuit layout. The "extractRC" tool from Cadence is used to get all the pairs of nets that are capacitively coupled. These pairs of nets are the most likely bridge locations. Feedback bridges are identified and removed. Table IV shows different circuits used, along with total number of gates and extracted bridges for each circuit. The dictionaries are generated by fault-simulating 500 pseudo-random test patterns[1] at three different voltage settings ($0.8V$, $1.0V$, $1.2V$) against each bridge, as discussed in section IV. Same test patterns are applied at each voltage setting for fair comparison between diagnosis at different voltage settings. The tester is emulated using the fault simulator described in [20]. A study presented in [22] on 14 wafers from different batches and different production lines concluded that 98.3% of resistive bridges are $\leq$ 5 kΩ, while considering upper bound of uncertainty. Therefore to mimic the real scenario, defects are injected by randomly selecting a resistance value between 0-5 kΩ for a randomly selected bridge. The tester applies all 500 TPs at different voltage settings and outputs the (FP, V_i, PO) tuples for the diagnosis algorithm. For each circuit, 500 such random defects are injected (one at a time). A set of parameters are defined as follows to categorise the diagnosis callout for each test case.

1) **Exact (EXT):** The test case for which the diagnosis procedure returns a single bridge location and that bridge matches with the injected random bridge.
2) **Contains (CNT):** The test case for which the diagnosis procedure returns more than one bridge location and one of them matches with the injected random bridge.
3) **Empty (EMT):** The test case for which the diagnosis procedure does not return any bridge location.

This setup is used to conduct five experiments. The first experiment analyses the voltage setting that achieves best level of diagnosis, second shows the possible improvement in diagnosis accuracy by carrying it out at multiple-voltage settings. Third experiment analyses the impact of missing out diagnosis at one of the three voltage setting and shows the effect of conducting diagnosis on different Vdd pairs {(0.8V, 1.0V), (0.8V, 1.2V), (1.0V, 1.2V)}. This experiment is motivated towards saving tester time while recognizing the Vdd pair that achieves highest diagnosis accuracy. The fourth experiment is geared towards getting an insight into diagnosis of hard-shorts in the context of multi-Vdd designs, as they behave differently than bridges with higher resistance value. Last experiment shows that higher diagnosis accuracy can be achieved using larger (or high resolution ATPG generated) tests.

[1]Please note that we used 1000 pseudo-random test patterns at each Vdd setting in the earlier version of this work presented at ETS'08, therefore diagnosis callout differ from results reported in ETS'08.

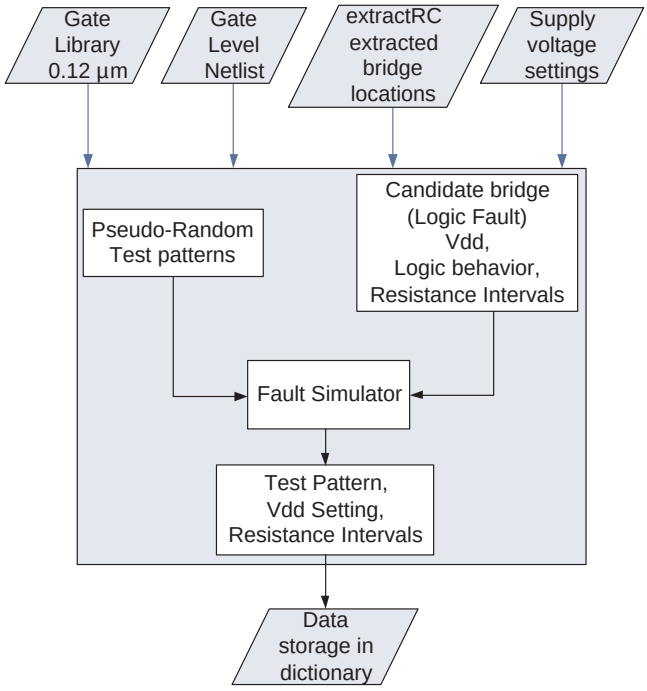

Fig. 8. Tool flow for Dictionary generation

TABLE IV
Benchmarks

CKT.	# Gates	# Bridges
c432	93	47
c880	161	69
c499	187	85
c1908	205	98
c1355	226	80
s1488	281	435
s9234	434	223
c3540	439	363
s5378	578	305
c7552	731	578
s13207	1064	358
s15850	1578	943
s35932	3689	1170
s38584	5133	2937

A. First Experiment

The first experiment uses first two steps of the proposed diagnosis algorithm, i.e., Bridge Intersection and Resistance Range Intersection at each voltage setting separately. For

TABLE V
DIAGNOSIS CALLOUT AT SINGLE VOLTAGE SETTING

CKT.	@ Vdd 0.8V			@ Vdd 1.0V			@ Vdd 1.2V		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	**350**	107	43	302	94	104	264	101	135
c880	**423**	41	36	355	47	98	297	45	158
c499	**330**	97	73	290	88	122	245	91	164
c1908	**263**	190	47	230	174	96	202	154	144
c1355	**372**	76	52	329	79	92	289	81	130
s1488	**228**	230	42	194	200	106	173	171	156
s9234	0	362	138	0	305	195	0	271	229
c3540	**339**	133	28	281	141	78	239	133	128
s5378	**102**	320	78	85	286	129	75	246	179
c7552	**369**	99	32	298	100	102	253	91	156
s13207	79	266	155	66	241	193	**129**	141	230
s15850	0	468	32	0	406	94	0	355	145
s35932	**276**	150	74	250	141	109	211	120	169
s38584	**180**	265	55	159	233	108	133	206	161

every defect these two steps are carried out at each voltage setting independently and results are compiled to compare the diagnosis accuracy at each voltage setting.

Table V tabulates the outcome of the experiment. The first column shows the benchmark circuits, the next three main columns, marked with "@ Vdd $0.8V$", "@ Vdd $1.0V$" and "@ Vdd $1.2V$", show the number of test cases which fall into one of the three diagnostic categories (EXT, CNT, EMT) as a result of applying first two steps of the proposed diagnosis procedure at the particular voltage setting. It can be observed from Table V that diagnosis accuracy is highest at $0.8V$ with highest number of Exacts and least number of Empty callouts for all the circuits. It is only for s13207 that we notice higher number of Exacts at $1.2V$ in comparison to other voltage settings. It was further investigated by analyzing the detailed diagnosis callout, which shows that majority of test cases diagnosed exactly at 1.2V are included in the CNT group with 2-3 candidate bridges at other voltage setting. From this experiment we can observe that the lowest voltage setting achieves highest diagnosis accuracy for a large majority of circuits, which is similar to the findings reported recently by Arumi *et al.*, using current based diagnosis [23].

From Table V it can also be observed that the number of empty callouts are quite high for all the circuits. This is further probed by a small experiment using circuits with higher number of empty callouts in Table V. In this experiment 500 random defects are inserted but unlike previous experiment, each defect is detectable at at-least one voltage setting and the outcome is tabulated in Table VI. In Table VI it should be noted that the number of empty callouts are quite high at 1.0V and 1.2V in comparison to 0.8V. Empty callouts at 0.8V are very few and these defects are then detected at higher voltage settings for s9234, s5378 and s13207. This behavior can be understood from the study reported in [24], which shows that for some bridges connected by gates of equal drive strength, higher Vdd is more effective for fault detection. This experiment shows that logic faults have higher detectability at the lowest voltage setting (0.8V) as a defect does not show a faulty logic behavior at higher voltage settings, which is in line with previously reported research [25]. Secondly high empty callouts (in Table V) is also due to using pseudo-random test patterns, which are not optimized for defect detection and are used for illustration purposes.

TABLE VI
ANALYSIS FOR EMPTY CALLOUTS

CKT.	@ Vdd 0.8V			@ Vdd 1.0V			@ Vdd 1.2V		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c499	385	115	0	336	107	57	283	109	108
c1908	291	209	0	252	192	56	220	170	110
c1355	415	85	0	367	189	44	321	90	89
s9234	0	499	1	0	415	85	0	365	135
s5378	113	384	3	93	342	65	84	291	125
s13207	117	380	3	96	341	63	185	203	112

B. Second Experiment

The second experiment uses the complete diagnosis algorithm across all the voltage settings. In this case, the tester response holds the failing patterns over all three voltage settings and corresponding primary output response. Table VII shows the outcome of this experiment. The 2^{nd} main column marked with "RRI", shows the effect of "Resistance Range Intersection" by taking into account all bridges (with their resistance ranges) detected at all voltage settings. The 3^{rd} main column marked with "PRI", shows the effect of applying "Passing Resistance Intersection" by using the partially passing patterns. The last main column marked with "POM", shows the effect of applying "Primary Output Matching" by fault simulating the suspected bridges using (FP, V_i, PO) tuples. From Table VII it can be observed that in all cases POM achieves best diagnosis accuracy with highest number of Exact callouts for all the circuits. It should also be noted from Tables V and VII that "RRI" marginally improves over diagnosis at 0.8V. For majority of circuits, the number of Exact callouts at 0.8V have improved by less than 10. It is in case of c1908, s1488 and especially s13207 that it achieves significant improvement over Exact callouts at 0.8V.

The relative increase (Incr) in the number of Exact callouts by PRI and POM over other schemes are shown in 2^{nd} and 3^{rd} main columns of Table VIII by comparing the number of Exact callouts in each case. In 2^{nd} main column of Table VIII, we list the relative increase in diagnosis accuracy of PRI over: A) "$0.8\,V$" (2^{nd} column of Table V) and B) "RRI" (2^{nd} column of Table VII). It should be noted that "PRI" achieves substantial improvement in diagnosis accuracy for all the circuits, showing up to 32.8% improvement over diagnosis callout at "0.8V" and

TABLE VII
DIAGNOSIS CALLOUT AT MULTIPLE VOLTAGE SETTINGS

CKT.	RRI			PRI			POM		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	357	100	43	383	74	43	**419**	38	43
c880	424	40	36	437	27	36	**441**	23	36
c499	330	97	73	376	51	73	**410**	17	73
c1908	276	177	47	326	127	47	**385**	68	47
c1355	373	75	52	396	52	52	**423**	25	52
s1488	251	207	42	347	111	42	**389**	69	42
s9234	0	363	137	109	254	137	**275**	88	137
c3540	340	133	27	395	78	27	**427**	46	27
s5378	105	320	75	250	175	75	**355**	70	75
c7552	371	97	32	400	68	32	**428**	40	32
s13207	160	188	152	200	148	152	**224**	124	152
s15850	0	468	32	164	304	32	**360**	108	32
s35932	276	151	73	295	132	73	**351**	76	73
s38584	183	262	55	303	142	55	**383**	62	55

TABLE VIII
DIAGNOSIS IMPROVEMENT BY PRI AND POM

CKT.	PRI %Incr. over		POM %Incr. over	
	0.8V	RRI	RRI	PRI
c432	6.6	5.2	12.4	7.2
c880	2.8	2.6	3.4	0.8
c499	9.2	9.2	16	6.8
c1908	12.6	10	21.8	11.8
c1355	4.8	4.6	10	5.4
s1488	23.8	19.2	27.6	8.4
s9234	21.8	21.8	55	33.2
c3540	11.2	11	17.4	6.4
s5378	29.6	29	50	21
c7552	6.2	5.8	11.4	5.6
s13207	24.2	8	12.8	4.8
s15850	**32.8**	**32.8**	**72**	**39.2**
s35932	3.8	3.8	15	11.2
s38584	24.6	24	40	16

"RRI". This clearly demonstrates the useful contribution of test patterns that pass at one voltage setting but fail at another (Partially Passing Patterns) in improving the overall diagnosis accuracy. Next, in 3^{rd} main column of Table VIII we list the relative increase in diagnosis accuracy of POM over: A) "RRI" (2^{nd} main column of Table VII) and B) "PRI" (3^{rd} main column of Table VII). It can be observed that "POM" achieves highest overall diagnosis accuracy for all the circuits, showing upto 72% improvement over "RRI" and 39.2% improvement over "PRI". This points to the success of POM in reducing the callouts catogrized as "CNT" by PRI scheme.

From this experiment, we can observe that the Partially Passing patterns, which are not available at single voltage diagnosis can significantly improve diagnosis accuracy. The time taken by the Multi-Vdd diagnosis algorithm ranges from a second to few minutes, depending on the size of benchmark circuit.

C. Third Experiment

Diagnosis cost is directly affected by the time individual IC spends on the tester while running diagnostic test. For this reason, it is desirable to reduce tester time to achieve low-cost diagnosis with least compromise on diagnosis accuracy. From previous experimental results we have seen that high diagnosis accuracy is achieved by carrying out diagnosis at multiple voltage settings. The aim of this experiment is to evaluate the trade-off between diagnosis cost and accuracy. This is accomplished by investigating the most useful Vdd settings or combination of Vdds, which may yield the desired outcome by omitting tests at a certain voltage setting, thereby reducing diagnosis cost.

The third experiment also uses the complete diagnosis algorithm across different voltage settings. In this case, we carry out diagnosis using 3 Vdd pairs, i.e., (0.8V, 1.0V), (0.8V, 1.2V) and (1.0V, 1.2V). The outcome of this experiment is shown in 2^{nd}, 3^{rd} and 4^{th} main columns of Table IX. From Table IX it can be observed that the diagnosis callout at "0.8V and 1.0V" achieves the highest accuracy in comparison to the other two Vdd pairs, i.e., (0.8V, 1.2V) and (1.0V, 1.2V).

It can be observed that Multi-Vdd diagnosis scheme that uses all Vdd settings (shown in 4^{th} main column of Table VII) achieves slightly better diagnosis accuracy than diagnosis at "0.8V and 1.0V". In terms of the number of exact callouts found by the two, the maximum difference is 12 for all the circuits. On the other hand, the maximum difference in number of exact callouts between diagnosis at all Vdd settings and at "0.8V and 1.2V" is 44 (in case of s15850). The maximum difference is even higher, i.e., 104 (in case of s1488) in comparison to the number of exact callouts at "1.0V and 1.2V". This experiment shows that the tester time, which is a crucial parameter in the diagnosis cost can be reduced by 33% by carrying out diagnosis at "0.8V and 1.0V" only, while achieving very high (close to the overall best) diagnosis accuracy.

D. Fourth Experiment

The purpose of this experiment is to get an insight into diagnosis of hard-shorts in the context of multi-Vdd designs and make appropriate recommendations for diagnosing such defects. The same experimental set up is used for diagnosis as for the first two experiments, but instead of inserting random resistance range for each bridge, resistance value is set to 0 Ohms for all the selected bridges. In this experiment the number of test cases are limited by the number of bridges extracted by the layout tool and listed in Table IV, however designs with more than 500 bridges are restricted by 500 test cases.

TABLE IX
DIAGNOSIS AT DIFFERENT VOLTAGE PAIRS

CKT.	@ 0.8V and 1.0V			@ 0.8V and 1.2V			@ 1.0V and 1.2V		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	**417**	40	43	416	41	43	357	39	104
c880	**440**	24	36	438	26	36	380	22	98
c499	**409**	18	73	408	19	73	364	14	122
c1908	**383**	70	47	376	77	47	325	79	96
c1355	**423**	25	52	419	29	52	378	30	92
s1488	**377**	81	42	375	83	42	285	109	106
s9234	268	95	137	**270**	93	137	218	87	195
c3540	**420**	53	27	416	56	28	352	70	78
s5378	**347**	78	75	344	80	76	279	92	129
c7552	**426**	42	32	**426**	42	32	343	55	102
s13207	215	132	153	**220**	127	153	190	118	192
s15850	**348**	120	32	316	152	32	323	83	94
s35932	**351**	76	73	**351**	76	73	317	74	109
s38584	**371**	74	55	366	79	55	312	80	108

The first part of experiment uses first two steps of the proposed diagnosis algorithm, i.e., Bridge Intersection and Resistance Range Intersection at each voltage setting separately. For every defect these two steps are carried out at each voltage setting independently and results are compiled to compare the diagnosis accuracy at each voltage setting. Table X tabulates the outcome of this experiment in the same fashion as for Table V. It should be noted that the number of exact callouts are in close proximity at all voltage settings for all the circuits other than s13207. Higher number of exact callouts are observed for s13027 at 1.2V than at other voltage settings, as noted in first experiment. The number of empty callouts are also in very close proximity for all the circuits, which suggests that injected defects are in CNT group for defects that are not uniquely identified (EXT group).

The second part of the experiment uses complete diagnosis algorithm across all voltage settings. In this case, the tester response holds the failing patterns over all three voltage settings and corresponding primary output response as used for the second experiment. Table XI tabulates the outcome of this experiment using RRI, PRI and POM. In case of hard-shorts, while comparing the number of EXT callouts with single voltage diagnosis (Table X), PRI shows up to 8.5% improvement (in case of s5378, while comparing with diagnosis at 1.2V) over single voltage diagnosis. However in case of resistive bridges this improvement is up to 32.8%, as shown in Table VIII. Next we analyze the impact of POM in improving the diagnosis accuracy, as it can be seen that POM shows significant improvement over PRI and other techniques, but this improvement should not be entirely attributed to using more than one Vdd settings, as inserted defect may be identified by POM using one of the three Vdd settings.

In the light of this discussion it is fair to conclude that multiple voltage diagnosis shows higher improvement for resistive bridges than for hard-shorts.

TABLE X
DIAGNOSIS CALLOUT FOR HARD SHORTS AT SINGLE VOLTAGE SETTING

CKT.	@ Vdd 0.8V			@ Vdd 1.0V			@ Vdd 1.2V		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	44	3	0	44	3	0	44	3	0
c880	67	2	0	67	2	0	67	2	0
c499	72	13	0	72	13	0	72	13	0
c1908	63	34	1	67	30	1	67	30	1
c1355	71	9	0	72	8	0	72	8	0
s1488	306	127	2	323	110	2	332	101	2
s9234	0	188	35	0	190	33	0	190	33
c3540	286	76	1	287	75	1	287	75	1
s5378	96	199	10	97	199	9	99	197	9
c7552	464	29	7	465	28	7	465	28	7
s13207	63	214	81	63	215	80	140	138	80
s15850	0	491	9	0	491	9	0	491	9
s35932	383	115	2	383	115	2	383	115	2
s38584	381	115	4	383	113	4	382	114	4

TABLE XI
DIAGNOSIS CALLOUT FOR HARD SHORTS AT MULTIPLE VOLTAGE SETTING

CKT.	RRI			PRI			POM		
	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	44	3	0	44	3	0	46	1	0
c880	67	2	0	67	2	0	67	2	0
c499	72	13	0	73	12	0	84	1	0
c1908	67	30	1	67	30	1	87	10	1
c1355	72	8	0	73	7	0	80	0	0
s1488	334	99	2	343	90	2	401	32	2
s9234	0	190	33	15	175	33	147	43	33
c3540	288	74	1	301	61	1	344	18	1
s5378	101	195	9	125	171	9	277	19	9
c7552	467	26	7	469	24	7	487	6	7
s13207	143	136	79	146	133	79	191	88	79
s15850	0	491	9	39	452	9	436	55	9
s35932	383	115	2	383	115	2	477	21	2
s38584	383	113	4	383	113	4	445	51	4

E. Fifth Experiment

The aim of this experiment is to show the impact of test size on diagnosis accuracy. In this experiment, we have used 2000 pseudo-random test patterns (4 times that of test size used in previous experiments) at each Vdd setting. Dictionaries are generated using the same flow as shown in Fig. 8 and explained in section V. The defects are randomly injected and are detectable at least at one voltage setting, which is what an ATPG normally aims to target during test generation.

Table XII shows the results of diagnosis callout at single voltage setting using first two steps of the diagnosis algorithm, i.e., Bridge Intersection and Resistance Range Intersection. As

TABLE XII
DIAGNOSIS CALLOUT FOR RESISTIVE BRIDGES AT SINGLE VOLTAGE SETTING

	@ Vdd 0.8V			@ Vdd 1.0V			@ Vdd 1.2V		
CKT.	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	**422**	78	0	355	100	45	316	97	87
c499	**406**	94	0	362	81	57	309	83	108
c1908	**381**	119	0	333	119	48	285	113	102
c1355	**430**	70	0	388	68	44	340	71	89
s9234	**198**	302	0	164	256	80	137	235	128
c3540	**383**	116	1	320	129	51	281	115	104
s5378	**259**	240	1	204	237	59	168	213	119
c7552	**411**	89	0	334	96	70	286	82	132
s13207	**228**	270	2	193	251	56	187	202	111

TABLE XIII
DIAGNOSIS CALLOUT FOR RESISTIVE BRIDGES AT MULTIPLE VOLTAGE SETTINGS

	RRI			PRI			POM		
CKT.	EXT	CNT	EMT	EXT	CNT	EMT	EXT	CNT	EMT
c432	428	72	0	445	55	0	**473**	27	0
c499	406	94	0	442	58	0	**480**	20	0
c1908	398	102	0	439	61	0	**465**	35	0
c1355	431	69	0	447	53	0	**471**	29	0
s9234	198	302	0	284	216	0	**375**	125	0
c3540	389	111	0	445	55	0	**474**	26	0
s5378	263	237	0	371	129	0	**450**	50	0
c7552	412	88	0	441	59	0	**467**	33	0
s13207	246	254	0	303	197	0	**355**	145	0

expected, for all the circuits shown in Table XII the diagnosis accuracy has improved in comparison to results shown in Table V, primarily due to increased test size.

In the second part of the experiment, complete diagnosis algorithm is used and results are shown in Table XIII. As can be seen from Table XIII multiple voltage diagnosis shows significant increase in the number of Exact callouts in comparison to single voltage diagnosis (shown in Table XII). For PRI step, the %age increase in the number of Exact callouts is up to 22.4% (as for s5378) over single voltage ($0.8V$) diagnosis. These results are further improved by the POM step, which shows up to 38.2% increase (as for s5378) in the number of Exact callouts in comparison to single voltage diagnosis.

The key observation of this experiment is that better diagnosis can be achieved with a large (high resolution) ATPG test set. It should be noted that for single voltage diagnosis highest accuracy is achieved at the lowest ($0.8V$) voltage setting, which can be further improved by multiple voltage diagnosis. In [20], it was shown that for 8 out of 12 multi-Vdd designs, 100% bridge defect coverage can't be achieved at single voltage setting. The study shows that most amount of bridge defect resistance is covered by tests at lowest Vdd setting ($0.8V$), however for 100% defect coverage it is essential to generate tests at higher Vdd settings. The proposed multi-Vdd diagnosis approach capitalizes on these findings and achieves overall high diagnosis accuracy by using multiple voltage settings.

VI. CONCLUSION

Low power ICs employing multiple-Vdd designs are commonly used in hand-held devices. Developing effective diagnosis capabilities for such ICs is important for today's competitive mobile electronics. This work is based on cause-effect diagnosis scheme using a simple pass/fail dictionary to minimize memory storage, however conclusions drawn through the experiments reported in this work are expected to hold if a complete dictionary that uses complete faulty responses or if an effect-cause diagnosis procedure [1], [13] is used. This paper has addressed for the first time diagnosis of multiple-Vdd ICs and proposed a novel multi-Vdd diagnosis algorithm to exploit the information from all voltage settings to achieve higher diagnosis accuracy. This work provides a proof-of-concept that Multi-Vdd diagnosis can improve diagnosis accuracy over single-Vdd diagnosis. In addition, it recommends a way to reduce diagnosis cost by carrying it out at ($0.8V$, $1.0V$) Vdd settings and still achieve high diagnosis accuracy. The improved diagnosis accuracy justifies the usage of test patterns at more than a single-Vdd setting. Lastly, it shows experimental results to establish that Multi-Vdd diagnosis is more effective for resistive bridges than for hard-shorts. Our future work includes integrating other real defects using their respective advanced fault models, and utilizing recently reported approaches [8], [9] to make it a more robust diagnostic suite. Furthermore, in deep submicron technology process variation has increased impact on effectiveness of test quality, therefore its impact on diagnosis accuracy will also be investigated.

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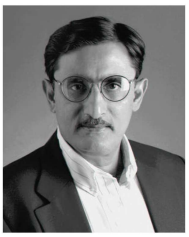

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