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Letter

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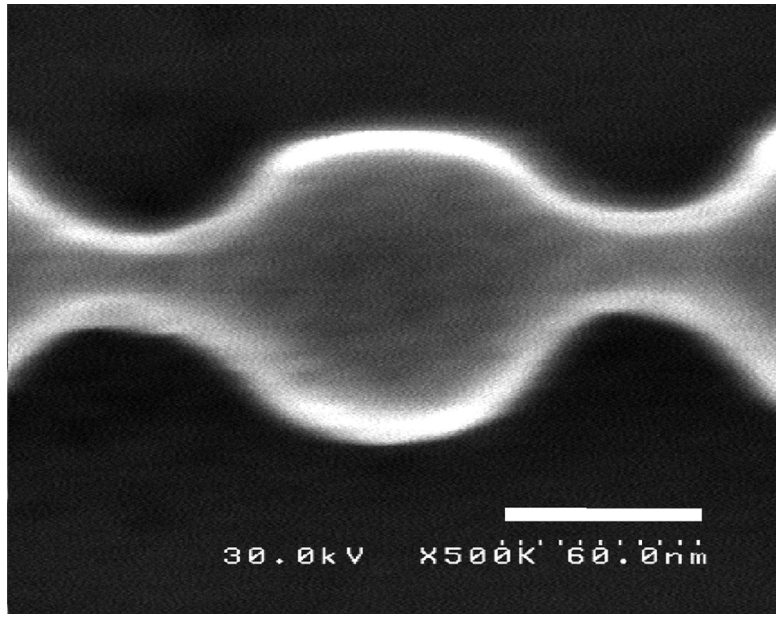


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# Silicon-on-Insulator-Based Radio Frequency Single-Electron Transistors Operating at Temperatures above 4.2 K

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## ABSTRACT

**A radio frequency single-electron transistor (RF-SET) based on a silicon-on-insulator (SOI) substrate is demonstrated to operate successfully at temperatures above 4.2 K. The SOI SET was fabricated by inducing lateral constrictions in doped SOI nanowires. The device structure was optimized to overcome the inherent drawback of high resistance with the SOI SETs. We performed temperature variation measurements after five thermal cyclings of the same sample to 4.2 K and found that the single-dot device transport characteristics are highly stable. The charge sensitivity was measured to be 36 $\mu e_{rms}$ $Hz^{-1/2}$ at 4.2 K, and the RF-SET operation was demonstrated up to 12.5 K for the first time. This work is an important prerequisite to realizing operation of RF-SETs at noncryogenic temperatures.**

In the past 15 years, single-electron devices (SEDs) based on silicon-on-insulator (SOI) substrates have been widely studied for potential applications in complementary metal oxide semiconductor (CMOS) and quantum information technology,[1−4] mainly due to their room-temperature operation, charge offset stability, and compatibility with CMOS technology.[5,6] In particular, silicon SEDs are actively studied for qubit,[7,8] nanoelectromechanical systems (NEMS),[9] and logic and metrology applications.[3,4] To accomplish successful qubit and NEMS measurements, high sensitivity and wide bandwidth readout are required. Even though the single-electron transistor (SET) is the ultimate charge-sensitive device available to date, the SET resistance and the lead capacitance at the output restrict the measurement bandwidth to a few kilohertz or less. Rather than carrying out standard voltage and current measurements, the so-called radio frequency single-electron transistor (RF-SET) overcomes this low-frequency limitation by measuring the radio frequency waves reflected[10] (or transmitted[11]) from (or across) the SET using an LC-resonant circuit for impedance matching.

In RF-SET measurements, the high resistance of the SET has to be matched to the characteristic impedance (50 Ω) of a coaxial cable by a resonance circuit. High-frequency operation is possible only if this matching is effective; otherwise, RF signal coupling between the SET and the RF circuit will be degraded severely.[12] Thus, lowering the resistance of SETs is crucial to realize RF-SET operation.[3,14] Unfortunately, the resistance of SOI-based SETs is on the order of megaohms. To reduce the SET resistance, we initially explored dual recess structured silicon channel SETs, where two extra side gates were fabricated in the recessed region to tune the SET resistance.[15] However, it was found that, depending on the fabrication conditions, multiple dots are formed in the channel. By further optimizing the geometrically defined single-dot SET structure, the SET resistance was reduced to 500 kΩ. This single-dot SET structure was adopted for the RF-SET measurement.

Operation of a RF-SET based on two-dimensional electron gas (2-DEG) in intrinsic silicon at 100 mK has been reported.[16] However, 2-DEG system operation is limited to very low temperatures. SOI-based SETs offer a promising approach to high-temperature operation.[5] In this paper, we report the first successful operation of RF-SET up to 12.5 K. We have measured the best charge sensitivity of 36 $\mu e$ $Hz^{-1/2}$ at 4.2 K. The shot noise characterization of the RF-SET has been presented, which is used to extract the gain and noise temperature of the system. In addition, we explore

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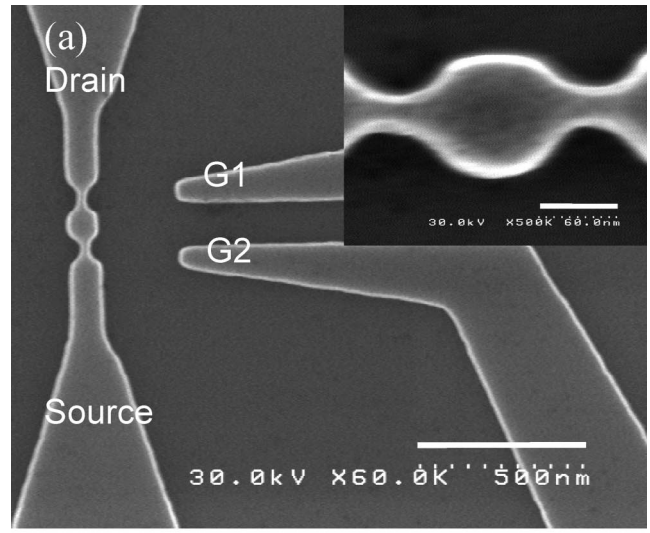
the potential applications of the high-temperature RF-SET in silicon detector readout circuits, which will benefit numerous research efforts.

A SOI wafer with original thickness of 100 nm and buried oxide (BOX) layer thickness of 200 nm was used to fabricate this device. Initially, the substrate was thermally oxidized and a phosphorus ion implanted ($\sim 10^{19}$ cm$^{-3}$). After ion-implantation, a drive-in process at 1100 °C was conducted to activate the dopants. The oxide layer that protected the device from damage during implantation was removed after the drive-in process. The substrate was thermally oxidized again to reduce the thickness of the SOI to ~40 nm. A single-dot structure was patterned on the substrate using high-resolution electron beam lithography. Electron cyclotron resonance-reactive ion etching (ECR-RIE) was conducted to transfer the lithographically defined pattern to the SOI layer. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI. A scanning electron microscopy (SEM) image of a typical fabricated laterally constricted SET is shown in Figure 1a. The bright regions indicate the SOI layer, and the dark regions indicate the BOX layer of the substrate. The inset shows an enlargement of the dot region, where the length and width of the constriction region are approximately 40 and 30 nm, respectively. The lithographically defined constrictions in the silicon channel act as tunnel barriers resulting from bandgap enlargement in the narrower regions.[17]

A He$^4$ physical property measurement system was used to carry out the direct current (DC) and radio frequency (RF) measurements. A schematic of the measurement setup is shown in Figure 1b. The high resistance of the silicon SET is matched to the 50 Ω characteristic impedance coaxial line by a LC resonant circuit. The drain of the SET was connected to a chip inductor of 560 nH by a bonding wire, and the source was grounded. The resonator capacitance is formed by the stray capacitance of the bond pad. The stray capacitance, $C_{pad}$, was determined to be ~0.44 pF on the basis of the resonant frequency measurement with a real-time chip inductor equivalent circuit model.[18] An RF carrier signal was applied to the drain of the SET through the directional coupler. A 30 dB directional coupler was used to direct the reflected signal from the SET to the low-noise cryogenic amplifier at low temperature. The amplified signal was fed to the spectrum analyzer for further measurements.

A DC source−drain voltage was introduced to the SET by a bias tee. This made it possible to independently measure the DC of the SET. The SET gate was connected directly to a low-frequency line to feed DC and AC signals. The sensitivity of the RF-SET was measured by applying a small-voltage signal with frequency $f_m$ together with DC voltage to the gate. The reflected RF carrier amplitude is modulated according to the SET conductance, which is dependent on the gate signal. The modulated RF signal, which is amplified by the low-temperature cryogenic amplifier, was fed directly into an R&S FSU spectrum analyzer. Amplitude-modulated RF carrier, $f_c$, along with the sidebands, $f_c - f_m$ and $f_c + f_m$, appeared together in the analyzer. The charge sensitivity of



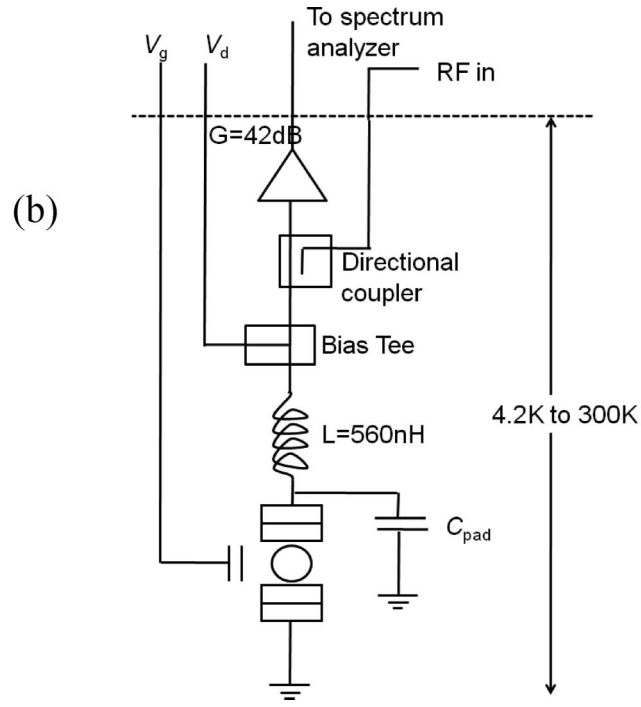




**Figure 1.** (a) SEM image of the fabricated silicon SET (scale bar, 500 nm). Inset: Zoomed-in SEM image of the dot region (scale bar, 60 nm). (b) Schematic of the RF and DC measurement setup.

the RF-SET is calculated[13] by $\delta q = \Delta Q(2\mathrm{RBW})^{-1/2} \times 10^{-\mathrm{SNR}/20}$, where $\Delta Q$ is the value of the gate signal measured in electrons (rms), RBW is the resolution bandwidth used for the spectrum analyzer, and SNR is the signal-to-noise ratio of the one of the side bands, measured in decibel (dB).

A contour plot of the SET drain current ($I_d$) as a function of drain voltage ($V_d$) and gate G1 voltage ($V_{g1}$) is shown in Figure 2a, with the other gate ($V_{g2}$) kept at 2 V, at 5 K. A virtually uniform oscillation period indicates that a single charging dot is responsible for the Coulomb oscillation. It can be noticed that there is a clear periodic lifting blockade for gate voltages above 1 V. Nonlifting of periodic blockade

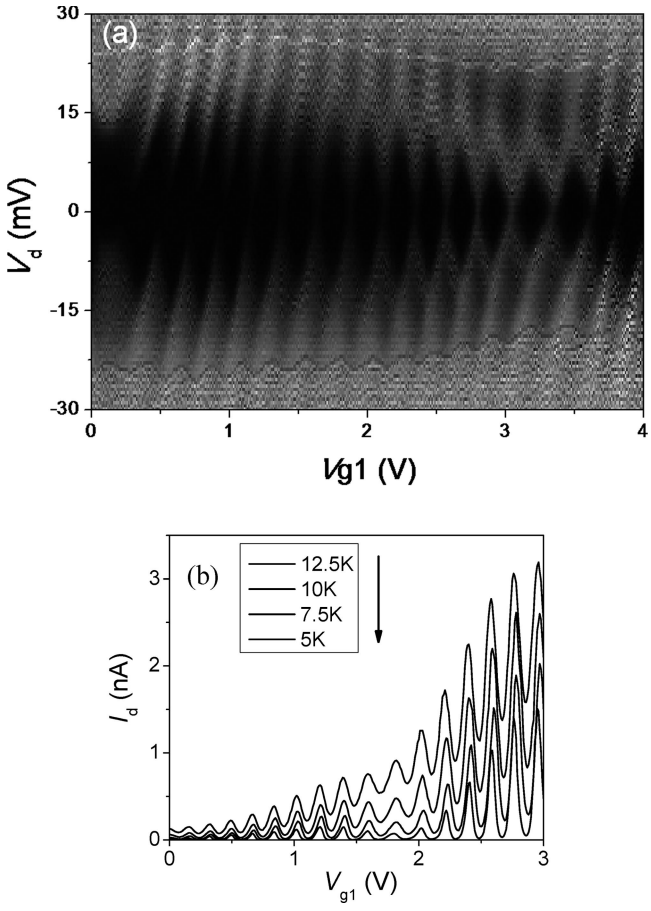



**Figure 2.** (a) Differential conductance plot of the SET as a function of drain voltage ($V_d$) and gate G1 ($V_{g1}$) voltage at 5 K. Gate G2 was kept at 2 V. (b) Temperature dependence of the drain current as a function of gate G1 ($V_{g1}$) voltage for the drain voltage of 5 mV. Gate G2 was kept at 0 V.

for gate voltages less than 1 V is attributed to the formation of additional multiple tunnel junctions (MTJs) in the narrow lateral constriction regions due to the potential induced by the random dopants. Such uncontrolled MTJs can be avoided by making the constrictions extremely short, with low surface roughness. For a detailed discussion of the origin and the method to overcome MTJs induced by random dopants, see ref 19.

As the gate is positioned in the channel constriction region, higher gate voltage influences the tunnel junction resistance. A Coulomb staircase can be clearly seen for gate voltages more than 2.5 V, which occurs due to asymmetric tunnel junction resistance. This physical phenomenon clearly indicates that the tunnel junction is defined by the channel constriction. The total resistance of the SET ($R_{SET}$) was calculated to be 547 kΩ from the linear slope region of the $I_{ds}-V_{ds}$ characteristics. The charging energy $E_c$ was 7 meV (average over wide gate voltage range), corresponding to 81 K and a total SET-island capacitance $C_\Sigma$ of 11.44 aF. The Coulomb oscillation periods were 0.22 and 0.26 V for gates G1 and G2, respectively. The corresponding gate capacitances are 0.73 and 0.62 aF. The nearly equivalent values of the gate capacitances confirms that the island is located symmetrically between gates G1 and G2.

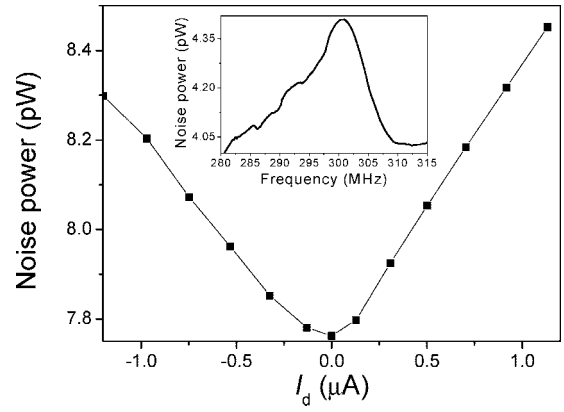



**Figure 3.** Output noise power of the whole measurement system as a function of current through the SET. The line connecting different points is to guide the eye. The inset shows measured shot noise power for 1.5 $\mu$A DC current through the SET. This curve was obtained by subtracting the background noise.

If we assume the central island to be spherical in shape with a radius $r$, embedded in a dielectric material, the capacitance is given by $C_\Sigma = 4\pi\epsilon_r\epsilon_0 r$, where $\epsilon_r$ is the dielectric constant of the dielectric material. By substituting $C_\Sigma$ and $\epsilon_r = 3.9$ for $SiO_2$, the dot diameter was calculated to be 53 nm. This value is in good agreement with the lithographically defined dimensions of the region between the two channel constrictions. From these data, it can be concluded that the formation a single dot, as expected for the lateral constrictions, is responsible for the observed Coulomb blockade oscillation characteristics.

To check the stability of the SET transport characteristics, temperature variation measurements were carried out. The temperature dependence of the SET drain current as a function of the gate G1 voltage is shown in Figure 2b for $V_{g2} = 0$ V and $V_d = 5$ mV. From this plot, it can be seen that conductance peak positions do not vary with temperature. This confirms the stable nature of the measured transport characteristics of the laterally constricted single-dot SET and clearly rules out disorder/surface roughness-induced dots in the channel. As the gate is positioned across the constricted region, increasing the gate voltage pulls down the potential barrier. This leads to an increase in the drain with the gate voltage ($V_{g1}$).[20] This temperature variation measurement was by temperature-cycling the same sample to 4.2 K five times. During the storage period, the sample was kept at room temperature and atmospheric pressure.

To characterize the tank circuit parameters, a DC current of 1.5 $\mu$A was applied through the SET, and the resulting shot noise was measured with a spectrum analyzer.[21] The inset in Figure 3 shows the measured shot noise power as a function of frequency. The useful bandwidth (half-width at half-maximum, HWHM[21]) was found to be 6.5 MHz. The noise temperature and gain of the whole system were evaluated from the noise power measurement as a function of the current through the SET. Figure 3 shows the output noise power of the system as a function of current through the SET. The shot noise of the SET is amplified by the cryogenic amplifier, which can be noticed from the slope of the linear parts. The total gain of the system, extracted from

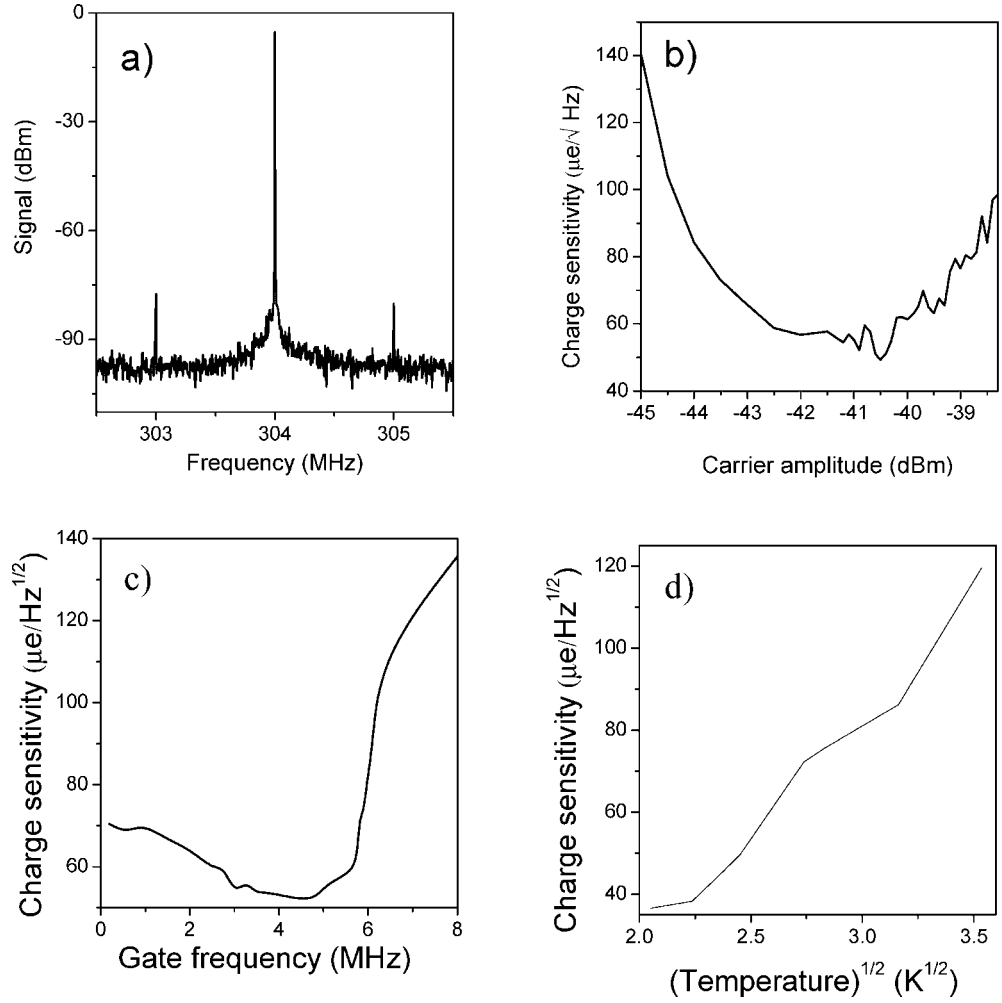



**Figure 4.** (a) Reflected power as a function of carrier frequency. The carrier is amplitude-modulated by the SET, generating two side bands for a gate signal of 0.025 $e_{rms}$ and 1 MHz (carrier amplitude was kept at −42 dBm). (b) Charge sensitivity as a function of carrier amplitude at the resonant circuit. (c,d) Charge sensitivity for the gate signal of 0.025 $e_{rms}$ and 1 MHz and carrier amplitude of −42 dBm at the resonant circuit as a function of (c) gate frequency and (d) temperature.

this slope, was found to be 49 dB. The noise temperature of the whole system was extracted from the crossing point of the linear asymptotes, which was 7.0 K.

Figure 4a shows the two sidebands of the amplitude-modulated carrier for a gate signal with amplitude of 0.025 $e_{rms}$ and 1 MHz at 5 K. The charge sensitivity as a function of carrier amplitude at the resonant circuit at 5 K is shown in Figure 4b. The RF carrier power coupling between the SET and the RF part of the measurement setup is degraded due to the large impedance mismatch between them.[22,23] On the basis of the RF-SET *S*-parameter formalism reported in ref 23, the ratio of power coupled between the SET and the RF part of the measurement setup ($K$) was found to be 0.08. The lower value of $K$ is due to the higher resistance of the SET (547 kΩ). [In the case of $R_{SET} = 54.7$ kΩ, $K$ was found to be 0.5 for the same resonant circuit parameters.] Two major limitations result from the lower value of $K$: a larger carrier power is needed to bias the SET, and the reflected signal is weakly coupled to the outside of the resonant circuit. The weak coupling of the reflected signal to the RF part of the measurement setup leads to low charge sensitivity. However, fabrication of a low-resistance silicon SET could be achieved by using the SOI 2-DEG-based SET[24] or SOI-based point-contact channel SET with low parasitic resistance.[25]

The RF-SET sensitivity as a function of gate frequency at 5 K is shown in Figure 4c. A sharp degradation of the charge sensitivity is observed at an applied gate frequency of approximately 6 MHz and above. This cutoff frequency is consistent with the HWHM bandwidth of the resonant circuit. Significantly low charge sensitivity below 2 MHz is attributed to the $1/f$ noise. Figure 4d shows the RF-SET sensitivity as a function of temperature. The best charge sensitivity was calculated to be 36 $\mu e\ Hz^{-1/2}$ at 4.2 K. It can be noticed that the charge sensitivity degrades as a function of the square root of the temperature. This is in good agreement with the theoretical charge sensitivity developed by Korotkov et al.[26] Thus, the successfully operation of RF-SETs based on silicon SETs up to 12.5 K is critical for the operation of RF-SETs at noncryogenic temperatures.

Silicon detectors are widely used as tracking detectors in high-energy particle physics, astronomy, and medical fields. In X-ray imaging, they are also used in crystallography and

in medical imaging and mechanical engineering for alignment. They have also found applications in the detection of photons in medicine and astrophysics.[27] However, the charge sensitivity of the readout electronics often limits the sensitivity of these detectors. The readout electronics require high charge sensitivity and wide bandwidth. High sensitivity and wide bandwidth can be realized by the reported RF-SETs using Al/$AlO_x$/Al tunnel junctions,[13] GaAs quantum dots,[11] semiconducting nanowires,[28] and carbon nanotubes.[29] However, these RF-SETs are limited to low-temperature operation.

With the reported silicon SET low resistance of 114 k$\Omega$[25] and optimum pad capacitance of 0.2 pF, the maximum achievable bandwidth—the theoretical limit set by the Bode−Fano criterion[22]—is 60 MHz. This bandwidth can be further improved by reducing the SET resistance and using on-chip inductor and capacitor matching circuits to reduce the pad capacitance. The lowest time limitation set by the silicon detector is 30 ns,[27] which can be realized with the above-mentioned bandwidth limitation for silicon SET. Other important requirements of the silicon detector readout electronics are high-temperature operation, charge offset stability, and long-term drift stability. These conditions have only been realized by the SOI-based SETs.[5,6,30] Thus, silicon RF-SETs will be the only devices to meet all these requirements to realize highly sensitive silicon detector readout electronics. The high-temperature silicon RF-SET will make it possible to realize high-sensitivity pixel detectors that will benefit many other research applications as well.

We have reported SOI-based RF-SETs operating at temperatures greater than 4.2 K for the first time. This clearly indicates that RF-SETs with high sensitivity and wide bandwidth can be realized at noncryogenic temperatures, which will pave the way for realization of high-sensitivity silicon detectors and pixel detectors for use in many other experiments. The best measured charge sensitivity was 36 $\mu e_{rms}$ $Hz^{-1/2}$ at 4.2 K, which was limited by the high resistance of the silicon SET. The resistance of the SET can be reduced by optimizing the device structure, which will improve the sensitivity further.

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