Design Optimization of NEMS Switches for Suspended-Gate Single-Electron Transistor Applications

Benjamin Pruvost, *Student Member, IEEE*, Ken Uchida, *Member, IEEE*, Hiroshi Mizuta, *Member, IEEE*, and Shunri Oda, *Member, IEEE*

Abstract—The operation of nanoelectromechanical switches is investigated through simulation. A simple methodology based on a 1-D lumped model taking account of the Casimir effect is first proposed to determine a low-voltage actuation window for conventional cantilevers. Results show good agreement with 3-D simulation and prove to be helpful for systematic design. The conventional cantilever shape is then optimized to a cross-like design that is fully studied in a 3-D environment. Static and dynamic behaviors as well as effect of the oxide layer thickness are investigated with a view to suspended-gate single-electron transistor applications. The proposed structure successfully combines low actuation voltage and low power consumption, and it is shown that the switching speed is the limiting factor for the considered applications.

Index Terms—1-D and 3-D modeling, cantilever switch, movable gate, nanoelectromechanical system (NEMS), single-electron transistor (SET).

I. INTRODUCTION

NLIKE conventional electronic devices, nanoelectrome-chanical systems (NEMSs) can be potentially manufactured to high tolerances on the scale of nanometers using CMOS-compatible infrastructures. They also exhibit superb performances in terms of power savings and new functionality, providing an ideal platform to build multifunctional nanoscale ICs. Therefore, hybrid devices coupling single-electron transistors (SETs) to NEMS have recently drawn much attention for their promised experimental insight into quantum aspects of mechanical systems as much as for their potential applications in communication and information technology. Some groups exploited the ultrahigh sensitivity of the SET to read out the motion of a capacitively coupled nanomechanical resonator,

Manuscript received June 12, 2008; revised November 14, 2008. First published December 12, 2008; current version published March 6, 2009. The review of this paper was arranged by Associate Editor B. Nelson.

B. Pruvost is with the Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, Tokyo 152-8552, Japan (e-mail: benjamin@neo.pe.titech.ac.jp).

K. Uchida and S. Oda are with the Quantum Nanoelectronics Research Center and the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan, and also with the Solution Oriented Research for Science and Technology (SORST), Japan Science and Technology (JST), Saitama 332-0012, Japan (e-mail: uchidak@pe.titech.ac.jp; soda@pe.titech.ac.jp).

H. Mizuta is with the School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, U.K., and also with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan. He is also with the Solution Oriented Research for Science and Technology (SORST), Japan Science and Technology (JST), Saitama 332-0012, Japan (e-mail: hm2@ecs.soton.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2008.2010453

managing to approach its quantum limit [1], [2], while another group proposed an SET whose island is located at the top of a free-standing silicon nanopillar shuttling between the source and the drain [3]. Finally, a notable suspended-gate architecture, which would enable to switch the SET gate capacitance between two values, has been suggested in [4] and [5], and we preliminary studied the *static* actuation of several double-clamped gate structure in a previous work [6]. Such movable gate structure may be a proper candidate to realize the variable capacitance SET needed in [7] in order to cope with the random background charge problem faced by the SET, and could also be used as threshold gate to build neural network or analog-to-digital flash converter [5]. The purpose of this paper is to optimize the design of NEMS switches, and in particular, for suspended-gate SET application. In the first part, we study the behavior of conventional NEMS cantilevers through a 1-D model taking account of the Casimir force, and we propose a simple methodology to determine a low-voltage actuation window for systematic design. In the second part, we focus on the design optimization of the switch in a 3-D environment for suspended-gate SET application. We study both its static and dynamic behaviors, and also discuss the merits and the disadvantages of the overall device in terms of speed and energy consumption as compared to current MOSFETs.

II. CONVENTIONAL CANTILEVER SWITCHES DESIGN

A. Principle and 1-D Analysis

Cantilever switches are basic building blocks in the NEMS platform: an electrode, the cantilever, is suspended over a fixed electrode, and as the voltage applied between these two electrodes is increased, the spacing between them continuously decreases until the electrostatic force overwhelms the elastic force of the spring resulting in a sudden snap down of the suspended electrode. This effect, called the pull-in effect, occurs at a voltage defined as the pull-in voltage $V_{\rm PI}$. Although simulation basically authorizes any dimensions for the cantilever, some theoretical constraints have to be imperatively respected for the structure to be viable. In particular and in contrast to micromechanical switches, the Casimir force is expected to be significant at the nanoscale [8] since it may overcome elastic restoring actions in the device and lead to the cantilever's sticking during the fabrication process, i.e., even without applying any voltage. The maximal length corresponding to the beam such that it does not stick to the substrate is called the detachment length and is an

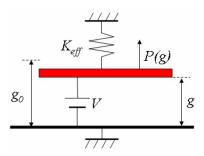


Fig. 1. Schematic of the cantilever 1-D lumped model.

essential design parameter [9], [10]. Therefore, in this part, we purpose to determine a low-voltage (<1 V) actuation window for conventional cantilevers that accounts for this constraint in order to help with the systematic design of NEMS switches. We will also see how this simple approach helps getting insight to the cantilever behavior.

In order to simplify the methodology, we only consider the 1-D lumped model, where the cantilever is approximated by a single rigid parallel-plate capacitor suspended above a fixed ground plate by a spring (see Fig. 1). The Young's modulus, length, and thickness of the cantilever are, respectively, denoted as E, L, and t. The single degree of freedom is the gap g (initially denoted g_0) between the two plates and is defined at the cantilever tip. The net upward pressure P(g) on the free plate is the sum of the electrostatic attractive pressure $\epsilon_0 V^2/2g^2$, where V is the voltage applied between the plates, the attractive Casimir force per unit area $\pi^2 \hbar c/240g^4$, and the spring restoring force $K_{\text{eff}}(g_0 - g)$, where $K_{\text{eff}} = 2Et^3/3L^4$ is the effective spring constant having units of newtons per cubic meter and derived from the small-deflection mechanical solution for the maximum displacement. In static equilibrium, we may write

$$P(g) = K_{\text{eff}}(g_0 - g) - \frac{\epsilon_0 V^2}{2g^2} - \frac{\pi^2 \hbar c}{240g^4} = 0.$$
 (1)

The equilibrium is stable if dP/dg < 0 and critical when

$$\frac{dP}{dq} = -K_{\text{eff}} + \frac{\epsilon_0 V^2}{q^3} + \frac{\pi^2 \hbar c}{60q^5} = 0.$$
 (2)

Now, contrary to what is usually done, we will not try to derive the expression of the pull-in voltage, but conditions on the cantilever's parameters (material and dimensions) to get a given pull-in voltage.

Writing (1) and (2) at the critical pull-in gap $g_{\rm PI}$ and rearranging them, we may, for example, get the following system of equations:

$$\frac{\pi^2 \hbar c}{g_{\rm PI}^2} \left(\frac{g_0}{60} - \frac{g_{\rm PI}}{48} \right) + \epsilon_0 V_{\rm PI}^2 \left(g_0 - \frac{3}{2} g_{\rm PI} \right) = 0 \tag{3}$$

$$K_{\text{eff}} = \frac{2Et^3}{3L^4} = \frac{\epsilon_0 V_{\text{PI}}^2}{g_{\text{PI}}^3} + \frac{\pi^2 \hbar c}{60g_{\text{PI}}^5}.$$
 (4)

Now, solving (3) for a given pull-in voltage $V_{\rm PI}$ (in our case $V_{\rm PI}=0$ V and $V_{\rm PI}=1$ V), and injecting the calculated $g_{\rm PI}$ in

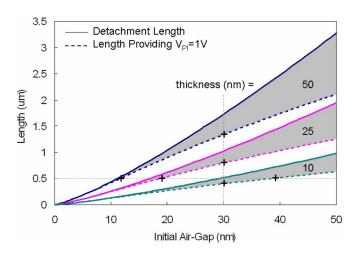


Fig. 2. Detachment length (solid line) and length providing 1 V pull-in voltage (dotted line) as a function of the initial air gap for aluminum cantilevers with various thicknesses. The gray areas show the <1 V actuation windows. Other areas represent either not viable or >1 V actuation switches.

(4), we obtain a relation between the cantilever's parameters that lead to this given pull-in voltage.

Notably, we can obtain an exact expression for the detachment length, which corresponds to $V_{\rm PI}=0~{\rm V}$

$$L_{\text{max}} = \frac{4}{5} g_0 \sqrt[4]{\frac{32Et^3 g_0}{\pi^2 \hbar c}}.$$
 (5)

This result is slightly different from the one obtained in [10], because we used the exact value of $g_{\rm PI}=(4/5)g_0$ at $V_{\rm PI}=0$ V, instead of the well-known, and in this case, approached value $g_{\rm PI}=(2/3)g_0$.

Note that for a fixed-fixed beam, by replacing K_{eff} with its actual value $32Et^3/L^4$, we would obtain

$$L_{\text{max}} = \frac{4}{5} g_0 \sqrt[4]{\frac{1536Et^3 g_0}{\pi^2 \hbar c}}.$$
 (6)

B. Low-Voltage Actuation Window for Cantilever Switches

By graphically combining the relations linking the parameters for $V_{\rm PI}=0$ V and $V_{\rm PI}=1$ V, we can visualize the so-called low-voltage actuation window for the cantilever. Gray areas in Fig. 2 show, for example, the theoretical range of lengths and initial air gaps providing a pull-in voltage lower than 1 V in the case of an aluminum cantilever. Also, for a given thickness, the area above the detachment length solid line shows dimensions leading to a nonviable cantilever, while the area below the 1 V pull-in voltage dotted line shows dimensions leading to a pull-in voltage higher than 1 V. As expected, the detachment length decreases with the thickness and the initial air gap. It is also interesting to note that the smaller the initial air gap, the less freedom we have in the choice of the cantilever's length in the current nanoscale resolution.

Fig. 2 may be used to determine not only the viability of a cantilever, but also the influence of other factors, independently of the static behavior. For example, let us study the influence of the thickness on the switching time. First, Fig. 2 is used to

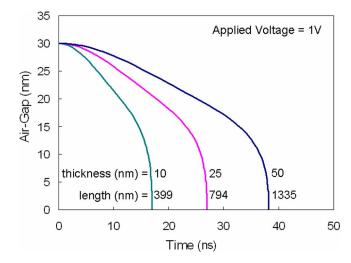


Fig. 3. Dynamic pull-in of three cantilevers having same initial air gap (30 nm) and same pull-in voltage (1 V) but different length and thickness.

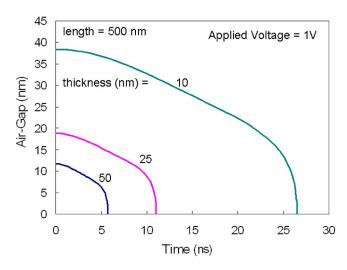


Fig. 4. Dynamic pull-in of three cantilevers having same length (500 nm) and same pull-in voltage (1 V) but different initial air gap and thickness.

determine two sets of three cantilevers of different thicknesses (10, 25, and 50 nm) having the same pull-in voltage (1 V) and:

- 1) same initial air gap (30 nm) but different lengths (set (1) located on the vertical dotted straight line in Fig. 2);
- 2) same length (500 nm) but different initial air gaps (set (2) located on the horizontal dotted straight line in Fig. 2).

Then, noting the density ρ of the material, we solve the dynamic equation of motion for each cantilever

$$\rho t \frac{d^2 g}{dt} = P(g) = K_{\text{eff}}(g_0 - g) - \frac{\epsilon_0 V^2}{2q^2} - \frac{\pi^2 \hbar c}{240q^4}.$$
 (7)

Note that we neglect the damping effect of the air layer underneath the cantilever, as it will be discussed later.

Figs. 3 and 4 show the switching times of set (1) and set (2), respectively. For a given initial air gap, the thinner and the shorter the cantilever, the faster the switching. On the contrary, for a given length, the thicker the cantilever and the smaller the

initial air gap, the faster the switching. It is important to note that all these cantilevers do have the same static behavior, as they have the same pull-in voltage. However, this study shows that their dynamic behavior is quite different, and that the thickness effect is not that straightforward. Furthermore, combining Figs. 3 and 4, we can see that at constant thickness, the switching time decreases when scaling down the cantilever, i.e., when moving toward 0 on an equipotential line for a given thickness in Fig. 2. We will see later how these results may help with the design optimization of the cantilever.

Obtaining this kind of figure from the 3-D simulation is very laborious and difficult, if not impossible. Nevertheless, in order to confirm at least partially the validity of our approach, we estimated the detachment length and the length leading to a 1-V pull-in voltage for several parameters by using the finite-element method (FEM) provided by the 3-D simulator COMSOL [11]. Since the Casimir force is not implemented in this software, we added it manually as an external pressure on the cantilever with the same expression as in the 1-D model. Then, for given cantilever's parameters (material, width, thickness, and initial air gap), we performed extensive simulations by varying the length until getting the one that leads to a 0-V or 1-V pull-in voltage. The data calculated for cantilevers made of aluminum and polysilicon are, respectively, gathered in Tables I and II together with the ones estimated from the 1-D lumped model. Whatever the material and the dimensions, the 1-D lumped model shows surprisingly stable and good agreement with the 3-D calculation for the detachment length (within 10%). This stability is due to the fact that the only force taken into account then is the Casimir force, which has the same expression as in the 1-D model. Therefore, we may suppose that this stable relative error (around 9%) mainly reflects the difference in the mechanical modeling between the 1-D simple spring constant K_{eff} and the more realistic 3-D FEM. Since the width does not have any significant influence on the detachment length, we can possibly include a corrective factor in (5) corresponding to this error to derive a more accurate (empirical though) expression for the detachment length expression

$$L_{\text{max}} = \frac{4}{0.91 \times 5} g_0 \sqrt[4]{\frac{32Et^3 g_0}{\pi^2 \hbar c}}.$$
 (8)

It is also interesting to note that the 1-D model always underestimates the actual detachment length, which is an important requirement for its experimental reliability.

When calculating the length leading to a 1-V pull-in voltage, the 1-D model shows more variable results because the 3-D modeled electric field is much more complex than the 1-D simple expression. However, the agreement is still acceptable (within 15%) and suggest that our approach is legitimate for the range of dimensions and materials used in our simulations.

III. OPTIMIZATION FOR SUSPENDED-GATE SET APPLICATIONS

A. Principle of the Suspended-Gate SET

The principle of the suspended-gate SET is depicted in Fig. 5: it combines in a top-down architecture an NEMS switch and a conventional SET. The NEMS switch is composed of two

TABLE I

COMPARISON OF THE DETACHMENT LENGTHS AND THE LENGTHS PROVIDING 1 V PULL-IN VOLTAGE CALCULATED BY THE 1-D LUMPED MODEL AND BY THE 3-D FEM FOR SEVERAL ALUMINUM CANTILEVERS

Aluminum Cantilever		$g_0 = 20 \text{ nm}$		$g_0 = 50 \text{ nm}$	
		L_{max}	L_{1V}	L_{max}	L_{1V}
t = 10 nm	1D	311 nm	268 nm	979 nm	629 nm
	w = 50 nm	344 nm (9.6%)	284 nm (5.6%)	1084 nm (9.7%)	734 nm (14.3%)
	w = 100 nm	342 nm (9.0%)	302 nm (11.3%)	1076 nm (9.0%)	649 nm (3.1%)
t = 25 nm	1D	619 nm	533 nm	1947 nm	1250 nm
	w = 50 nm	680 nm (9.0%)	608 nm (12.3%)	2144 nm (9.2%)	1414 nm (11.6%)
	w = 100 nm	676 nm (8.4%)	588 nm (9.4%)	2137 nm (8.9%)	1320 nm (6.1%)
t = 50 nm	1D	1040 nm	896 nm	3274 nm	2102 nm
	w = 50 nm	1141 nm (8.8%)	940 nm (4.7%)	3586 nm (8.7%)	2190 nm (4.0%)
	w = 100 nm	1132 nm (8.1%)	1036 nm (13.5%)	3586 nm (8.7%)	2205 nm (4.7%)

TABLE II

COMPARISON OF THE DETACHMENT LENGTHS AND THE LENGTHS PROVIDING 1 V PULL-IN VOLTAGE CALCULATED BY THE 1-D LUMPED MODEL AND BY THE 3-D FEM FOR SEVERAL POLYSILICON CANTILEVERS

Polysilicon Cantilever		$g_0 = 20 \text{ nm}$		$g_0 = 50 \text{ nm}$	
		L_{max}	L_{1V}	L_{max}	L_{1V}
t = 10 nm	1D	383 nm	329 nm	1204 nm	773 nm
	w = 50 nm	420 nm (8.8%)	367 nm (10.4%)	1319 nm (8.7%)	868 nm (10.9%)
	w = 100 nm	420 nm (8.8%)	365 nm (9.9%)	1317 nm (8.6%)	836 nm (7.5%)
t = 25 nm	1D	761 nm	655 nm	2393 nm	1537 nm
	w = 50 nm	833 nm (8.6%)	723 nm (9.4%)	2622 nm (8.7%)	1765 nm (12.9%)
	w = 100 nm	834 nm (8.7%)	740 nm (11.5%)	2621 nm (8.7%)	1763 nm (12.8%)
t = 50 nm	1D	1280 nm	1101 nm	4025 nm	2585 nm
	w = 50 nm	1400 nm (8.6%)	1114 nm (1.2%)	4404 nm (8.6%)	2640 nm (2.1%)
	w = 100 nm	1402 nm (8.7%)	1274 nm (13.6%)	4405 nm (8.6%)	2651 nm (2.5%)

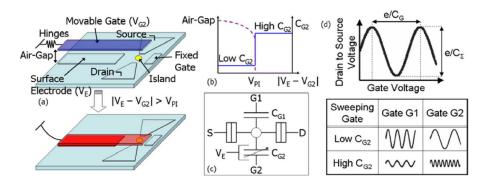


Fig. 5. (a) Concept of NEMS-gate SET device. (b) Gate displacement (left axis) and corresponding capacitance (right axis) versus actuation voltage. (c) Electrical equivalent schematic. (d) Information encoding principle: sweeping gate G1: encoding in amplitude; sweeping gate G2: encoding in periodicity.

electrodes: a suspended one, which also acts as a gate for the SET, and a fixed one, which is called the surface electrode and should ideally not interfere with the SET island. As the voltage applied between these two electrodes is increased, the spacing between them continuously decreases until the pull-in effect occurs. Since the spacing between the two electrodes also determines the spacing between the movable gate and the island of the SET, and hence the corresponding gate capacitance, the NEMS switch actually acts as a two-state tunable gate capacitor for the SET. This means that the gate capacitance can be tuned between two values according to the voltage of a third electrode, leading to further control of the Coulomb oscillations, independently of the island potential.

A possible logic application of this device based on the theory developed in [7] is shown in Fig. 6. First, one defines two logic states "LOW" and "HIGH" depending on the signal periodicity, in contrast to the "conventional" encoding that is based on the

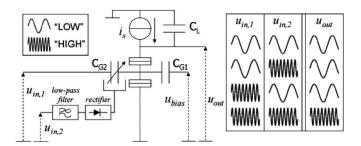


Fig. 6. Possible implementation of the AND function based on the theory developed in [7]. The period of the signal $u_{\mathrm{in},2}$ determines the voltage applied to the actuation electrode of the NEMS switch, and therefore the value of C_{G2} .

signal level. Since the background charge only alter the phase of the transfer function, an encoding of the signal into the periodicity has to be insensitive. The device is then used to store and transmit logic states by changing the Coulomb oscillation

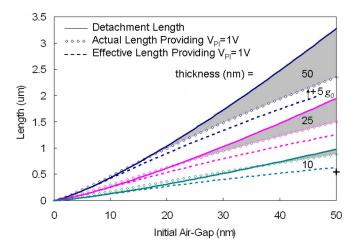


Fig. 7. Reduced <1 V actuation voltage windows for aluminum cantilevers. The symbol lines show lengths providing 1 V pull-in voltage assuming the fixed electrode is located at a distance equal to five times the initial air gap.

frequency through the gate capacitance C_{G2} . The gate position is determined by the periodicity of the signal $u_{\text{in},2}$ that is decoded via the filter/rectifier stage. Now, by sweeping $u_{\text{in},1}$ over a few periods of the transfer function, one gets a periodic output voltage with a period depending on $u_{\text{in},2}$, so that the "AND" function is realized

$$out = in, 1 \cdot in, 2. \tag{9}$$

In contrast to the conventional cantilever switches studied before, the fixed electrode is the electrode that is used to actuate the switch, and it needs to be carefully considered as it should cope with some requirements specific to the suspended-gate SET. Notably, it has to be as far as possible from the SET island in order not to interfere with the gate control. It is thus shorter than the cantilever, and the overall overlap area is reduced. The 1-D lumped model is not sufficient to account for this asymmetry, and it is all the more inadequate that we showed in a previous report that for asymmetric electrodes, the actuation voltage may vary depending on which electrode is actuated [6]. Nevertheless, as a starting point, we may get physical intuition by simply adjusting the previously defined window. For example, let us suppose that the minimal distance separating the surface electrode from the center of the island has to be five times greater than the initial air gap to ensure that the island is mainly controlled by the gate and not by the surface electrode, and assume that a cantilever with a length L and an initial air gap g_0 will behave like a cantilever having a length $L^* = L - 5g_0$. Now, we may adjust the low-voltage actuation window as shown in Fig. 7. To obtain the symbol lines, we added the virtual length $5g_0$ to the previously calculated lengths providing 1 V pull-in voltage. The result is, of course, approximate but give insight to the problem. As we can see, the range of possible lengths is reduced, and it even becomes impossible for a given thickness to get a pull-in voltage lower than 1 V below a certain initial air gap (corresponding to the intersection of the symbol and solid lines). This figure also shows that it is difficult to shorten the cantilever length below 500 nm.

B. 3-D Optimization

As shown previously with the 1-D lumped model, the dimensions and the position of the surface electrode, together with the cantilever design, have to be optimized. The 1-D model gives physical intuition but further design needs to be performed in a 3-D context, and we now proceed by using the 3-D simulator COMSOL [11]. Again, we manually implement the Casimir force as an external pressure in order to make sure that any considered structure will not collapse even when no potential is applied. Note also that, since the model solves the electrostatic equation on the deformed mesh introduced by the arbitrary Lagrangian-Eulerian (ALE) method, topology changes are not handled and solution ceases to converge before the beam touches the substrate so that it is impossible to numerically obtain the contact when statically solving the structural deformation. For the static analysis, this problem may be avoided by scanning the considered structure over different applied voltages so that a very precise estimation of the pull-in voltage may be obtained. For the dynamic analysis, however, we have to evade the absence of contact by substituting the electrostatic field (which becomes extremely complex when approaching the contact) with an electrostatic *pressure* over the overlap region. We also need to model the gas distribution beneath the cantilever that may affect the switching time. When the movable electrode squeezes the gap indeed, the gas flows out from its edges, and the narrow pathway restricts the displacement of the gas perpendicular to the surfaces, which causes gas pressure to increase and decelerates the cantilever movement. In order to model the pressure distribution in the narrow gap, we use the modified Reynold's equation

$$\nabla \cdot (h^3 Q_{ch} p \nabla p_F) = 12 \eta \left(\frac{p_F}{dt} h + p \frac{h}{dt} \right)$$
 (10)

where p_F denotes the gas film pressure variation, $p=p_A+p_F$ is the total fluid pressure consisting of the ambient pressure and the variation, $h=h_0+\Delta h$ is the gap height consisting of the initial gap and the deformation in the normal direction of the boundary, and η is the fluid viscosity at normal conditions. The term Q_{ch} denotes the relative flow rate function that accounts for the rarefied gas effects [12].

Let us first consider an 800-nm-long, 100-nm-wide, and 10-nm-thick aluminum cantilever, suspended at 50 nm over a 550 nm \times 300 nm surface electrode, so that this electrode is located at a distance five times greater than the initial air gap from its tip. The corresponding point (symbol + in Fig. 7) intuitively shows that its pull-in voltage is higher than 1 V, and the 3-D simulation indeed gives a pull-in voltage of 1.52 V. A 300-nm-wide cantilever with the same dimensions has approximately the same pull-in voltage 1.56 V. Given the length of upper limit due to the Casimir force, it seems difficult to decrease the pull-in voltage under 1 V while keeping the same thickness and initial air gap.

Now, we propose to investigate a cross-shaped structure, as shown in Fig. 8, which seems to be ideal for suspended-gate SET applications. First, it enables to reasonably and laterally increase the overlap area of the two electrodes while keeping

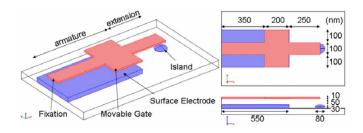


Fig. 8. 3-D simulation of a cross-shaped structure with COMSOL [11]. The insets show the dimensions of the considered structure.

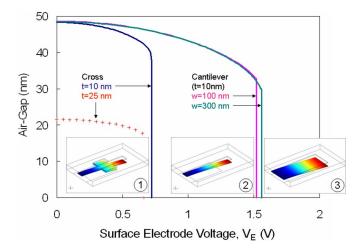


Fig. 9. Static pull-in. ①: the considered cross-shaped structure. ②: a 100-nm-wide cantilever. ③: a 300-nm-wide cantilever. The other parameters (length, thickness, air gap, and surface electrode size) are the same for the three structures and denoted in Fig. 8. The + symbols show the pull-in of a cross-shaped structure with the same dimensions except for the thickness (25 nm) and the initial air gap (25 nm). The displacement is defined at the cantilevers tip.

good flexibility and limiting air friction. Furthermore, it may be divided into two parts that can be independently designed.

- 1) The "armature" part determining the suspension and the overlap area of the overall structure, critical for the pull-in voltage.
- 2) The "extension" part determining the covering of the island, critical for the corresponding SET gate capacitance.

Let us consider from now the structure described in Fig. 8 as an example. As the previous cantilever, it is 800 μ m long, 100 nm wide, and 10 nm thick, made of aluminum, and suspended at 50 nm over a 550 nm \times 300 nm surface electrode, but two 200-nm-long and 100-nm-wide wings are also designed. The extension part is 250 nm long so that the surface electrode is located at a distance five times greater than the initial air gap from the center of the island.

Fig. 9 shows the static actuation of this cross-shaped structure as compared with the previous conventional cantilevers. As we can see, the cross-shaped design enables to substantially decrease the pull-in voltage to 0.72 V, under the symbolic 1 V value. This result is an original finding of the cross shape: it enables to combine a large overlap area (as compared to a narrow cantilever) and a certain flexibility (as compared to a wide cantilever) in order to decrease the pull-in voltage. Also

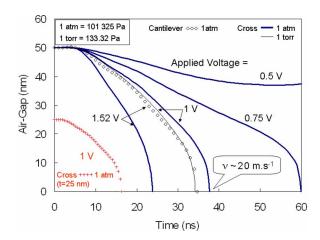


Fig. 10. Dynamic pull-in of the considered cross-shaped structure (solid lines) and a 100-nm-wide cantilever (symbol line) at several applied voltages and under different ambient pressures. The + symbols show the pull-in of a cross-shaped structure with the same dimensions except for the thickness (25 nm) and the initial air gap (25 nm) at 1 V and under standard atmospheric pressure. The displacement is defined at the cantilevers tip.

note that when no voltage is applied to the electrodes, the gap is smaller than the 50 nm initial air gap because of the Casimir force attraction.

Fig. 10 shows the dynamic response of the considered cross structure for different applied voltages under standard atmospheric pressure (1 atm = 101 325 Pa). As we can see, if the applied potential is lower than the static pull-in voltage, the cantilever moves toward its equilibrium position. However, as expected, if the applied potential is higher than the pull-in voltage, the movable electrode snaps down. The higher the applied voltage, the faster the switching, so that there is a tradeoff between the low-voltage actuation and the high-speed pull-in. For an applied voltage of 1 V (that is, $1.4V_{PI}$), we may expect a switching time of less than 40 ns. Also note that the cantilever tip speed is around 20 m·s⁻¹ for this voltage just before hitting the bottom, which is typical for NEMS switches. The dynamic response of the 100-nm-wide cantilever at its critical pull-in voltage (1.52 V) is also provided for comparison. However, for the same applied voltage, the cross is much faster. A commonly suggested solution to decrease the pull-in time is to encapsulate the device in vacuum to suppress the air friction, but this solution is of a limited interest for practical applications. Moreover, the simulation performed for a reduced ambient pressure of 1 torr (133.32 Pa) shows that the switching time is not significantly reduced because the overall size of the device is not much larger than the initial air gap. Another solution is to use a result obtained with the previous 1-D study: for a desired static pull-in voltage and for a given length, a thicker cantilever with a smaller initial air gap has a faster switching. Therefore, let us consider the same cross structure, but with a thickness of 25 nm and an initial air gap of 25 nm. Its pull-in voltage, shown in Fig. 9 (+ symbols), is 0.66 V, which is almost the same as the previous cross structure (0.72 V). Now, by computing its dynamic response, we can see in Fig. 10 (+ symbols) that its switching is more than twice faster than the previous cross structure for the same applied voltage of 1 V (16 ns versus 37 ns), which is

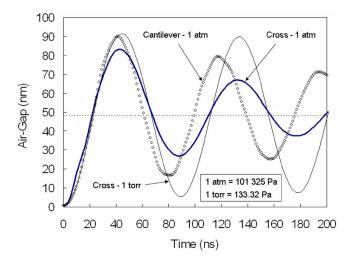


Fig. 11. Dynamic pull-out of the considered cross-shaped structure (solid lines) and a 100-nm-wide cantilever (symbol line) under different ambient pressures. The displacement is defined at the cantilevers tip.

an original finding obtained through the previously introduced methodology. Note that the tip speed before hitting the bottom is reduced (around $10~{\rm m\cdot s}^{-1}$), which also enables to reduce the pull-in energy. If the improvement is not negligible, the calculations yet show that the operation frequency of this structure is at best limited to a few hundreds of megahertz. Further miniaturization (especially concerning the air gap) and/or introduction of a tip bump to reduce the travel range [13] will be needed to achieve the gigahertz range.

To calculate the pull-out time, we use the final solution of the dynamic pull-in as initial condition in the transient analysis, and ground the surface electrode. Fig. 11 shows the dynamics of the pull-out for the considered cross structure under standard atmospheric pressure (1 atm) and low pressure (1 torr). The structure oscillates around its equilibrium position but we use the first crossing of the displacement with the final equilibrium position (slightly under the initial air gap because of the Casimir force) as a measure of the pull-up time, which is estimated to 23 ns in both cases. However, the oscillations may be an unwanted phenomenon because they can interfere with the ideal two-state capacitance behavior of the switch, and they should be absorbed as fast as possible. Lowering the ambient pressure is therefore not viable. Fig. 11 also shows the pull-out of a 100nm-wide cantilever under standard atmospheric pressure. The pull-out time as defined earlier is the same as in the case of the cross structure but the frequency of the oscillations is slightly higher. However, the dampening of the oscillations is better in the case of the cross structure because of its larger size. We will see anyway in the following section that the moment the structure pulls off, the capacitance is not significantly affected by the oscillations in the "OFF" state because of its large nonlinear change.

C. Gate Capacitance

A key parameter for the suspended-gate SET is the ratio between its gate capacitance in "ON" and "OFF" states, which

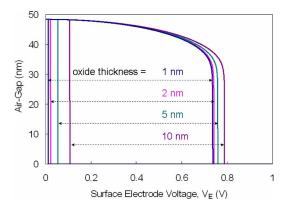


Fig. 12. Static 3-D calculated pull-in and 1-D calculated pull-out of the considered cross-shaped structure for different oxide thicknesses.

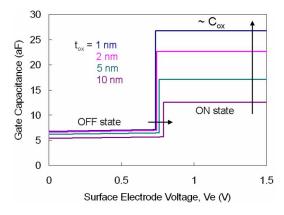


Fig. 13. Gate capacitance of the considered cross-shaped structure as a function of the surface electrode voltage for different oxide thicknesses.

should be as large as possible. A large nonlinear change can be facilitated by configuring the movable electrode so as to contact an insulating oxide layer formed on at least a portion of the SET island in the "ON" state. We may include in our model this oxide layer, which, in practice, also covers the surface electrode. To evaluate the gate capacitance, we model an ellipsoidal island with the dimensions 80 nm \times 80 nm \times 30 nm, along the x-, y-, and z-axis, respectively, and an oxide layer covering this island. The capacitance is then calculated using the energy storage distribution in the electric field and integrating over the considered volumetric domain. The final value is evaluated assuming there is a single contact point between the gate and the oxide. Fig. 12 shows that the thickness of the oxide layer does not have a significant impact on the pull-in voltage. On the contrary, as shown in Fig. 13, it is critical for the corresponding capacitance because the cantilever tip contacts the oxide covering the island in the "ON" state. Since both the size of the island and the design of the so-called extension part covering the island are also deciding the capacitance, we believe that there should be enough degrees of freedom for the designer to efficiently and precisely control the ratio between the "ON" and "OFF" capacitances. Note that problems that may arise from the fabrication process have not been addressed. Particularly, we assumed in our simulations a perfect alignment of the gate with the island, which may

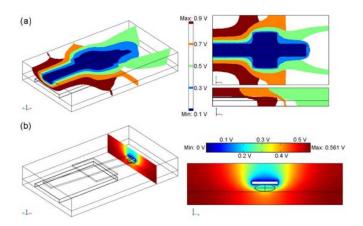


Fig. 14. Electric field distribution around the considered device calculated with COMSOL [11] by assuming the gate grounded and a potential $V_E=1~\rm V$ at the surface electrode. (a) Isosurfaces. (b) Cross section of the island.

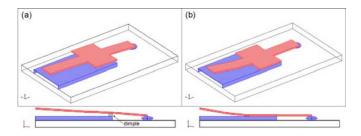


Fig. 15. Shape of the structure. (a) If it does not come into contact with the substrate. (b) If it comes into contact with the substrate ("complete collapse").

actually be very difficult to achieve since such vertical NEMS switch would have to be realized by such vertical, multilayer surface nanomachining process. Making the gate larger is one solution to reduce the probability of misalignment. However, doing so will inevitably increase the gate coupling with the drain and source electrodes, which might affect the switching speed of the device.

Another concern is the influence of the surface electrode on the SET island potential. Fig. 14(a) shows the electric field distribution around the device at the contact with the island, assuming a 2-nm-thick oxide layer and a potential $V_E=1~\rm V$ at the surface electrode (the gate is grounded). The cross section of the island [see Fig. 14(b)] shows that the field induced by the surface electrode does not critically affect the field induced by the movable gate because of the contact with the island. The parasitic capacitance between the surface electrode and the island is estimated to 5.5 aF, which is about one-fourth of the "ON" state gate capacitance.

D. Pull-Out Problem

If the structure never comes into contact with the substrate surface [see Fig. 15(a)], the pull-out should not be a problem. However, if it does [see Fig. 15(b)], the pull-out voltage may be estimated by the well-known 1-D expression

$$V_{\rm PO} = \sqrt{\frac{2d^2 K_{\rm eff} g_0}{\epsilon_0 \epsilon_r^2}} \tag{11}$$

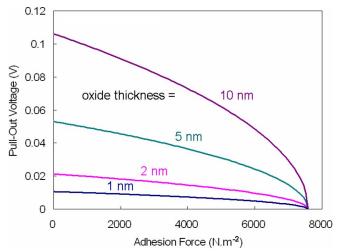


Fig. 16. Pull-out voltage as a function of the adhesion force for different oxide thicknesses.

where d and ϵ_r are the oxide thickness and dielectric constant, and $K_{\rm eff}$ is the effective spring constant calculated from (4) having units of newtons per cubic meter.

Fig. 12 shows the pull-out voltages calculated with this expression for the previously considered oxide thicknesses.

In reality, stiction is an annoying problem that may prevent the pull-out of the switch, and (11) does not take account of the corresponding adhesion force. This force is mainly due to attractive van der Waals forces and depends on various parameters such as the nature and the roughness of the surface. Let F_a be this force per unit area. The pull-out voltage is then calculated as

$$V_{\rm PO} = \sqrt{\frac{2d^2(K_{\rm eff}g_0 - F_a)}{\epsilon_0 \epsilon_r^2}}.$$
 (12)

When the cantilever comes into contact with the substrate surface, adhesion will not occur if the necessary elastic deformation requires more energy than the surface energy obtained through adhesion, i.e., if $V_{PO} > 0$. Fig. 16 shows the pull-out voltage as a function of the adhesion force. The stronger the force, the lower the pull-out voltage. Ultimately, if the adhesion force is greater than 7600 N·m⁻², the cantilever is prone to permanent adhesion, independently of the oxide thickness. Assuming $F_a = 2(\Gamma/D_0)$, where Γ is the interfacial adhesion energy per unit area and D_0 is an offset corresponding to the closest approach of the two surfaces [14], the involved adhesion energy has to be around $10 \mu \text{J} \cdot \text{m}^{-2}$ or less, which is much lower than the lowest surface energies observed in nature, but typical for NEMS structure. The treatment of the surface to reduce this energy is therefore one possible solution to reduce the likelihood of adhesion without changing the cantilever dimensions. For example, whereas for untreated polysilicon, the surface energy is approximately $270 \pm 100 \,\mathrm{mJ \cdot m^{-2}}$, self-assembled monolayer films can reduce the surface energy to approximately 3 μ J·m⁻² [15]. Another solution may be to introduce dimples to reduce the contact area. Otherwise, assuming stiction has occurred, some attempt to recovery may be made by applying a stress wave from a piezoelectric, which could be done over the whole wafer.

E. Performance Analysis

The switching speed of the suspended-gate SET can be limited by two factors: the speed of the gate movement and the intrinsic delay of the SET. The previous dynamic analysis showed that the gate speed is limited to a dozen nanoseconds. However, the fundamental speed limit of SETs being linked to the speed of quantum mechanical tunneling (<1 ps), the limiting factor is by far the switching speed of the gate, which limits the operation frequency to the megahertz range. As said before, further miniaturization of the dimensions is needed to reach the gigahertz range.

The energy consumed in the switching process is given by

$$E(t) = V_s \int_0^t i(t')dt' \tag{13}$$

where V_s is the source voltage and i(t) the switching current, and the voltage applied to the cantilever being $V(t) = V_s - Ri(t)$. It consists of the following.

1) The electrostatic energy E_e stored in the NEMS and the SET capacitors

$$E_e(t) = E_0 + \frac{1}{2}C_{\text{gap}}(t)V(t)^2$$
 (14)

where $C_{\rm gap}(t)$ is the total (both NEMS and SET) gap capacitance and E_0 the energy loss while instantaneously charging $C_{\rm gap}(0)$.

2) The mechanical energy E_m stored in the cantilever spring

$$E_m(t) = \frac{k}{\tau} \iiint_{\tau} z_M^2(t) d\tau \tag{15}$$

where τ and k, respectively, denote the volume and the spring constant (in newtons per meter) of the structure, and z_M denotes the vertical displacement of the infinitesimal volume $d\tau$.

3) The kinetic energy E_k of the inertial mass

$$E_k(t) = \frac{\rho}{2} \iiint_{\tau} v_M(t)^2 d\tau \tag{16}$$

where ρ denotes the density of aluminum and v_M denotes the velocity of the infinitesimal volume $d\tau$.

4) The energy E_d dissipated in the damping mechanism

$$E_d(t) = -\int_{C(t)} \iint_S \mathbf{F}_M(t') \cdot d\mathbf{s}_M(t') dS \qquad (17)$$

where S denotes the surface of the structure, and C, \mathbf{F}_M , and \mathbf{s}_M , respectively, denote the path traversed, the surface damping force vector (in newtons per square meter) applied, and the position vector of the infinitesimal surface dS

5) The energy E_R dissipated in the bias resistor (used to reduce the current density in the structure)

$$E_R(t) = R \int_0^t i(t')^2 dt'.$$
 (18)

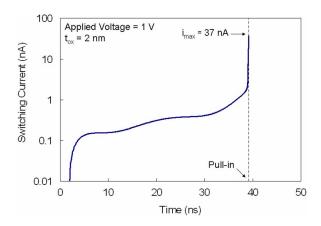


Fig. 17. Switching current of the considered cross-shaped structure, assuming a zero source resistance.

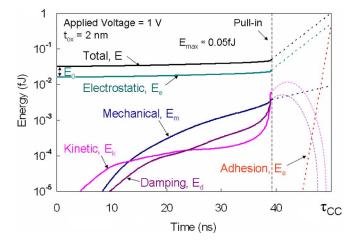


Fig. 18. Variation of the total energy and its components during the switching process for the considered cross-shaped structure, assuming a zero source resistance. τ_{CC} denotes the assumed time of complete collapse of the considered structure.

The total energy consumed at time t is

$$E(t) = E_e(t) + E_m(t) + E_k(t) + E_d(t) + E_R(t).$$
 (19)

To simplify, we assume in this simulation a zero source resistance (R=0), which is to say that the voltage V across the structure is equal to the voltage V_s delivered by the source. In practice, a 100-k Ω resistor is needed to reduce the current density to a reliable range in the structure because of its reduced cross section. The presence of the resistor would actually reduce the velocity of the structure at the point of contact by causing the voltage across the switch to drop because of the rapid change of capacitance at this time [16].

Fig. 17 shows that the peak of the switching current occurs during the pull-in effect, when the structure speed is the highest. At the contact with the island, it is estimated to be 37 nA. The variation of the total energy and its components during the switching process is shown in Fig. 18. As we can see, the kinetic and the damping energies account for a nonnegligible part of the total switching energy. At the contact with the island, the pull-in energy is estimated to 0.05 fJ. For comparison, the minimum

switching energy achieved by the present CMOS technology is 0.1 fJ [17].

However, because the transient analysis stops when the contact occurs, it is difficult to know the actual final state of the switch. If the structure does not adhere to the substrate [see Fig. 15(a)], i.e., if the final shape is close to the last simulated point, the current and energies calculated before are valid. However, if the structure completely collapses [see Fig. 15(b)], it will drastically increase both the switching current and the consumed energy. The expected evolution of the energies until the complete collapse (at time τ_{CC}) is shown in Fig. 18. While the kinetic and damping energies gradually vanish, the beam obtains energy through adhesion. In this case, the total consumed energy is estimated to be 1 fJ, which is 20 times higher than without the collapse. This state is all the more unwanted because, as seen previously, it also increases the likelihood of adhesion. Increasing the stiffness of the structure would at the same time increase the pull-in voltage so that the use of a tip bump [13] or a dimple [see Fig. 15(a)] is likely to be the best solution to prevent the complete collapse.

IV. CONCLUSION

We investigated the operation and the performance of NEMS switches. We proposed a simple methodology based on the 1-D model to determine a low-voltage actuation window for conventional cantilevers. The model gives fast and accurate physical insight and certainly helps with systematic design. We then modeled and optimized a cross-shaped cantilever in the aim of using it as a movable gate to modulate the Coulomb oscillation of a conventional SET. Both its static and dynamic characteristics were simulated, the effect of the oxide layer was investigated, and the pull-out problem was addressed. Although further miniaturization is required to achieve the gigahertz range, gain in terms of power consumption and scalability makes it very competitive.

ACKNOWLEDGMENT

The authors would like to thank M. Manoharan and K. Akarvardar for their valuable help.

REFERENCES

- [1] R. G. Knobel and A. N. Cleland, "Nanometre-scale displacement sensing using a single electron transistor," *Nature*, vol. 424, pp. 291–293, 2003.
- [2] M. D. LaHaye, O. Buu, B. Camarota, and K. C. Schwab, "Approaching the quantum limit of a nanomechanical resonator," *Science*, vol. 304, pp. 74–77, 2004.
- [3] D. V. Scheible and R. H. Blick, "Silicon nanopillars for mechanical singleelectron transport," *Appl. Phys. Lett.*, vol. 84, no. 23, pp. 4632–4634, 2004.
- [4] C. Wasshuber, "Recent advances and future prospects in single-electronics," in *Proc. Design Autom. Conf.*, 2003, pp. 274–275.
- [5] S. Mahapatra, V. Pott, S. Ecoffey, A. Schmid, C. Wasshuber, J. W. Tringe, Y. Leblebici, M. J. Declercq, K. Banerjee, and A. M. Ionescu, "SETMOS: A novel true hybrid SET-CMOS high current Coulomb blockade oscillation cell for future nano-scale analog ICs," in *Proc. IEDM*, 2003, pp. 703–706.
- [6] B. Pruvost, H. Mizuta, and S. Oda, "3-Dimensional design and analysis of functional NEMS-gate MOSFETs and SETs," *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 218–224, Mar. 2007.

- [7] R. Klunder and J. Hoekstra, "Circuit architecture solution for background charge fluctuations in single electron tunneling transistors," in *Proc.* ECCTD, 2001, pp. 213–216.
- [8] H. B. Chan, V. A. Aksyuk, R. N. Kleiman, D. J. Bishop, and F. Capasso, "Quantum mechanical actuation of microelectromechanical systems by the Casimir force," *Science*, vol. 291, pp. 1941–1944, 2001.
 [9] R. W. Johnstone and M. Parameswaran, "Theoretical limits on the free-
- [9] R. W. Johnstone and M. Parameswaran, "Theoretical limits on the freestanding length of cantilever produced by surface micromachining technology," *J. Micromech. Microeng.*, vol. 12, pp. 855–861, 2002.
- [10] W.-H. Lin and Y.-P. Zhao, "Casimir effect on the pull-in parameters of nanometer switches," *Microsyst. Technol.*, vol. 11, pp. 80–85, 2005.
- [11] COMSOL. User's guide. (2007). [Online]. Available: www.comsol.com
- [12] T. Veijola, H. Kuisma, J. Lahdenpera, and T. Ryhanen, "Equivalent-circuit model of the squeezed gas film in a silicon accelerometer," *Sens. Actuators*, vol. A48, pp. 239–248, 2005.
- [13] K. Akarvadar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, and H.-S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," in *Proc. IEDM*, 2007, pp. 299–302.
- [14] J. A. Knapp and M. P. de Boer, "Mechanics of microcantilever beams subject to combined electrostatic and adhesive forces," *J. Microelectromech. Syst.*, vol. 11, no. 6, pp. 754–764, 2002.
- [15] R. Maboudian and R. T. Howe, "Critical review: Adhesion in surface micromechanical structures," *J. Vacuum Sci. Technol.*, vol. B15, pp. 1– 20, 1997.
- [16] J. B. Muldavin and G. M. Rebeiz, "Nonlinear electro-mechanical modeling of MEMS switches," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2001, pp. 2119–2122.
- [17] ÎTRS. (2007). Emerging Research Devices. [Online]. Report. Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm



Benjamin Pruvost (S'09) received the Diplôme d'Ingénieur from the Ecole Supérieure d'Electricité (Supélec), Gif-sur-Yvette, France, and the M.S. degree in physical electronics in 2006 from Tokyo Institute of Technology, Tokyo, Japan, where he is currently working toward the Ph.D. degree at the Quantum Nanoelectronics Research Center.

His current research interests include modeling and design of new hybrid nanodevices.



Ken Uchida (M'00) received the B.S. degree in physics and the M.S. and Ph.D. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 1993, 1995, and 2002, respectively.

In 1995, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He was involved in the study of carrier transport in nanoscale devices such as single-electron devices, Schottky source/drain MOSFETs, ultrathin-body silicon on insulator (SOI) MOSFETs, strained silicon MOSFETs, carbon nanotube transistors, and (1 1 0)

Si MOSFETs. Since April 2008, he has been an Associate Professor at Tokyo Institute of Technology, Tokyo, Japan. He is also with the Solution Oriented Research for Science and Technology (SORST), Japan Science and Technology (JST), Saitama, Japan.

Dr. Uchida is a member of the Japan Society of Applied Physics and the IEEE Electron Devices Society (EDS). He won the 2003 IEEE EDS Paul Rappaport Award for his work on single-electron devices and the 2005 Young Scientist Award from Ministry of Education, Culture, Sports, Science and Technology of Japan. He was a member (2005, 2006) as well as the Subcommittee Chair (2007) of the Solid-State and Nanoelectronic Devices (SSN) Subcommittee of the IEEE International Electron Devices Meeting (IEDM). He was a Distinguished Lecturer of the Solid-State Circuit Society of IEEE in 2007/2008.



Hiroshi Mizuta (M'89) received the B.S. and M.S. degrees in physics and the Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1983, 1985, and 1993, respectively.

In 1985, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan, where he was involved in research on high-speed heterojunction devices and resonant tunneling devices. From 1989 to 1991, he was involved in the study of quantum transport simulation. From 1997 to 2003, he was the Laboratory Manager and a Senior Researcher at the Hitachi

Cambridge Laboratory, U.K., where he was involved in the research on single-electron devices and associated nanoelectronic devices. From 2003 to 2007, he was an Associate Professor of physical electronics at Tokyo Institute of Technology, Japan, where he is currently an Adjunct Professor of quantum nanodevices. Since April 2007, he has been a Professor of nanoelectronics at the University of Southampton, Southampton, U.K. He is also with the Solution Oriented Research for Science and Technology (SORST), Japan Science and Technology (JST), Saitama, Japan. His current research interests include silicon-based nanoelectronics, nanoelectromechanical devices, quantum information processing, and *ab initio* simulation of silicon nanostructures and quantum transport. He has authored or coauthored more than 280 scientific papers and filed over 50 patents. He has also authored books and chapters, including *Physics and Applications of Resonant Tunnelling Diodes* (Cambridge University Press).

Prof. Mizuta is a member of the Physical Society of Japan, the Japan Society of Applied Physics, the Institute of Physics, and the Electron Device Society of the IEFE.



Shunri Oda (M'89) received the B.Sc. degree in physics and the M.S. and Ph.D. degrees from Tokyo Institute of Technology, Tokyo, Japan, in 1974, 1976, and 1979, respectively.

He is currently a Professor in the Department of Physical Electronics and Quantum Nanoelectronics Research Center, Tokyo Institute of Technology. He is also with the Solution Oriented Research for Science and Technology (SORST), Japan Science and Technology (JST), Saitama, Japan. His current research interests include fabrication of silicon quan-

tum dots by pulsed plasma processes, single-electron tunneling devices based on nanocrystalline silicon, ballistic transport in silicon nanodevices, silicon-based photonic devices, and high-k gate oxide ultrathin films prepared by atomic layer metal-organic chemical vapor deposition (MOCVD). He has authored or coauthored more than 200 papers published in journals and conference proceedings.

Prof. Oda is a member of the Electrochemical Society, the Materials Research Society, and the Japan Society for Applied Physics. He is a Distinguished Lecturer of the IEEE Electron Devices Society.