Optimal Sizing of Configurable Devices to Reduce Variability in Integrated Circuits

Abstract

This paper describes a systematic approach that facilitates yield improvement of integrated circuits at the post-manufacture stage. A new Configurable Analogue Transistor (CAT) structure is presented that allows the adjustment of devices after manufacture. The technique enables both performance and yield to be improved as part of the normal test process. The optimal sizing of the inserted CAT devices is crucial to ensure the greatest improvement in yield and this paper considers this challenge in detail. An analysis and description of the underlying theory of the sizing problem is given along with examples of incorrect sizing. Guidelines to achieve optimal CAT sizing are proposed, and results are provided to demonstrate the overall effectiveness of the CAT approach.

1. Introduction

Silicon based semiconductor technology is heading towards increasingly smaller components with transistors being scaled down to nanometre dimensions. For example, 45nm and 65nm technologies are being used for high integration microprocessor circuits, superseding the ubiquitous 90nm technology node [1]. As device dimensions shrink, digital circuit performance on the whole continues to thrive [2]. The reality of multi-processors on a single die has been realized and the prospects for continued success beyond 65 nm are good. Due to this extensive integration capability, the need has grown for Analogue and Mixed Signal (AMS) support circuitry on what are predominantly digital chips. Integrating a wide range of analogue circuit functions on the same silicon as vast microprocessor and memory blocks brings about new challenges for analogue design. As a result, the analogue parts of system chips are now becoming a serious design bottleneck. Typically 10% of the chip design may be analogue in function, but this same section can absorb 90% of the design time. Now, more than ever, analogue designers realize they will become as reliant on design automation tools as the digital design community, especially with increasing pressure on time to market precluding the received wisdom of "bespoke" analogue design for every process node that emerges.

Annema *et al* [3] clearly highlight the "roadblocks" approaching for analogue design, which include reducing supply voltage and increased leakage and process variation. The reduction of supply voltage leads to a direct loss of headroom when designing analogue circuits – which in turn impacts on dynamic range, noise and signal integrity. As technologies become smaller, leakage becomes a greater problem in analogue circuits, indeed this is one of the most significant problems for digital design [4]. Variability in process parameters is a far greater problem in DSM nodes especially as device models are reaching their limits of predictability [5]. To overcome these significant issues, fundamentally new design techniques are required. The demands on analogue designers require that they continue to keep pace with their digital counterparts, by developing new models and supporting methodologies. Clearly, these methodologies must consider yield as an active part of the design process, such that the initial design can be made as tolerant of device variability as possible. Crucially, even if a design has been implemented taking these factors into account, it may simply not be possible to ensure that a performance is met over the specified yield. A mechanism for post-manufacture compensation is essential in order to integrate high performance analogue circuits on current and future DSM process nodes.

Bernstein, *et al* noted the problem of intrinsic device variability with decreasing process technology nodes in [6]. This is a particular problem for AMS designs where yield is severely degraded below the 120nm process node as a result of this increasing variability. Recent research has been targeted at analog circuit design as result, to identify potential solutions to this problem from a structural perspective, such as recently by Gielen *et al* [4]. Variability can be broadly categorized into spatial and temporal effects. Spatial variability can include die to die parameter mean shifts, on-chip layout induced variations and device to device mismatch caused by atomistic dopant

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variations, line edge roughness and parameter standard deviation [6],[7]. Temporal effects refer to time dependant changes in performance and reliability such as dielectric breakdown (DB), hot carrier injection (HCI) and negative bias temperature instability (NBTI), and these are now causing significant changes in a circuit's performance over its lifetime [7]. In the case of analogue circuits the impact of variability can be complex due to a large number of performance specifications. Traditional approaches to increase robustness and resilience can introduce unacceptable power and area penalties when applied to modern process nodes [4]. Conventional techniques have attempted to mitigate the effects of device variability using a standard robust design approach, but this clearly has limitations, and does not fundamentally address the issue of post-manufacture failure, lifetime degradation and device drift [8],[9],[10].

In this paper a systematic approach is proposed to improve the overall integrated circuit yield by facilitating the adjustment of yield-critical circuit transistors, after manufacture. In Section 2, we provide a background of the technique and associated structures, to an extent required by later sections. In Section 3 we provide an analysis of the underlying theory, proving how it can improve the yield of a design. In Section 4 the sizing approach is derived and an optimal solution demonstrated. Section 5 presents results from fabricated silicon to prove the concept works in a practical context.

2. Introduction to the CAT technique

A configurable analogue transistor (CAT) consists of a main device and a number of additional adjustment devices. The adjustment device drains, sources and bulks are connected in parallel to the main device, and their gates are connected to the main device gate through switches. An NMOS CAT structure containing n adjustment devices is shown in Figure 1.

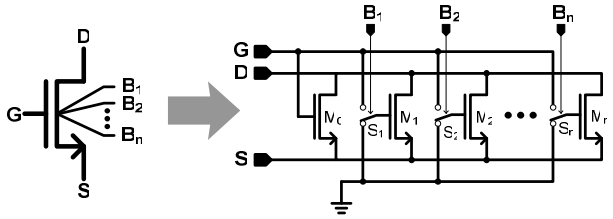

Figure 1. CAT Structure

By selectively driving the bit lines B_1 to B_n, it is possible to connect an adjustment device M_1 to M_n in parallel to the main device M_0. This effectively changes the overall device width, allowing tuning of the fundamental characteristics of the CAT. The CAT technique therefore provides a mechanism to adjust the width of a transistor after manufacture, in order to improve the performance or yield [11].

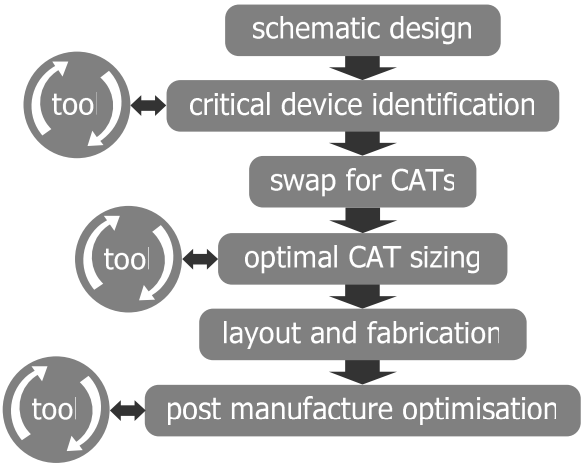

Figure 2. CAT process

Figure 2 shows the design process used for the CAT technique. In the critical device identification stage, sensitivity analysis is carried out to ensure that only the most yield-critical devices in a circuit are swapped with CAT devices. The number of critical devices to swap is chosen as a design trade-off between potential yield improvement and area and complexity overhead. Once the chosen transistors are swapped for CAT devices, the adjustment devices must be sized to achieve the best potential for yield improvement. The CAT adjustment devices are typically weighted in a binary fashion, to allow 2^n possible width variations. If the adjustment is too fine, then variations may not be sufficiently compensated to meet the target value. Conversely, if the adjustment is too coarse then there may be insufficient resolution for effective variation compensation. Section 3 considers the underlying theory for this step, and an optimum sizing algorithm is derived in Section 4. After manufacture, the characteristic of each individual transistor may deviate from the typical mean due to the systematic and random variation sources already discussed. The CAT devices are adjusted, following suitable measurements, in order to tune their widths and hence compensate for these variations.

3. Fundamental CAT sizing concepts

This section presents a simple example of the problem of process variation and demonstrates the effect of the CAT sizing on the potential for yield improvement. The results provided in this section are all obtained from large numerically derived data sets, generated by a computer to simulate variation on a wafer.

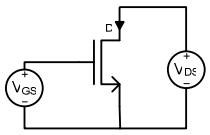

Figure 3. Single device drain current.

Figure 3 shows the simple circuit of an NMOS transistor, biased in its saturation region to give a constant drain current, I_D. In reality, although the transistor may be sized for a particular current, the measured I_D performance will form a distribution around the mean, the spread of which will relate to the variability of the process used. To illustrate this point, this circuit has been simulated 100,000 times using a statistical process model, and the result is shown in Figure 4. Although the device was sized for a mean I_D of 400µA, the spread due to process variation causes some samples to exhibit an I_D as low as 300µA or as high as 500µA. For this single device, the standard deviation in I_D is 30µA.

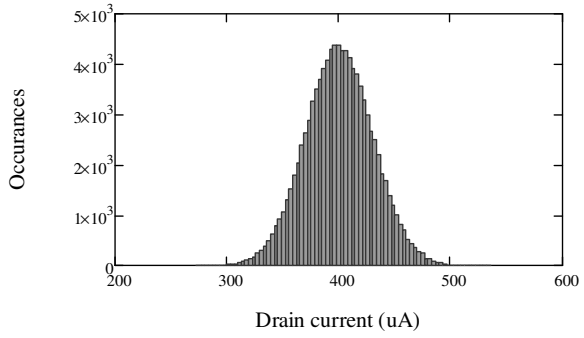

Figure 4. Typical process spread of an NMOS device

The spread of the samples directly relates to the obtainable yield. If, for this example, the specification permits a drain current of 400µA ± 15µA, then yield would be 38.4%. Traditional approaches in analogue circuit design can help enormously to reduce the impact of variation on circuit performance, but as process technologies become less reliable these approaches are not always enough to ensure high yield. Although here the parameter of drain current has been chosen for simplicity, it should be appreciated that this could just as well be any circuit performance parameter. Provided the sources of error can be approximated to a Gaussian distribution, then the spread in the performance parameter will also approximate to a Gaussian distribution.

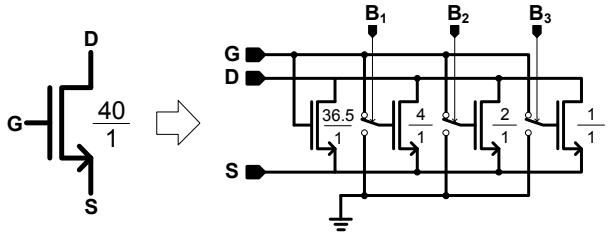

Figure 5. Example CAT device replacement.

As explained in Section 2, the CAT technique uses a number of additional transistors as adjustment devices to allow compensation of a circuit's performance after manufacture. Figure 5 shows the example of a transistor with width 40µm being replaced by a main transistor of width 36.5µm and three adjustment devices, of 1, 2 and 4µm. This provides a total adjustment range of 36.5µm to 43.5µm and resolution of 1µm, with eight possible sizes depending on which adjustment pieces are selected. As shown in Figure 6, when the chip returns from fabrication, if the drain current is too high then the CAT size can be reduced accordingly through the adjustment pieces. Conversely, if the drain current is too low, then the CAT size can be increased.

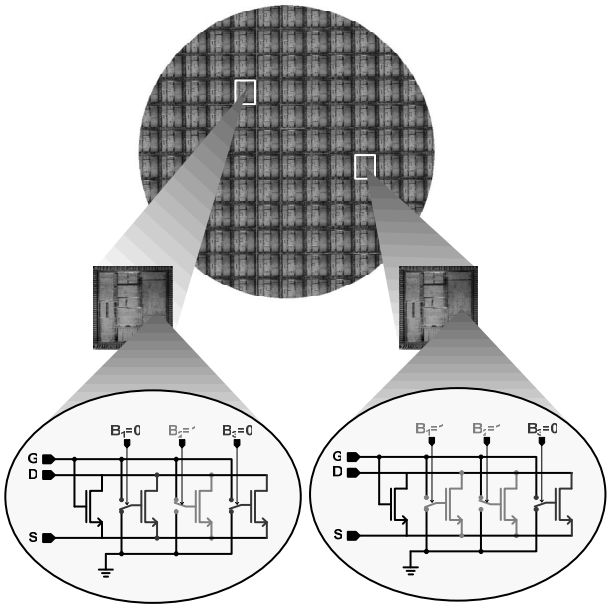

Figure 6. Example CAT adjustment after manufacture

The sizing of the CAT adjustment pieces determines the potential for yield improvement. Using the example of Figure 4, we can consider the eight different combinations of the three adjustment pieces as eight distributions with evenly spread means. Figure 7 shows the distribution in Figure 4 in the case of a mean separation of 35µA (bars have been joined with lines for clarity). After manufacture, the configuration which gives the least distance to the target value can be chosen. The process of choosing the closed configuration to the mean can be expressed as:

```
For each sample
   MinError = 100%
   For each configuration
        Calculate error between
          measured and designed
        If error < MinError
        Store configuration
        MinError = calculated error
   End For
End For
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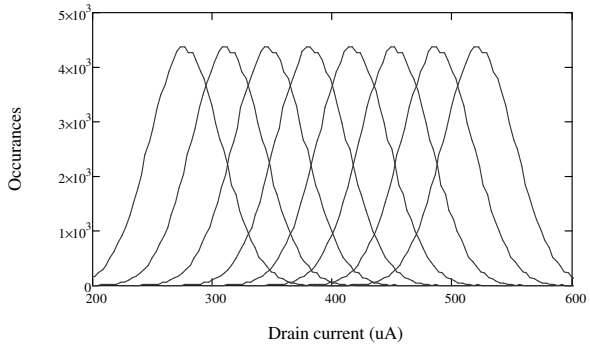

Figure 7 Device distribution seperation

This simple algorithm is an exhaustive search on the configuration space, and could be improved by standard optimisation approaches; however it is suitable for this example. A new sample set can therefore be generated for the compensated CAT devices, using the best configuration for each sample point. For the example given in this section, Figure 8 shows the distribution of the compensated sample set along with the original distribution. Clearly there is an improvement in spread - indeed the standard deviation has improved from 30µA to 10.11µA. Consequently this has resulted in a yield increase from 38.4% to 85.7%. However, the choice of a 35µA separation was arbitrary in this case, and there seems to be potential for greater improvement.

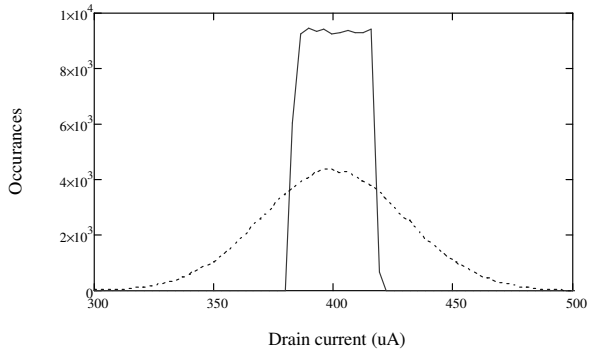

Figure 8. Compensated and uncompensated samples

It is intuitive that a very wide separation would not offer the granularity of adjustment to make a large improvement in spread. Conversely, a very fine separation is unlikely to offer enough adjustment to compensate the outliers. To demonstrate this point, Figure 9 shows the compensated CAT distribution for separations of 65µA, 35µA and 8µA. Although the spread appears tighter as the separation reduces, the smallest separation is not capable of greatly improving the sample outliers, and so the distribution 'leaks' at the extremes. Indeed this is reflected in the standard deviations which are 18.96µA, 10.11µA and 12.65µA for the 65µA, 35µA, and 8µA separations respectively. What this suggests is that there would appear to be some separation at which the standard deviation is optimum. Clearly this provides an optimization opportunity to find the best choice of separation for a given CAT device. Furthermore, this example has only considered three adjustment devices, whereas more devices would give a greater number of width combinations and hence offer even greater opportunity for yield improvement.

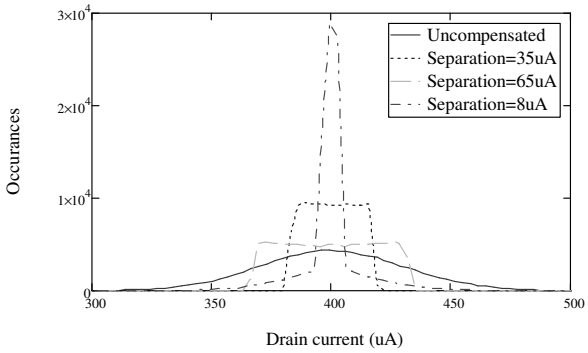

Figure 9. Effect of separation on distribution spread.

4. Systematic approach to device sizing

The previous section relied on large sample sets of numerical data to draw the conclusion that an optimum separation existed. In this section an additive integral technique is used instead of raw numerical data. Although outside of the scope of this paper, it can be shown that the addition of sections of the separated CAT distributions results in the distribution of the compensated data. This allows a much faster computation of the results shown in Figures 7 to 9. Again using the example of a mean of 400µA and a standard deviation (*sd*) of 30µA, Figure 10 plots mean separation against standard deviation. This confirms an optimum separation of 17.5µA which gives the lowest standard deviation of 5.8µA. This represents an 80.7% reduction compared to the uncompensated case.

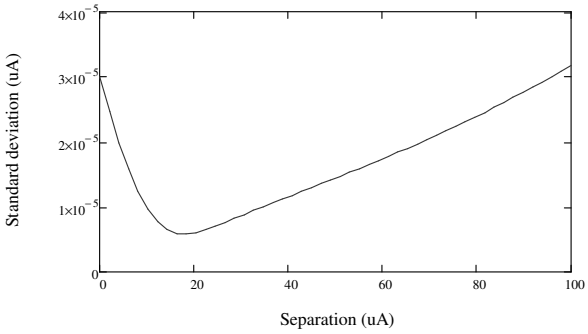

Figure 10. Improvement in *sd* versus separation

Mean separation is a key parameter in the CAT sizing algorithm. However, it is also important to consider the effect of the number of adjustment pieces (*n*) on the standard deviation improvement. Again using the additive integral model, Figure 11 has been generated to show the standard deviation against separation for the case of *n*=1, 2, 3 and 4 adjustment pieces, providing 2, 4, 8 and 16 width combinations respectively.

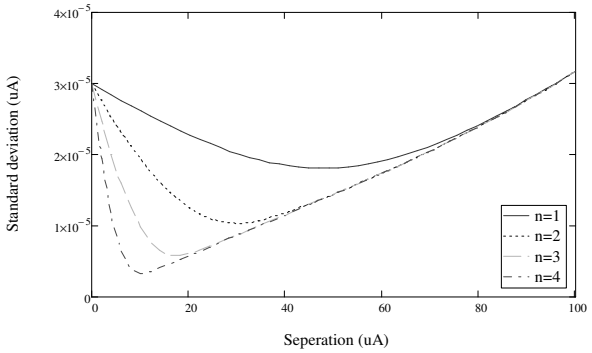

Figure 11. Standard deviation for different values of n

As expected, there is an advantage in increasing the number of adjustment pieces. With just one adjustment piece, it is possible to achieve a 40% improvement in standard deviation, whereas four adjustment pieces gives an improvement of 89%. A greater number of adjustment pieces will naturally increase the area and complexity overheads of the CAT technique, and so the value of n must be carefully traded off against the improvement in standard deviation. To further illustrate the choice of adjustment pieces, Figure 12 shows the relationship between n and both the improvement in standard deviation and the optimum separation. This Figure suggests that above five adjustment pieces, the standard deviation improvement is unlikely to warrant the additional area and complexity overhead. Indeed, two or three adjustment pieces seem to provide the best trade off between overhead and yield improvement.

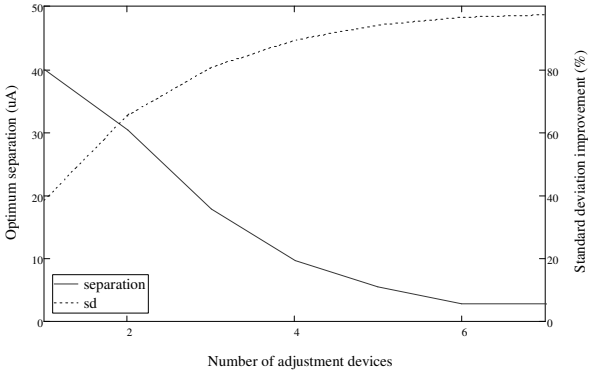

Figure 12. Effect of number of adjustment pieces

Once the mean separation has been determined, it is trivial to work back from this value to determine the adjustment device resolution required to achieve this separation. For example in the case of a 40µm transistor giving a mean current of 400µA with a standard deviation of 30µA, the optimum mean separation for the three adjustment pieces would be 17.5µA. The three adjustment pieces in this case would be 1.75µm, 3.5µm and 7µm and the main device would be scaled down to 33.875µm. This would give an adjustment range of 12.25µm with the required mean separation, and maintaining an overall mean of 40µm.

A solver has been written using the integral area method to give the optimum mean separation for a given number of adjustment devices and transistor standard deviation. An interesting finding is that the mean optimum separation is constant when expressed as a percentage of the standard deviation. The best possible standard deviation improvement is also fixed for any given number of adjustment pieces. This makes it trivial to calculate the correct separation simply by knowing the standard deviation of the transistor parameter in question. Table 1 summarises the optimum separation percentages and best improvements for adjustment pieces up to *n*=5.

n	Mean separation (% of sd):	Improvement (%):
1	158.5	39.7
2	99.0	65.5
3	58.2	80.7
4	33.3	89.3
5	18.7	94.1

Table1. Separation and improvement values

5. Measurement results

In order to prove the benefits of the CAT technique, a silicon demonstrator has been fabricated on a standard 120nm 1.2V digital process. A total of 192 NMOS CAT cells are implemented in an array of 24x8, each containing three adjustment devices. The CAT devices have been sized using method derived in this paper.

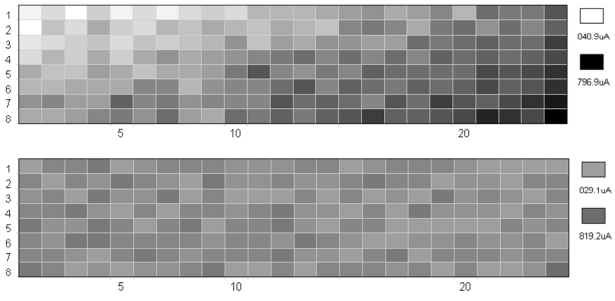

Figure 13. Uncompensated (top) and compensated (bottom) CAT array silicon results.

Figure 13 shows a topographical map showing the measured, uncompensated and compensated CAT drain currents for one sample die. Clearly there is a large improvement in spread, as predicted by the theory, which is indicated by the variation of colours apparent in the graph (13(a)). A histogram of the drain currents is shown in Figure 14, for both the uncompensated and compensated array. The standard deviation reduction from 9.85µA to 2.46µA represents an improvement of 75%. When 20 sample dies were measured, the improvement ranged from 73.4% to 78.8% which agrees extremely well with the theoretical maximum improvement of 80.7% shown in Table 1. The improvement in variability is also demonstrated visually in Figure 13(b).

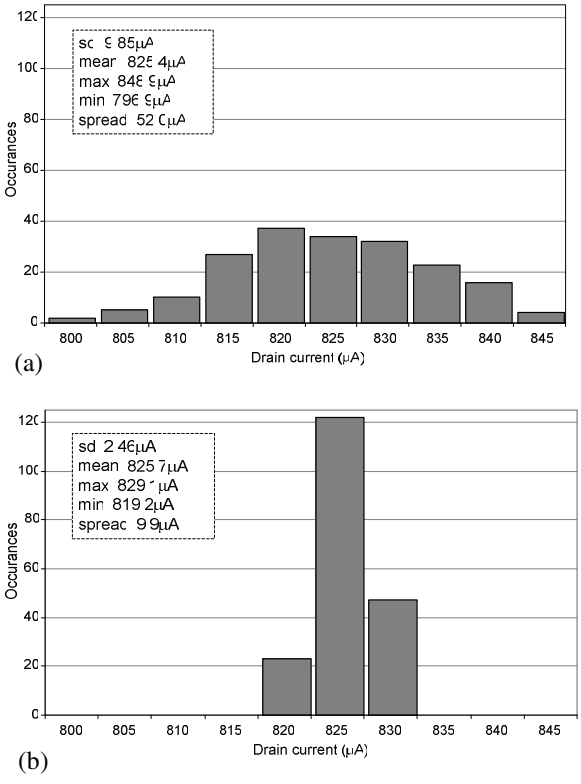

Figure 14 histogram of compensated (a) and uncompensated (b) drain currents.

6. Conclusions

Variation is one of the biggest challenges associated with deep submicron process technologies, and is particularly acute for analogue designs. This paper has introduced a new technique for post fabrication variation compensation. A configurable analogue transistor (CAT), containing a number of small additional transistors allows the size of a device to be adjusted after fabrication. A key parameter of the CAT devices is the sizing of the adjustment pieces which determines the potential for yield improvement. The fundamental issues regarding mean separation have been demonstrated through numerically simulated data sets, and the potential for an optimum separation has been identified. Using an additive integral technique, the optimum point of separation has been identified, and this has been extended to a number of adjustment devices. It has been found that the optimum separation point can be easily determined for any number of adjustment pieces. A silicon demonstrator has been fabricated and demonstrates an improvement in standard deviation of up to 78.8% following compensation with the CAT devices. This work shows how the CAT technique can be used to effectively address the issue of process variation in analogue circuits.

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