INVITED PAPER

VERTICAL MOSFETs FOR HIGH PERFORMANCE, LOW COST CMOS

S. Hall*, L. Tan*, O. Buiu*, M.M. Hakim, T. Uchino**, P. Ashburn**, W. Redman-White****

*Department of Electrical Engineering & Electronics, University of Liverpool, Brownlow Hill, Liverpool L69 3GJ, UK
E-mail: s.hall@liv.ac.uk
**School of Electronics and Computer Science, University of Southampton
E-mail: pa@ecs.soton.ac.uk

Abstract–*We present a review of recent reports on vertical MOSFETs which includes a summary of our own research in this area. Such devices can offer a decananometer channel length in a relaxed lithography. Furthermore, the footprint is substantially smaller than an equivalent lateral MOSFET for a given on-current. We summarise a number of innovative device architectures that allow control of short channel effects and reduction of parasitic elements. Both numerical modelling and experimental results are presented to validate the proposals. The devices are particularly suited to radio frequency application.*

Keywords: *vertical MOSFETs, short channel effects, RF devices*

1. INTRODUCTION

Vertical MOSFETs (vMOSTs) are proposed as a possible device architecture to allow continued scaling along the ITRS roadmap[1]. In fact, processing steps such as epitaxy and ionimplantation (II) offer high precision and reproducibility for forming thin, doped regions in the vertical plane. Device architectures based on II are to be preferred due to the ease with which the p-channel and n-channel devices required for full CMOS can be realized in addition to the relatively low cost. The work presented here focuses mainly on n-channel devices which could be used for radio-frequency applications. Such devices could either form discrete amplifier modules or be incorporated into a full CMOS or BiCMOS process. We will show that the device can be realized at relatively relaxed lithographic nodes but bring performance comparable to two or three generations. Fig. 1 illustrates the reduced footprint achievable for double gate and gate all-around vertical architectures compared to a lateral layout. The challenges for vertical architectures relate to the need for short channel control, exacerbated by the relatively deep junctions and large parasitic overlap capacitances inherent in vMOSTs.

The paper is organized as follows. In section 2, we present a review of the more recently reported work on vMOSTs. In section 3 we summarise our work on architectural innovations to control short channel effects and to reduce parasitic capacitance. This is followed in section 4, by a description of more advanced features for vMOST design. Section 5 contains a discussion of possible applications of the devices, particularly for radio-frequency applications and the paper is concluded in section 6.

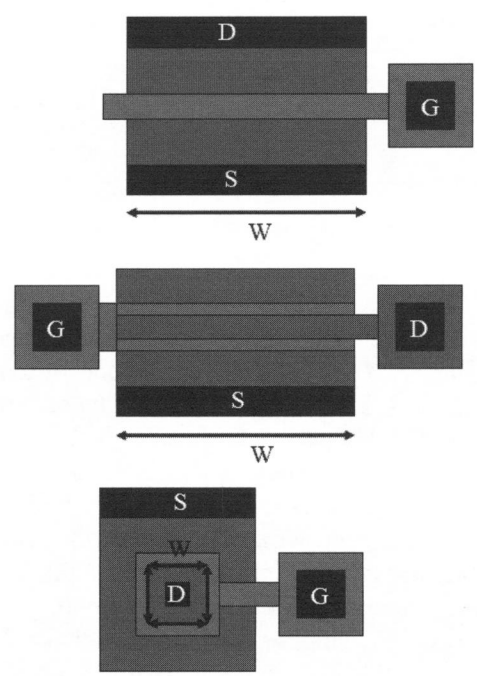

Fig. 1. Comparison of layouts to illustrate reduced footprints: TOP lateral MOSFET, MIDDLE: vertical double gate MOSFET, BOTTOM gate all-around vMOST.

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2. REVIEW

The recent development of vertical vMOST has been largely driven by two factors observed by the industry, firstly the potential as a strong nonclassical CMOS contender in continuing along the ITRS roadmap and secondly for applications in low standby power and RF device markets due to the low cost process and compatibility with CMOS technology. The recent vMOSTs can be mainly classified into two types according to the two different fabrication processes in defining the channel and source/drain regions, namely epitaxy and implantation respectively. Fig. 2 illustrates generic architectures.

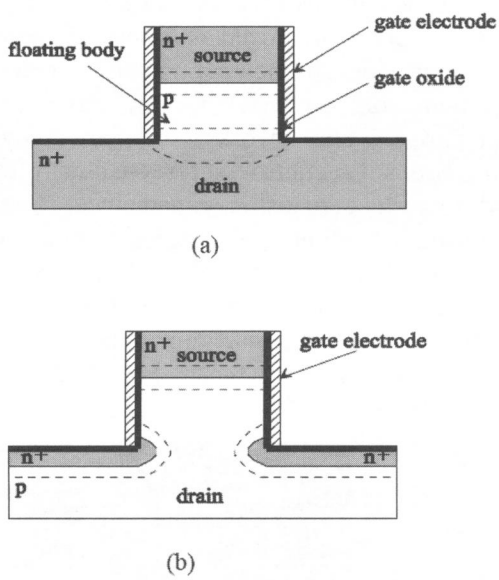

Fig. 2. Generic vMOST architectures: a) epitaxial, b) ion-implanted.

A classical epitaxially grown vMOST with channel length down to 70nm precisely defined by the thickness of a silicon film using LPCVD was reported in [2, 3]. The channel is uniformly doped. The sidewall interface quality was enhanced by the deposition and etching of a sacrificial oxide layer before the gate oxide growth. However, the biggest disadvantages of this device are the severe short channel effects (SCE), floating body effects and high overlap capacitance. To suppress the SCE without compromising on-current, a technology was later reported using MBE instead of LPCVD to grow a highly doped thin layer in the center of the body as a 'junction field stopper' [4]. Additionally, compared to homogeneously doped body this delta doping profile also served to reduce the hot carrier effects due to the reduced average drain electric field along the channel and thus improved the breakdown voltage. However, the application of this device in RF application is limited due to the large overlap capacitance between the gate and the drain/source. A selective epitaxy method was proposed to solve this problem by depositing the poly gate layer previously to the selective epitaxial growth of the p+np+ junctions therefore reducing the overlap regions [5]. Because the floating body effect still remained as an important issue inducing severe parasitic bipolar effect in aforementioned epitaxial devices, a SiGe source layer was developed to suppress majority carrier (hole) accumulation and consequently, offset avalanche breakdown [6]. For ultra short channel device especially with p type channel, SiGeC layers were also seen as important technology to suppress the dopant diffusion from the drain and source, which would lead to severe bulk punch through [7].

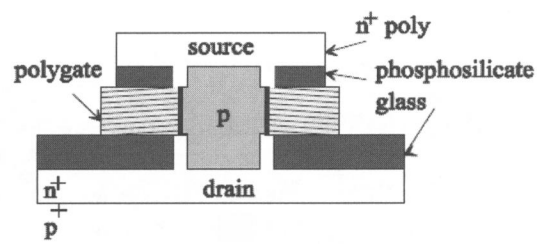

Fig. 3. Replacement gate scheme.

The overlap capacitance problem for the epitaxial vMOST has been addressed by incorporating a process of replacement gate [8] as shown in Fig. 3. In that work, after etching of the dummy gate, the poly gate was self-aligned with the previously grown channel and therefore the overlap region was largely limited. In the device junction depth could be controlled by the solid source diffusion (SSD). However, shallow junctions were still difficult to form because of the limitation of the thermal budget for annealing. More recently, an ultra thin vertical channel nMOSFET process that can simultaneously address the aforementioned short channel and parasitic issues especially overlap capacitance problems was reported in

[9]. In this device, a replacement gate process was used to allow LDD drain region self-aligned with the gate, thus largely limiting the overlap region of which the rest is isolated by SiN layers. The ultra thin body effectively suppresses the SCE with the aid of a boron-doped poly-$Si_{0.5}Ge_{0.5}$ gate to adjust the threshold voltage. However, the process brought problems of high series resistance in contacts and drain/source regions together with poor sidewall interface quality because of the difficulty of incorporating the sacrificial oxide step. A process for threshold voltage adjustment involving only a BSG film has been reported, to allow the Si body surface to be doped accordingly, thus precluding the poly gate doping design [10].

The vMOSTs fabricated through an etching and implantation process were first discussed in [11]. Unlike the epitaxial processes, the channel, drain and source regions are defined by ionimplantation. This approach has the significant advantages of simplicity and full compatibility with conventional planar CMOS technology. In other work, the on-current in such implanted devices was enhanced by implantation of Ge into the channel region [12]. As a result, the channel mobility is enhanced and also the on-current is further increased due to the intensive field at the gradual SiGe drain junction? The impact of the sidewall interface orientations on gate oxide thickness, interface state density and inversion layer mobility was assessed in other work [13]. The overlap capacitance problem in implanted vMOST was addressed by using a simple selfaligned process which is less complicated than in the epitaxial channel devices [14, 15]. However, the performance of implanted devices was degraded by the onset of short channel effects. One proposed solution was to implant a graded channel doping which has high doped end near the source [16]. In this way, the source junction barrier is enhanced that provides suppression on drain field penetration and also bulk punchthrough. The lightly doped drain end channel serves to increase the carrier mobility and reduce the impact ionization rate. The disadvantage of this approach is that the highly doped source end channel may have high band to band leakage.

Furthermore the device must be biased in source on top mode to allow aforementioned benefits realized. This does introduce some circuit design constraints and is also less than optimal for RF applications where a grounded source is required.

3. DESIGN ISSUES FOR VMOSTs

Figure 4 shows a generic vMOST whereby channels are formed on the vertical sidewalls of etched pillars.

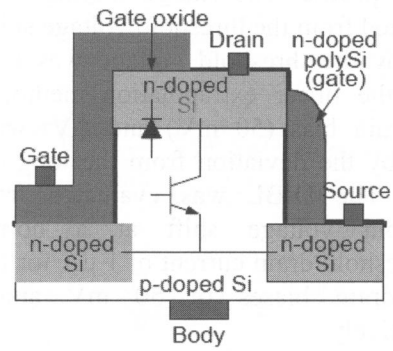

Fig. 4. Generic Vertical MOSFET.

The source and drain can be assigned to either the top or the bottom of the pillar but as is apparent from the figure, a considerable asymmetry is evident for these regions. The bottom contact region can be formed by an angled implant followed by a drive-in to ensure the doped region encroaches around the corner of the pillar thus ensuring full gate control of the channel. In contrast, the top contact is easily formed by an implant into the top of the pillar. Thus a shallow junction is formed at the bottom and a very deep junction at the top. The latter has severe consequences for control of short channel effects. Furthermore, it is evident that there is a considerable degree of gate overlap with source and drain regions which results in very high parasitic overlap capacitance. We observe also that a large area parasitic bipolar transistor is evident together with a large area parasitic diode at the top of the pillar. In the following subsections we summarise some of our recently reported strategies to address the two main related issues of control of short channel effects (SCE) and parasitic capacitance.

Device simulations were conducted using Silvaco Atlas. We included the hydrodynamic and Bohm Quantum Potential models to

account for non-equilibrium carrier temperature and quantum potential effects respectively. The Lombardi CVT mobility model was adopted together with Fermi-Dirac statistics and bandgap narrowing. vMOSTs are compared with lateral n-MOSFET structures. Body doping was set at $1x10_{18}$ cm_{-3}, channel length was 70nm and gate oxide thickness was 2 nm. The vMOST has a constant top junction depth. The bottom junction depth was varied from 5 nm to 100 nm, with an abrupt junction doping profile. The charge sharing (CS) was evaluated from the threshold voltage shift, ΔV_T whereby the threshold voltage was extracted using the linear extrapolation method under low drain bias (50 mV) and ΔV_T was then given by the deviation from the long channel value. The DIBL was evaluated from the threshold voltage shift at a normalized subthreshold drain current of 1 μA for low and high drain biases of 50 mV and 1 V respectively.

3.1 Channel Design

We first address the SCE in the generic vMOST. Fig. 5 shows DIBL and CS as a function of bottom junction depth for vMOSTs with varying bottom junction depth in both drain on top (DoT) and drain on bottom (DoB) configuration. A lateral MOSFET structure with varying source and drain junction depths is shown for comparison.

The smaller DIBL and CS values for the lateral MOSFET indicate the superiority of symmetrical junctions. However, the DIBL curve for the case of variable drain junction depth in DoB configuration, illustrates a similar behaviour to that of the symmetrical structure. All three curves also show similar limiting behaviour at large drain/source junction depths for both DIBL and CS.

These results indicate a generic problem for vMOST design. We have suggested a solution based on the concept of the 'dielectric pocket' also referred to as 'junction stop (JS)' [17, 18] and the architecture is shown in Fig. 6. The JS essentially forms a hard mask on top of the pillar which allows formation of a shallow top junction by out-diffusion from the poly-Si top contact region. The details of the process can be found elsewhere [18]. We draw attention to the gap between the JS and the gate oxide depicted in Fig. 6. The width of this region is crucial in defining the junction depth.

In the simulations of the vMOSTs-JS, the drain spacer width is varied from 3 nm to 80 nm yielding a drain junction depth in the range 5 nm to 100 nm. The junction stop has a thickness of 20 nm.

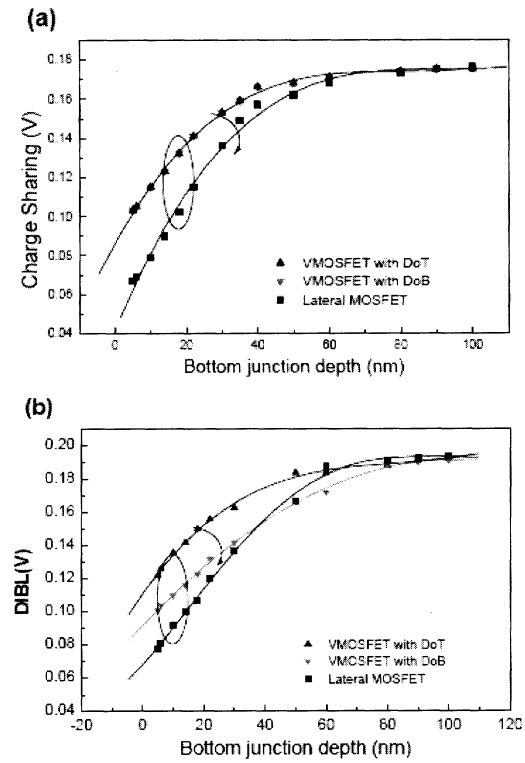

Fig. 5. (a) Charge sharing and (b) DIBL as a function of bottom junction depth for a vMOST and a conventional lateral MOSFET. Three cases are compared: (1) a vMOST in DoT configuration; (2) a vMOST in DoB configuration; (3) a conventional lateral MOSFET with identical drain and source junction depths. The devices were simulated with Vds=50 mV and Vgs=1 V for charge sharing and Vds=1 V and Vgs=50 mV for DIBL.

Simulation results of SCEs are shown in Fig. 7 for devices biased in the DoT configuration with different JS spacer widths and therefore different drain junction depths. The devices have a body doping of $1x10^{18}$ cm^{-3} and a 30 nm source junction depth. The results indicate that when the drain junction depth exceeds 50-60 nm, the JS loses electrical influence on the SCEs and the device behaves as a 'conventional' vertical vMOST. When the drain junction depth is reduced to 20 nm, the CS and the DIBL are reduced by nearly 50 mV.

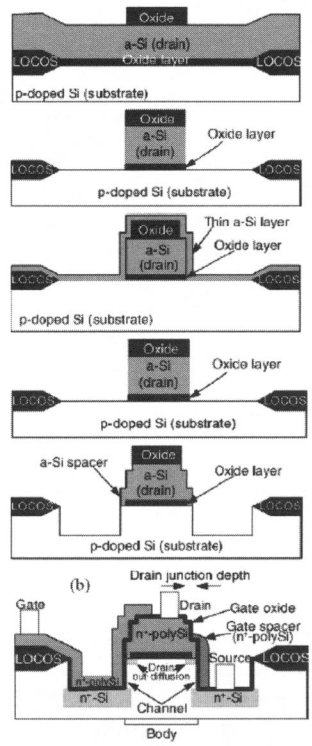

Fig. 6. Bottom figure shows the vMOST incorporating a junction stop at top of pillar. The figures above show the outline of the associated fabrication process.

A further advantage of the JS is that it allows for a decrease of the channel doping. Simulation results (not shown) of DIBL for vMOSTs with and without a JS in the DoT configuration, as a function of body doping show that a body doping of $8x10^{17}$ cm^{-3} demonstrates a DIBL value of 166mV, but the same value can be achieved with body doping of $5x10^{17}$ cm^{-3} if a JS is incorporated. This reduced doping leads to higher channel mobility and hence on-current.

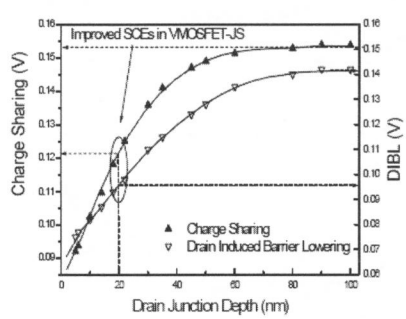

Fig. 7. Simulations of DIBL and CS as a function of reducing drain junction depth in a vMOST with a junction stop (vMOST-JS). Improved SCEs are obtained for shallower drain junctions. All the devices are biased in DoT configuration, with a body doping of $1x10^{18}cm^{-3}$ and a source junction depth of 30 nm.

The simulation results above have demonstrated the increasing efficacy of the JS on DIBL control in devices with lower body doping. Lower channel doping yields higher channel mobility, thus a doping trade-off can be enabled to enhance the I_{on}/I_{off} ratio.

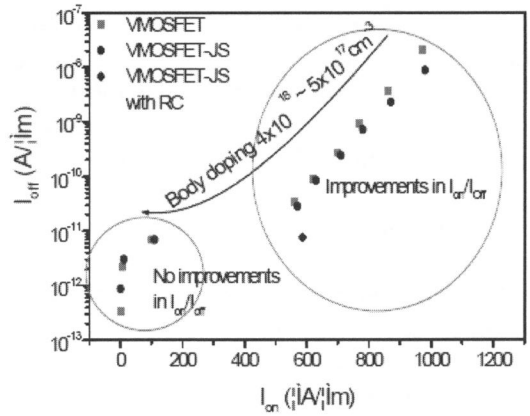

Fig. 8. Ioff as a function of Ion for vMOST and vMOSTJS devices with different body doping levels. The arrow shows the direction of increasing body doping. Also shown is a point for a retrograde channel vMOST - JS (vMOST-JS with RC) with a channel doping of 5×10^{16} cm^{-3} and a body doping of 4×10^{18} cm^{-3}.

The benefits are shown in Fig. 8 where I_{on} vs. I_{off} is plotted for both vMOSTs and vMOST-JSs. For high body doping (left hand side of the graph) the JS provides little improvement in the I_{on}/I_{off} ratio, but at low body doping (right hand side of the graph) the JS gives a significant improvement in the I_{on}/I_{off} ratio. For body dopings of $5.0x10^{17}$ cm^{-3} and $6.0x10^{17}$ cm^{-3} the JS gives improvements in I_{off} of 58.7% and 37.8% respectively for a given I_{on}.

3.2 Leakage and Latch-Up

As we have seen, it is a property of vMOSTs, that the source and drain junctions are inherently asymmetric. It follows that gate overlaps are in turn inherently different. We have investigated the effect of the asymmetric source and drain geometries of surround-gate vMOSTs on the drain leakage currents and gate-induced drain leakage (GIDL) in the OFF-state region of operation for both drain-on-top and drain-onbottom configurations [19]. Asymmetric leakage currents are seen when the source and drain terminals are interchanged, with the GIDL being higher in the drain-on-bottom configuration and the

body leakage being higher in the drain-on-top configuration. Temperature dependence together with voltage dependence of the leakage currents show that band-to-band tunneling is the dominant leakage mechanism for both the GIDL and body leakage from electrical measurements at temperatures ranging from 50 to 200°C. The asymmetric body leakage was explained by a variation in body doping concentration down through the pillar due to the use of a well ion implantation. The asymmetric GIDL was explained by the difference in gate oxide thickness on the orthogonal sidewall (110) and horizontal (100) crystal planes.

The junction stop concept brings the added benefit of reducing considerably the area of the top contact which for a DoT configuration, corresponds to the collector of the parasitic bipolar transistor (PBT) formed by the source and drain of the vMOST. Consequently, the magnitude of base and collector currents of the PBT is considerably reduced. The DP device is however inherently 'drain up.' An alternative approach to minimise parasitic bipolar transistor gain for drain-down configurations (DoB), is to include a poly-SiGe extrinsic source contact.

This serves to steepen the profile of minority carriers injected into the parasitic emitter so increasing the base current and reducing the gain. A theoretical model and experimental proof of the concept in the context of a bipolar transistor technology has been presented in [20].

3.3 Parasitic Capacitance

The higher parasitic capacitances compared to conventional lateral MOSFETs represents a major disadvantage for vMOSTs. We have developed technology whereby thickened oxide regions can be realised, as depicted in Fig. 9. Reduction of gate-source overlap capacitance (bottom of pillar) is achieved by a LOCOS type process which we designate fillet local oxidation (FILOX) [21].

Fig. 10 shows a field emission SEM cross-section of an nvMOST featuring this approach. Incorporation of a deposited oxide region on top of the pillar and the thicker oxide grown on the highly doped poly-Si extrinsic drain contact can reduce significantly the gate-drain capacitance.

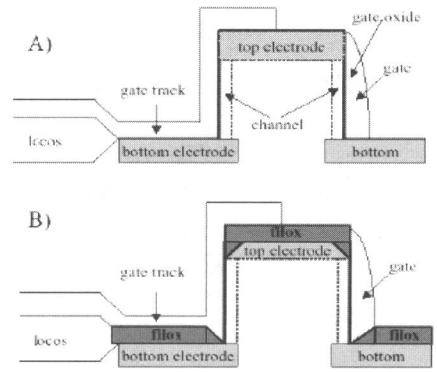

Fig. 9. Incorporation of thickened oxide regions as shown above can reduce significantly the overlap capacitances from case A, to B.

A study using MOS-capacitors has demonstrated a 5-fold reduction in parasitic overlap capacitance using FILOX and a thick top oxide [21]. To summarise the study, we show in Fig. 11, CV plots for pillars with gate oxide only, with a 20 nm thermal oxide-130 nm CVD nitride and 50 nm LTO stack (ONO) and finally the ONO stack plus the FILOX process. The ONO stack reduces the capacitance by 30% and the introduction of the FILOX gives the reduction overall of a factor 5.

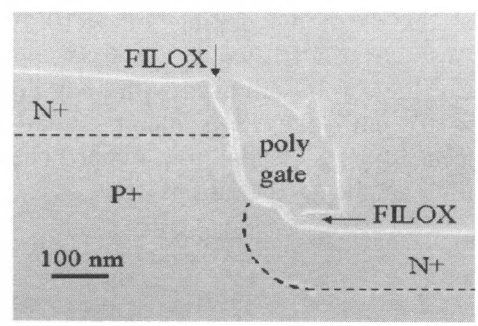

Fig. 10. SEM cross section showing the thickened oxide regions designated FILOX.

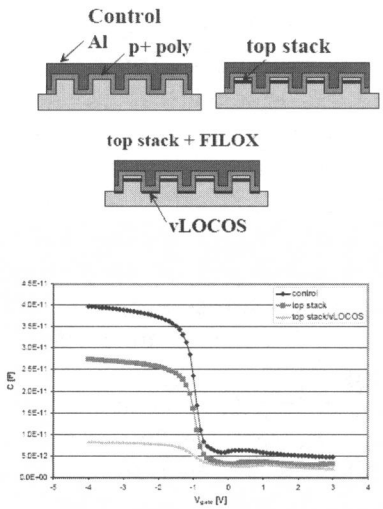

Fig. 11. MOS capacitor study showing 5 times reduction in capacitance due to the presence of FILOX layers.

Figure 12 shows the results of calculations for transistor structures. It is evident that significant reductions in C_{GS} and C_{GD} can be realised using the FILOX process.

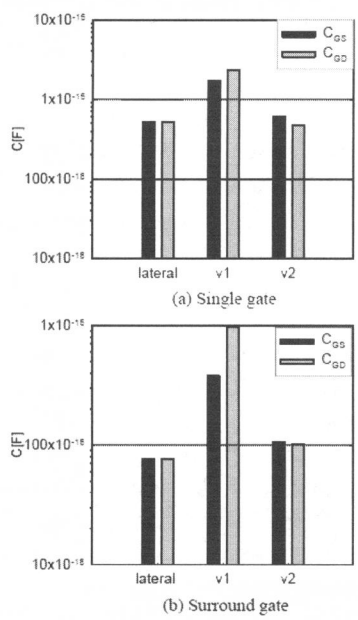

Fig. 12. Calculations of overlap capacitances comparing lateral, single and gate all around MOSFETs.

4. FURTHER DEVELOPMENTS

A particular feature of vMOST technology is the ease by which large aspect ratio and multi gate devices can be realised. We have reported a process whereby appropriate masking allows us to realise single, double and gate-all-around architectures relatively easily [22] as shown in Figure 13. Good device characteristics as shown in Fig. 14, have been obtained and the technology allows an easy route to investigating the properties of such structures.

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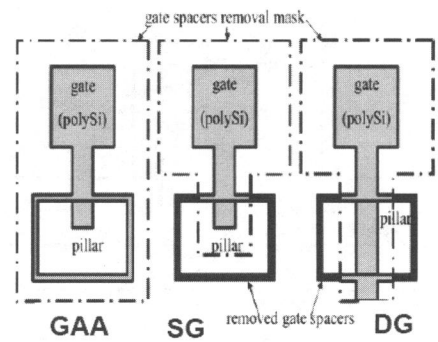

Fig. 13. Masking scheme to realise single (SG), double (DG) and gate-all-around (GAA) vMOSTs.

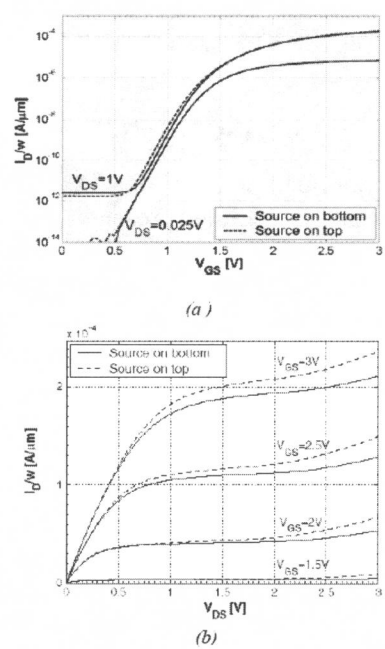

Fig. 14. Transfer characteristic(a) and output characteristic (b) of a surround gate vMOS transistor with channel width 24um and approximate channel length 125 nm.

The devices discussed so far and more appropriate for use in RF application. For advanced digital application, it is desirable to scale the pillar width to smaller dimensions such that full depletion is achieved for double gate configuration. This can bring many benefits such as volume inversion, enhanced mobility and hence on-current. However, scaling of the pillar width introduces floating body effects because the depletion regions associated with the bottom contacts tend to merge before those associated with the channel regions within the pillars, as depicted in Fig. 15 [23]. Thus floating body effects, similar to those of SOI devices, can become apparent.

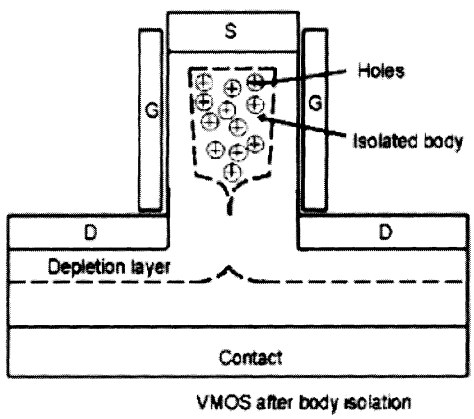

Fig. 15. Schematic cross-sectional views of vMOST operated in the depletion-isolation mode.

5. DISCUSSION

The continued scaling of MOSFETs to the decananometre regime presents very major technological challenges to the industry and will require enormous investment in plant and equipment. Vertical transistors are currently of interest because they offer an alternative route to ultra-short channel MOS transistors with relaxed lithography requirements, and hence considerably lower costs.

It is worth pointing out that there is little research so far on the potential and feasibility of vertical MOSFETs as medium power RF devices aimed at the highly lucrative 1-10 GHz market. In this context, the key advantages of the vMOSFET are the ability to use relaxed lithography (0.35μm say) to produce a very short channel (sub-0.1μm) transistor. Furthermore, with vertical MOSFETs, surround gates can be easily produced and provide a very high aspect ratio in a very small silicon area. Both advantages to contribute to very high transistor transconductance, g_m, and $f_T \approx g_m/C_{gat.}$, and hence provide a device with a high LF gain, $A_V \approx g_m/g_d$ and a high bandwidth, $f_T \approx g_m/C_{gate}$.

The widespread adoption of modern cellular, satellite and wireless connectivity systems depends critically on the availability of low cost, high integration semiconductor technology.

Enormous strides have been made in recent years in realising cellular and wireless connectivity systems in a few ICs with very low external component counts. Typical 900MHz and 1.8GHz GSM designs now have a single smallsignal RF system IC, including LNA, VCO, mixers, all channel filtering, and low power transmit driver [24]. IEEE802.11 systems are similarly integrated at the 2.4 and 5.5GHz ranges [25].

Traditionally, such small signal RF ICs have been fabricated in advanced Si or SiGe BiCMOS technologies, with bipolar f_T figures of 40-60GHz, and many quite good passive components available. However, as CMOS technology is scaled, the usable bandwidth increases with the decreasing channel length. Typical f_T values are of the order of 50GHz for 0.25μm, 65GHz for 0.18μm, and 130GHz expected for 0.09μm. In GSM, 2.4GHz and 5.5GHz WLAN applications, CMOS [CSR, Bluetooth, Atheros WLAN] has been shown to be capable of delivering satisfactory performance and high integration in practical transceiver circuits, with very few process modifications, and the possibility of integrating GSM RF and digital baseband in a single CMOS chip is now becoming reality.

Alongside the increase in f_T comes the reduction in operating voltage. This poses challenges in the design of high linearity front end circuits, where significant operating currents are needed while maintaining enough headroom to avoid compression. Less obvious is the VCO circuit; these work best with large signal swings since the carrier to phase noise ratio is then maximized. MOS devices are generally preferred for this reason, albeit with the limitation imposed by the power supply. A higher working supply and a high bandwidth device make the design trade-offs easier here.

Finally we come to the transmit path, which is a particular challenge for CMOS. To obtain a (relatively) large output power (ie, of the order of +20 to +30dBm) with a low supply voltage there will be large currents and potentially large losses; we also require wide devices driven with large gate swings. Hence driving the driver itself and matching its output is something of a challenge. Using an inherently higher bandwidth device at this point, i.e. with larger g_m for a given input capacitance, eases the internal drive and hence power consumption. Raising the power supply voltage means that the losses of the stage can be increased and the matching becomes easier. If one can use a direct battery connection, then the losses of a DC-DC converter are removed.
From the above discussion one can see that with the availability of vertical MOSFET devices incorporated in a mature mainstream CMOS technology, there are significant opportunities for the design of highly integrated radio systems which can include a low power PA or relatively strong transmit driver on relatively inexpensive substrates.

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