Chapter 8
Test Strategies for Multi-Voltage Designs

Saqib Khursheed and Bashir M. Al-Hashimi

Abstract Reducing the power consumption of digital designs through the use of more than one Vdd value (Multi-Voltage) is known and well practiced. Some manufacturing defects have Vdd-dependency, which implies defects can become active only at certain power supply setting, leading to reduced defect coverage. This chapter presents a coherent overview of recently reported research in testing strategies for multi-voltage designs including defect modelling, test generation and DFT solutions. The chapter also outlines number of worthy research problems that need to be addressed to develop high quality and cost effective test solutions for multi-Vdd designs.

8.1 Introduction

Minimizing power consumption through the use of low power design techniques has been an active research area for nearly two decades, motivated by the portable and hand-held devices application market. The operating voltages needed for such designs are generated either through dedicated multiple power supplies on chip [Hamada et al. 1998] or through adaptive voltage scaling circuitry consisting of DC-DC converters and voltage controlled oscillators [Lee and Sakurai 2000]. These techniques operate gates or circuits not on the critical path of a design at lower operating voltage than those on the critical path thereby achieving low power without compromising performance. Commercial CAD tools support multi-Vdd design approach (Synopsys *galaxy*^{TM}) and for that reason it is normally employed in designs where power consumption is a key requirement. This chapter addresses the following general question, “Can existing test techniques be used to test multi-Vdd

Saqib Khursheed
University of Southampton, Southampton, SO17 1BJ, UK, e-mail: ssk06r@ecs.soton.ac.uk

Bashir M. Al-Hashimi
University of Southampton, Southampton, SO17 1BJ, UK, e-mail: bmah@ecs.soton.ac.uk

designs?" The simple answer is yes and to ensure high defect coverage it is necessary to repeat the test at all operating voltages of the design since some defects show Vdd-dependency. This may not be viable in designs where cost is of great importance as the case with hand-held devices market. Recently researchers have started to develop specific test solutions to multi-Vdd designs where the aim is to improve defect coverage without the need to repeat the test at all operating voltages of the design. Testing multi-Vdd designs is an orthogonal problem to Very Low Voltage (VLV) testing [Hao and McCluskey 1993], which was proposed over a decade ago to improve reliability. It was shown that testing between $2V_t$ and $2.5V_t$, where V_t is the transistor threshold voltage, achieves high defect coverage for resistive bridges. The differentiation is that in multi-Vdd designs there are a number of operating Vdds, in practice up to four, and the aim of multi-Vdd test is to determine the minimum number of voltage settings to ensure the highest level of defect coverage.

In this chapter we outline recent findings for two major types of defects: resistive bridge and resistive open in the context of multi-Vdd designs. A non-resistive defect (e.g., a short) between an interconnect line and power supply (Vdd) or ground rail (Gnd) can be modeled using a stuck at fault model, which represents permanent failure of the line in terms of stuck-at 1 (short with Vdd) or stuck-at 0 (short with Gnd) respectively. Such type of failures do not show Vdd dependent detectability[1] and therefore are not discussed in this chapter. Sections 8.2 and 8.3 discuss test techniques for resistive bridge and resistive open defects in the context of multi-Vdd designs. The DFT technique for devices employing multi-Vdd is discussed in Section 8.4, with the aim to achieve cost-effective test as well as reducing power dissipation during test. Section 8.5 provides a summary of emerging and new test research problems and finally, Section 8.6 concludes the chapter.

8.2 Test for Multi-Voltage Design: Bridge Defect

Resistive bridge represent a major class of defects for deep submicron (DSM) CMOS. It is due to an un-wanted metal connection between two lines of the circuit, which deviates the circuit from its ideal behavior. A typical resistive bridge is shown in Fig. 8.1. A study on **resistive bridge distribution** is reported in [Rodriguez-Montanes et al. 1992] based on 14 wafers from different batches and production lines. The study shows that around 96% of bridges have a resistance value which is less than 1 kΩ. On the other hand, a physical defect between an interconnect line and power supply (Vdd) or ground rail (Gnd) is referred to as hard-short (bridge with 0 Ω resistance). It was shown in [Khursheed et al. 2009b] that detectability of hard-short is irrespective of Vdd settings and therefore is not further discussed in this chapter.

[1] Stuck-at fault model does not capture physical complexities at the fault site and therefore more complex fault models have evolved to improve testability of the design. For a comprehensive discussion on evolution of fault models see [Delgado 2008].

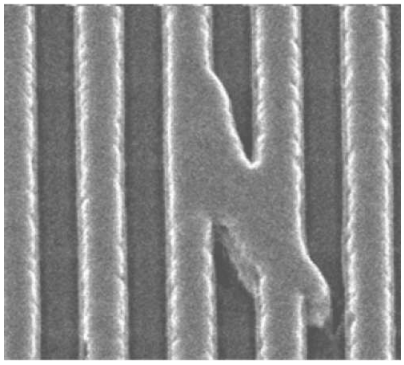

Fig. 8.1: Resistive Bridge [Kundu et al. 2001].

This section discusses **modelling and test generation of resistive bridge** for multi-Vdd designs. Section 8.2.1 describes the analog and digital behavior of resistive bridge at single voltage setting. This is further extended by showing Vdd-dependency of resistive bridge in Section 8.2.2. Finally, Section 8.2.3 provides a summary of recently reported research related to cost-effective testing of resistive bridge for multi-Vdd designs.

8.2.1 Resistive Bridge Behavior at Single Vdd Setting

The resistance of a bridge is a continuous parameter which is not known in advance. A recent approach based on interval algebra [Engelke et al. 2004], [Engelke et al. 2006b] allowed treating the whole continuum of bridge resistance values R_{sh} from 0 Ω to ∞ by handling a finite number of discrete intervals. The key observation which enables this method is that a resistive bridge changes the voltages on the bridged lines from 0 V (logic-0) or Vdd (logic-1) to some intermediate values, which will be different for different R_{sh} values. The logic behavior of the physical defect can be expressed in terms of the logic values perceived by the gate inputs driven by the bridged nets based on their specific input threshold voltage.

A typical bridge fault scenario is illustrated in Fig. 8.2. D1 and D2 are the gates driving the bridged nets, while S1, S2, S3 and S4 are successor gates, i.e. gates having inputs driven by one of the bridged nets. The resistive bridge affects the logic behavior only when the two bridged nets are driven at opposite logic values. For example, consider the case when the output of D1 is driven high and the output of D2 is driven low. For illustration, we assume that the shown bridge R_{sh} affects only the output of D1, i.e., S1, S2 and S3 are affected by the resistive bridge. The dependence of the voltage level on the output of D1 (V_O) on the equivalent resistance of the physical bridge is shown in Fig. 8.3. The deviation of V_O from the ideal voltage level (Vdd) is highest for small values of R_{sh} and decreases for larger values

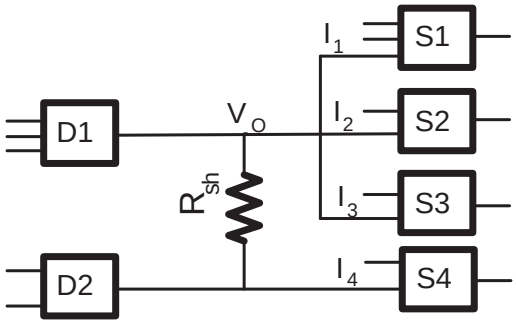

Fig. 8.2: Example of a Resistive Bridge fault.

of R_{sh}. To translate this analog behavior into the digital domain, the input threshold voltage levels V_{th1}, V_{th2} and V_{th3} of the successor gates S1, S2 and S3 have been added to the V_O plot. For each value of the bridge resistance R_{sh}, the logic values at inputs I_1, I_2 and I_3 can be determined by comparing V_O with the input threshold voltage of the corresponding input. These values are shown in the second part of Fig. 8.3. Crosses are used to mark the faulty logic values and ticks to mark the correct ones. It can be seen that, for bridge with $R_{sh} > R_3$, the logic behavior at the fault site is fault-free (all inputs interpret the correct value), while for bridge with R_{sh} between 0 and R_3, one or more of the successor inputs are interpreting a faulty logic value. The R_{sh} value corresponding to R_3 is normally referred to as "critical resistance" as it represents the crossing point between faulty and correct logic behavior. Methods for determining the critical resistance have been presented in several publications [Sar-Dessai and Walker 1999], [Engelke et al. 2006b].

A number of bridge resistance intervals can be identified based on the corresponding logic behavior. For example, all bridges with $R_{sh} \in [0, R_1]$ exhibit the same faulty behavior in the digital domain (all successor inputs interpret faulty logic value). Similarly, for bridges with $R_{sh} \in [R_1, R_2]$, successor gates S2 and S3 interpret the faulty value, while S1 interprets the correct value. Finally, for bridges with $R_{sh} \in [R_2, R_3]$ only S3 interprets a faulty value while the other two successor gates interpret the correct logic value. Consequently, each interval $[R_i, R_{i+1}]$ corresponds to a distinct logic behavior occurring at the bridge fault site. The logic behavior at the fault site can be captured using a data structure further referred to as logic state configuration (LSC), which can be looked at as logic fault model [Khursheed et al. 2008]. The union of the resistance intervals corresponding to detectable faults forms the Global Analogue Detectability Interval (G-ADI) [Engelke et al. 2006b]. Basically, G-ADI represents the entire range of detectable physical defects. Given a test set TS, the Covered Analogue Detectability Interval (C-ADI) represents the range of physical defects detected by TS. The C-ADI for a bridge defect is the union of one or more disjoint resistance intervals, the union of intervals corresponding to detectable faults [Renovell et al. 1996], [Engelke et al. 2004], [Engelke et al. 2006b], and [Engelke et al. 2006a]. The quality of a test set is estimated by measuring how

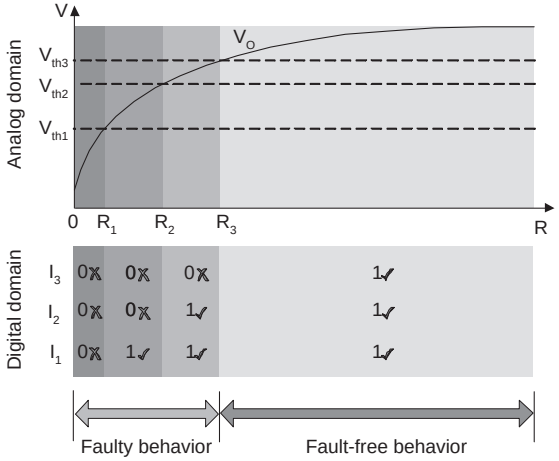

Fig. 8.3: Behavior of a bridge fault at a single Vdd setting in analog and digital domains.

much of the G-ADI has been covered by the C-ADI. When the C-ADI of test set TS is identical to the G-ADI of fault f, TS is said to achieve full fault coverage for f.

Several test generation methods for resistive bridge faults RBF have been proposed for a fixed supply voltage setting [Sar-Dessai and Walker 1999], [Maeda and Kinoshita 2000], [Shinogi et al. 2001], [Chen et al. 2005], and [Engelke et al. 2006a]. The method presented in [Maeda and Kinoshita 2000] is to guarantee the application of all possible values at the bridge site without detailed electrical analysis. In [Chen et al. 2005], the effect of a bridge on a node with fanout is modeled as a multiple line stuck-at fault. The study in [Sar-Dessai and Walker 1999], identifies only the largest resistance interval and determines the corresponding test pattern. In contrast to [Sar-Dessai and Walker 1999], the sectioning approach from [Shinogi et al. 2001] considers all the sections (resistance intervals) $[R_i, R_{i+1}]$. For each section, the corresponding LSC (and associated faulty logical behavior) is identified. This avoids the need for dealing with the resistance intervals and improves the test quality compared with [Sar-Dessai and Walker 1999], but the number of considered faults grows. In [Engelke et al. 2006a], the authors combined the advantages of the interval based [Sar-Dessai and Walker 1999] and the sectioning approach [Shinogi et al. 2001] into a more efficient test generation procedure by targeting the section with the highest boundaries first. Interval based fault simulation is then used to identify all other sections covered by the test pattern.

Prior research has analyzed the effect of varying the supply voltage on the defect coverage using pseudo random tests [Engelke et al. 2004]. The reported experimental results show that the fault coverage of a given test can vary both ways when the supply voltage is lowered, because not all faults can be covered using a single Vdd setting during test. However [Engelke et al. 2004] suggests that applying the tests at a lower supply voltage in addition to the nominal can improve the fault cover-

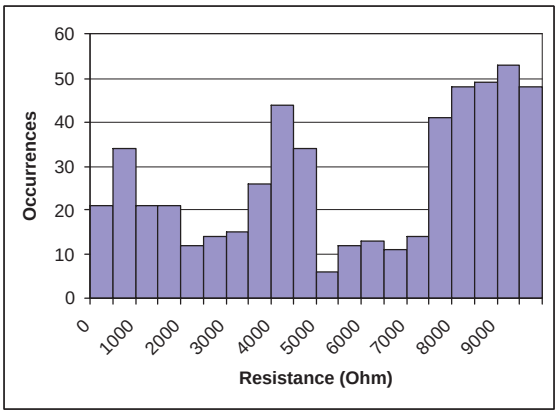

Fig. 8.4: Resistance values that cannot be detected at lowest Vdd setting [Khursheed et al. 2008].

age. This finding is further elaborated by Fig. 8.4. It shows the number of defects and respective resistance values, which cannot be detected (test escapes) at Vdd = 0.8 V (which would be a preferred Vdd for a 1.2 V process according to [Renovell et al. 1996], [Engelke et al. 2004]). The test escapes at 0.8 V, as shown in Fig. 8.4 is based on seven of the medium and large size ISCAS 85 and 89 benchmarks. The random spread of these defects across the resistance range suggests that to ensure high defect coverage it will be necessary to test at more than one Vdd setting for 100% defect coverage, as motivated by [Khursheed et al. 2008]. In the next section we explain why it may be necessary to use more than one Vdd setting during test to ensure full bridge defect coverage for multi-Vdd designs.

8.2.2 Resistive Bridge behavior at Multi-Vdd Settings

This section provides an analysis of the effect of varying supply voltage on bridge fault behavior. Fig. 8.5 show the relation between the voltage on the output of gate D1 (Fig. 8.2) and the bridge resistance for two different supply voltages Vdd_A and Vdd_B. The diagrams in Fig. 8.6 show how the analog behavior at the fault site translates into the digital domain. In this example, three distinct logic faults LF1, LF2 and LF3 could be identified for each Vdd setting. However, because the voltage level on the output of D1 does not scale linearly with the input threshold voltages of S1, S2 and S3 when changing the supply voltage (this has been validated through SPICE simulations), the resistance intervals corresponding to LF1, LF2 and LF3 differ from one supply voltage setting to another. This means that a test pattern targeting a particular logic fault will detect different ranges of physical defects when applied at different supply voltage settings. For example, at Vdd_A, a test pattern

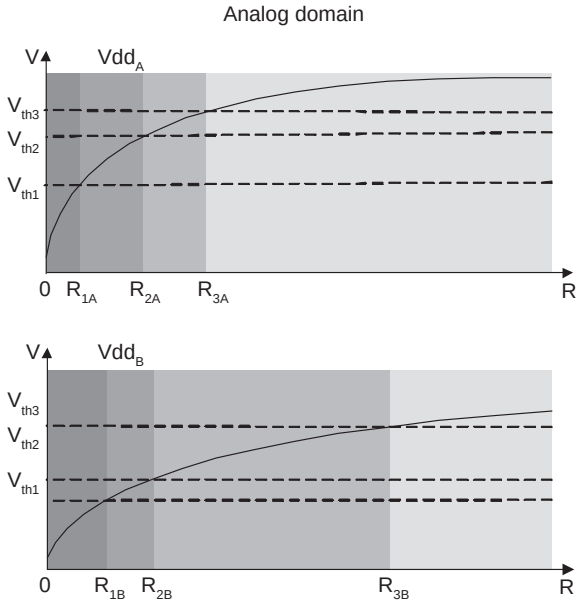

Fig. 8.5: Effect of supply voltage on bridge fault behavior: Analog domain [Khursheed et al. 2008].

targeting LF3 will detect bridge with $R_{sh} \in [R_{2A}, R_{3A}]$, while at Vdd_B it will detect a much wider range of physical bridge ($R_{sh} \in [R_{2B}, R_{3B}]$). Analysing this from a different perspective, a bridge with $R_{sh} = R_{3B}$ will cause a logic fault at Vdd_B but not at Vdd_A. To demonstrate the need for using multiple Vdd settings during test we use the following two scenarios. In Case 1 (Fig. 8.7) all three logic faults LF1, LF2 and LF3 are non-redundant. Fig. 8.7 shows the ranges of bridge resistance corresponding to faulty logic behavior for the two Vdd settings (basically the G-ADI sets corresponding to the two Vdd settings). Previous work on test generation for bridge faults [Engelke et al. 2006a] has used the concept of G-ADI assuming a fixed Vdd scenario. [Ingelsson et al. 2007] has extended the concept of G-ADI to capture the dependence of the bridge fault behavior on the supply voltage by defining the multi-Vdd G-ADI as the union of Vdd specific G-ADIs for a given design.

$G\text{-}ADI = \bigcup G\text{-}ADI(Vdd_i)$

The overall G-ADI consists of the union of the two Vdd specific G-ADI sets. It can be seen that $G\text{-}ADI(Vdd_A)$ represents about 45% of the overall G-ADI while $G\text{-}ADI(Vdd_B)$ fully covers the overall G-ADI. This means that a test set detecting LF1, LF2 and LF3 will achieve full bridge defect coverage when applied at Vdd_B. In Case 2 from Fig. 8.7, only LF2 and LF3 are non-redundant, which means that there is no test pattern which can detect LF1. In this case, $G\text{-}ADI(Vdd_A)$ represents about 30% of the overall G-ADI while $G\text{-}ADI(Vdd_B)$ rep-

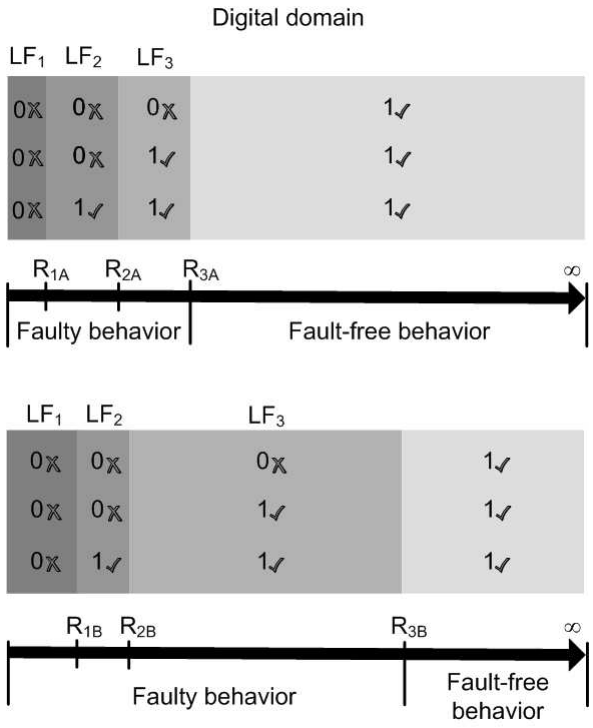

Fig. 8.6: Effect of supply voltage on bridge fault behavior: Digital domain [Khursheed et al. 2008].

resents about 90% of the overall G-ADI. This means that full bridge fault coverage cannot be achieved using a single Vdd setting.

From this analysis it can be concluded that to achieve full G-ADI coverage in a variable Vdd system, it may be necessary to apply tests at several Vdd settings. Instead of repeating the same test at all Vdd settings, which would lead to long testing times and consequently would increase the manufacturing cost, it would be desirable to be able to determine for each Vdd settings only the test patterns which effectively contribute to the overall defect coverage.

It has been shown in [Engelke et al. 2004] that the fault coverage of a test set targeting resistive bridge faults RBF can vary with the supply voltage used during test. This means that, depending on the operating Vdd setting, a given RBF may or may not affect the correct operation of the design. Consequently, to ensure high fault coverage for a design that needs to operate at a number of different Vdds, it may be necessary to perform testing at more than one Vdd to detect faults which manifest themselves only at particular Vdds. A Multi-Vdd Test Generation (MVTG) methodology is presented in [Khursheed et al. 2008], which computes a number of Vdd-specific test sets to achieve 100% defect coverage. In [Khursheed et al. 2008]

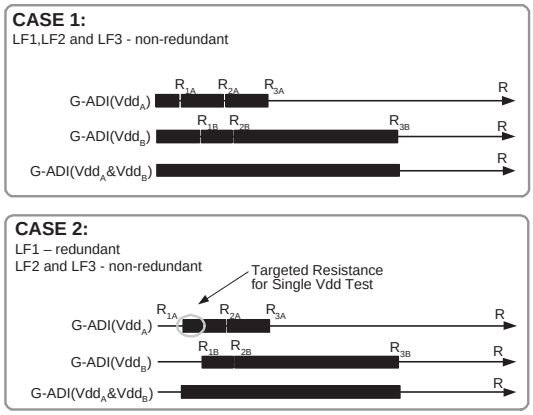

Fig. 8.7: Effect of supply voltage on bridge fault behavior: Observable bridge resistance ranges [Khursheed et al. 2008].

experiments are conducted using ISCAS-85' and 89' benchmark designs and fault list is compiled using coupling capacitance between neighboring nodes, these are most likely to form a bridge. Three Vdd settings are used for the experiment, i.e., 0.8 V, 1.0 V and 1.2 V and the outcome is tabulated in Table 8.1. The first two columns show the benchmark designs along with the number of faults extracted for each design. In this experiment, Synopsys *TetraMAX*^{TM} is used to generate a test set for each design, which is then fault simulated at 0.8 V (since higher resistive bridge fault coverage is achieved at a lower Vdd). The defect coverage achieved and the number of test patterns in the TetraMAX test-set are shown in the third main column of Table 8.1. Subsequently, MVTG [Khursheed et al. 2008] is used to generate top-up tests, targeting bridges that are not fully covered by the TetraMAX test-set. It is therefore used to provide the remaining defect coverage up to 100%. The sizes of the test sets generated by the MVTG top-up run are given in the fourth column for each Vdd setting. Finally, the total test pattern count is shown in the last column of Table 8.1, marked as "Tot.". From test flow point of view, it is therefore suggested to use MVTG [Khursheed et al. 2008] as a post-processing step to cover resistance intervals that remains uncovered by commercial ATPG tools.

8.2.3 Cost Effective Test for Resistive Bridge

In Section 8.2.2, it has been shown that more than one Vdd setting is required to achieve 100% defect coverage of resistive bridging defects. Switching between different Vdd settings during test is not a trivial task, and therefore a large number of Vdd settings required during test can have a detrimental effect on the overall cost of test. Consequently it would be desirable to keep the number of Vdd settings required

Table 8.1: Results of using Synopsys TetraMAX and Multi-Vdd Test Generation (MVTG) as a combined test generation flow for RBF [Khursheed et al. 2008].

		TMAX		MVTG top-up			
		0.8 V		0.8 V	1.0 V	1.2 V	Tot.
Design	# of RBF	DC	#tp	#tp	#tp	#tp	#tp
c1355	80	83	33	32			65
c1908	98	98	42	27			69
c2670	104	90	27	50			77
c3540	363	96	72	126	6	1	205
c7552	577	95	44	198		1	243
s838	34	88	17	17	2		36
s1488	435	96	82	82	2		166
s5378	305	95	60	123			183
s9234	223	89	48	92	2		142
s13207	358	95	60	89	5	1	155
s15850	943	98	56	144	4	5	209
s35932	1170	96	33	89	36	66	224

during test to a minimum. By analysing the scenario described in Case 2 (Fig. 8.7), it can be seen that full bridge defect coverage could be achieved using a single Vdd setting (Vdd_B), if the logic fault (LF) corresponding to the resistance interval $[R_{1A}, R_{1B}]$ (shown separately in Fig. 8.7), LF1 in this case, would become detectable at Vdd_B. Based on this observation, two techniques are available in literature and are summarized in this section.

8.2.3.1 Test Point Insertion

The first method to reduce Vdd settings during test is by using ***Test Point Insertion*** (TPI) as proposed in [Khursheed et al. 2008]. Test points are used to provide additional controllability and observability at the fault-site to detect resistance intervals at the desired Vdd setting, which are otherwise redundant and therefore helps reducing the number of test Vdd(s). This can be understood using Fig. 8.7, which shows marked resistance range is detectable only at Vdd_A. The TPI scheme proposed in [Khursheed et al. 2008] is used to cover the resistance interval at desired Vdd (Vdd_B) by providing additional controllability and observability using test points. In this case, Vdd_B is desirable as it covers most amount of detectable resistance range as shown in Fig. 8.7. Experimental results presented in [Khursheed et al. 2008] show that (TPI) can be used to reduce the number of Vdd settings during test, without affecting the defect coverage of the original test, thereby reducing test cost. One drawback with TPI scheme [Khursheed et al. 2008] is that it does not guarantee single Vdd test and usually results in more than one test Vdd settings. Experimental

results presented in [Khursheed et al. 2008] and more recently in [Khursheed et al. 2009a] show that TPI is unable to reduce test to single Vdd setting for majority of circuits. This can be understood from the following explanation. In Fig. 8.2, the gates used for driving the bridge (D1, D2) and the driven gates (S1, S2, S3, S4), influence the number of test Vdd(s) in a circuit. For the same circuit, assume that D1 is driving high and D2 is driving low, the output of D2 (V_O) on the equivalent resistance of the physical bridge is shown in Fig. 8.8, which shows that higher resistance range is covered at 1.2 V (non-preferred test Vdd) than at 0.8V (preferred test Vdd). This means that 1.2 V becomes essential test Vdd and TPI includes it for 100% defect coverage, as resistance range covered at 1.2 V can not be covered at 0.8 V.

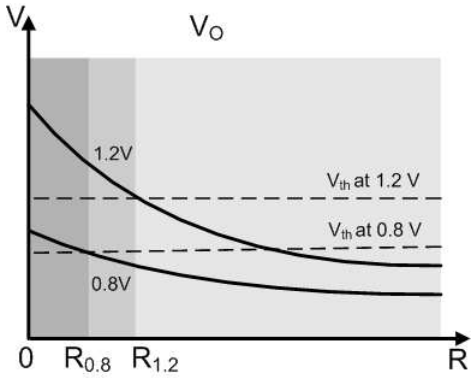

Fig. 8.8: Resistance range detection at different voltage settings.

8.2.3.2 Gate Sizing

Recently a new technique for reducing test cost of multi-Vdd designs with resistive bridging defect has been reported in [Khursheed et al. 2009a]. It targets resistive bridge that cause faulty logic behavior to appear at a non-desired test Vdd setting and uses ***Gate Sizing*** (GS) to expose the same physical resistance at preferred test Vdd. This is achieved by adjusting the drive strengths of gates driving the bridge, such that higher resistance is exposed at the desired Vdd setting. The drive strength of the gates driving the bridged nets can be adjusted to increase the voltages on the bridged nets (V_O in Fig. 8.2). This increase in voltage level can help expose maximum resistance at the desired Vdd setting thereby reducing the number of test Vdd settings; additionally it can also be used to cover resistance intervals (such as the one marked in Fig. 8.7) at the desired Vdd setting. This concept is illustrated by Fig. 8.9, which shows same pair of bridged nets as shown in Fig. 8.8 (derived from Fig. 8.2, where D1 is driving high and D2 is driving low), i.e., the logic thresh-

olds of the driven gates remain the same. In Fig. 8.9 it can be noticed that the voltage level V_O has increased such that $R_{0.8} > R_{1.2}$, by increasing the drive strength of the gates driving the bridge. This means that test generation will favor 0.8 V over 1.2 V, thereby reducing the number of test Vdd(s) and removing 1.2 V as a test Vdd and thus reducing total number of test Vdd settings. The drive current of a transistor I_{ds} is directly proportional to the gain factor β, which in turn is directly proportional to the W/L of the transistor. Thus replacing a gate with another having higher value of β (especially for transistors feeding the output) results in higher drive strength. This is feasible since, different versions of functionally equivalent gates are usually available in the gate library.

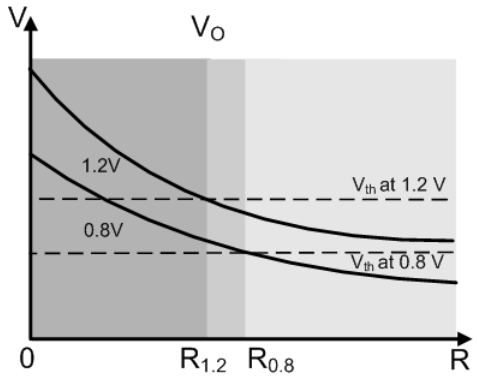

Fig. 8.9: Resistance range detection after adjusting the drive strength of the gates driving the bridge.

Experiments are conducted using ISCAS'85 and '89 full scan circuits, and results for TPI [Khursheed et al. 2008] and Gate Sizing [Khursheed et al. 2009a] are tabulated in Table 8.2. The first two columns show the benchmark designs and respective gate count in each design. The third main column (labeled as Test Vdd(s)) tabulates total number of test Vdd setting(s) for each of the original design (labeled as Orig.), by TPI [Khursheed et al. 2008] (labeled, TPI) and by the gate sizing technique (labeled, GS). As can be seen the GS technique is able to achieve 100% defect coverage at a single Vdd. This is unlike TPI, which requires two or more Vdd setting for most of the circuits to achieve the same defect coverage. Moreover, TPI is unable to reduce any test Vdd in case of c432 and c1908. The last main column of Table 8.2 (labeled as Gates) shows the number of gates replaced by gate sizing (GS) technique and the number of test points (control/observation points) added by TPI[2]. The number of gates replaced by GS technique ranges from 1-14, while TPI has added up to 28 test points.

[2] The number of test points is the sum of control and observation points.

Table 8.2: Results of Gate Sizing technique (GS) [Khursheed et al. 2009a] and its comparison with TPI [Khursheed et al. 2008].

CKT.	No. of Gates	Test Vdd(s)			Gates	
		Orig.	TPI	GS	GS	TPI
c432	93	All*	All	0.8 V	2	0
c1355	226	All	0.8 V	0.8 V	4	10
c1908	205	1.2 V, 0.8 V	1.2 V, 0.8 V	0.8 V	3	0
c2670	269	All	1.2 V, 0.8 V	0.8 V	6	19
c3540	439	All	1.0 V, 0.8 V	0.8 V	7	7
c7552	731	All	0.8 V	0.8 V	1	1
s344	62	1.2 V, 0.8 V	0.8 V	0.8 V	1	1
s382	74	1.2 V, 0.8 V	0.8 V	0.8 V	2	5
s386	63	All	1.2 V, 0.8 V	0.8 V	7	4
s838	149	All	0.8 V	0.8 V	14	28
s5378	578	All	1.0 V, 0.8 V	0.8 V	9	9
s9234	434	All	1.0 V, 0.8 V	0.8 V	6	2
s15850	1578	All	0.8 V	0.8 V	8	3

*All = 0.8 V, 1.0 V, 1.2 V

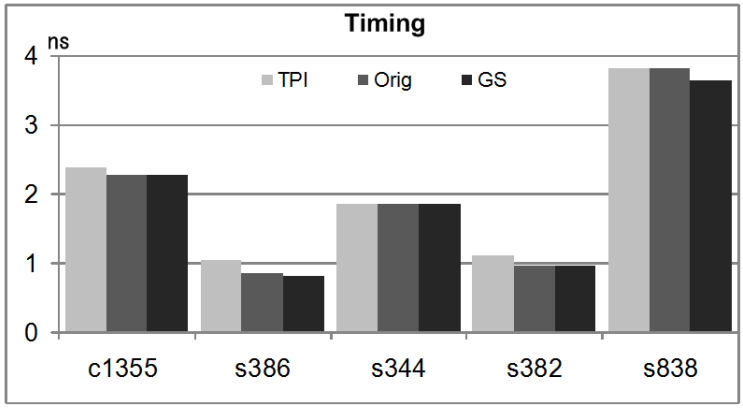

Fig. 8.10: Timing performance of TPI [Khursheed et al. 2008] and GS [Khursheed et al. 2009a] in comparison to the original design.

In another experiment reported in [Khursheed et al. 2009a], the timing performance of the original design (Orig), is compared with the design altered by Gate Sizing (GS) and by Test Point Insertion (TPI) techniques using Synopsys design compiler. Fig. 8.10 shows the timing performance, as can be seen the GS technique has little affect on the timing performance when compared to the original design. This is unlike the case with TPI, where the timing has increased because of test

points in critical path. It should be noted that for some circuits the GS technique has reduced timing than the original design due to larger and faster gates. Thus Gate Sizing technique represents an improvement over TPI, as it achieves 100% defect coverage at single test Vdd setting, while TPI mostly employs two or more test Vdd setting (Table 8.2). Furthermore, it has less cost of area, power and timing overhead as compared to TPI. For further details refer to [Khursheed et al. 2009a].

8.3 Test for Multi-Voltage Design: Open Defect

Section 8.2 considered test techniques for bridge defect, this section discusses test techniques for open defects, which is another dominant defect type commonly found in deep-submicron CMOS. It is due to unconnected nodes in a manufactured circuit that were connected in the original design and therefore deviates the circuit from ideal behavior. Open defects can be classified as full or strong opens with resistance greater than 10 MΩ and resistive or weak open with resistance less than 10 MΩ [Montanes et al. 2002]. Full open cause logic failures that can be tested using static tests (test patterns applied without timing consideration). On the other hand, resistive open show timing dependent effects and therefore should be tested using delay tests. Fig. 8.11 shows a cross-section of resistive open defect. In this section electrical characteristics of full open is discussed first, followed by resistive open.

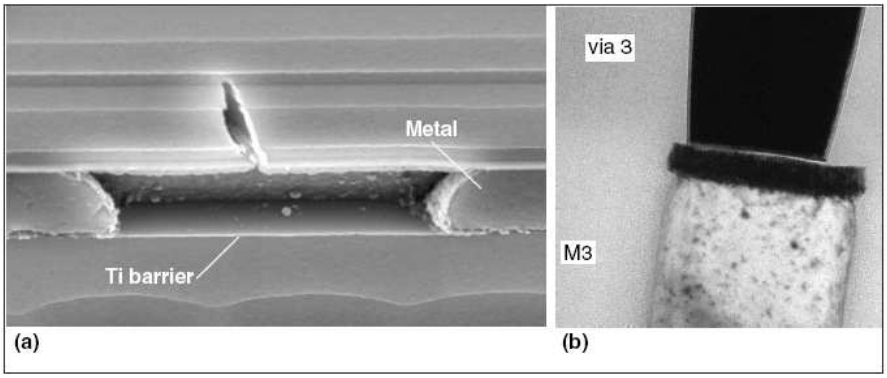

Fig. 8.11: Resistive or Weak Open Defects: (a) Cross section of metal open line; and (b) a resistive via [Montanes et al. 2002].

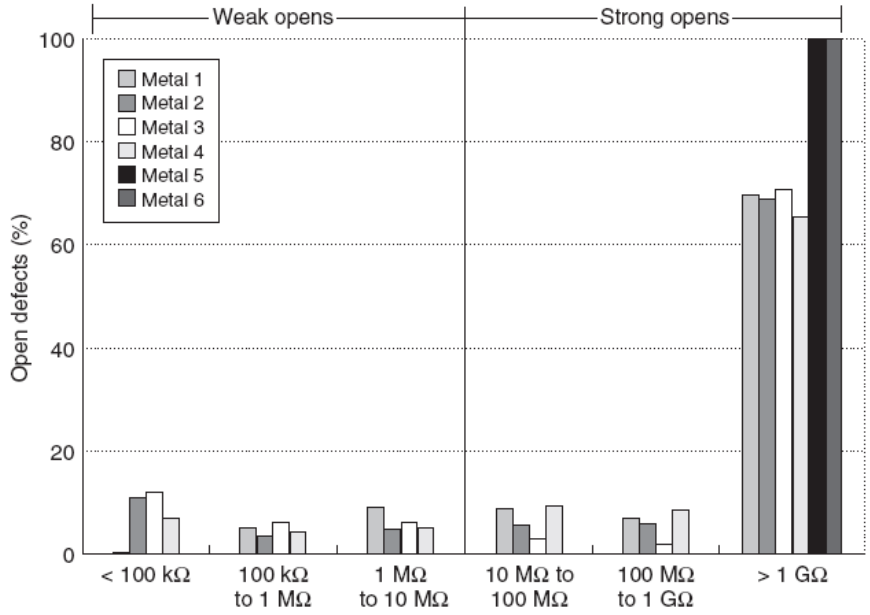

Fig. 8.12: Distribution of metal open resistances [Montanes et al. 2002].

8.3.1 Testing Full Open Defect

Fig. 8.12 shows **open defect distribution** in six different metal layers corresponding to 7440 dies from 12 lots, manufactured in 180 nm CMOS process. As can be seen, the majority of open defects can be categorized as strong or full open defects. Similar trend is reported for contact or via open [Montanes et al. 2002]. The occurrence frequency of full-open defects is expected to increase in future technologies [Sreedhar et al. 2008], [Arumi et al. 2008a]. Two fault models are available in literature for modelling full-open defects, which can be categorized as **capacitance based full-open fault model** [Henderson et al. 1991], [Johnson 1994], [Choudhury and Sangiovanni-Vincentelli 1995], [Rafiq et al. 1998] and **leakage-aware full-open fault model** [Lo et al. 1997], [Guindi and Najm 2003], [Sreedhar et al. 2008], [Arumi et al. 2008a]. Several recent studies have used capacitance based models [Gomez et al. 2005], [Zou et al. 2006], [Rodriguez-Montanes et al. 2007], [Spinner et al. 2008], [Arumi et al. 2008b] for testing full-open defects, which uses the following electrical characteristics: 1) the capacitance between floating line (disconnected from the driver node) and its neighboring line(s), 2) the parasitic capacitance due to transistors (PMOS and NMOS connected to floating line) driven by the floating net, and 3) the trapped charge on the floating net. If F represents a floating net that is disconnected from its driver, then voltage V_F is given by [Zou et al. 2006], and [Ingelsson 2009]:

$$V_F = \frac{C_{High}}{C_{High} + C_{Low}} V_{dd} + \frac{Q_{trap}}{C_{Gnd}} \quad (8.1)$$

where, V_F is voltage on the floating net, C_{High} and C_{Low} is capacitance due to neighboring lines driving high and low respectively (including capacitance due to V_{dd} and Gnd), V_{dd} is the supply voltage, $\frac{Q_{trap}}{C_{Gnd}}$ represents the trapped charge on the floating net. From (8.1), it can be noticed that for detecting full-open defects, V_F can be induced such that voltage on the floating net is higher than the logic threshold L_{th} voltage of the gate input, i.e., $V_F > L_{th}$, thereby exciting a stuck-at 1 fault. Voltage on the floating net can be induced by using test patterns that result in setting the neighboring nets to desired logic value, thereby increasing the fraction $\frac{C_{High}}{C_{High}+C_{Low}}$, as shown in (8.1). Similarly a stuck-at 0 fault can be induced on the floating net. The fault effect can then be propagated to any of the primary outputs for detection [Zou et al. 2006].

In nanometer CMOS ($\leq$ 90 nm), since the thickness of gate oxide is few tens of $\mathring{A}$, it does not act as a strong insulator. This results in higher gate-tunneling leakage current in comparison to previous technologies [Sreedhar et al. 2008], [Arumi et al. 2008a], [Ingelsson 2009], and therefore affects the voltage on the floating net causing full-open defect. A floating net connected to a gate has a bi-stable input state [Sreedhar et al. 2008], [Arumi et al. 2008a]. In [Sreedhar et al. 2008] an inverter synthesized using 45 nm technology was simulated with a floating input and the change in input voltage was observed. It was found that the voltage on the floating net increased from 0V to 0.17 V (due to gate leakage through the PMOS, as inverter output goes to logic high) and the input voltage reduced from 0.8 V to 0.58 V (due to gate leakage through the NMOS, as inverter output goes to logic low). Furthermore, in [Arumi et al. 2008a] an experiment is conducted using 0.18 μm technology with an open defect. It is shown that an interconnect open initially set to behave as stuck-at 1 (using (8.1) and procedure described above to set a particular logic value on an interconnect) changes to stuck-at 0 in approx. 2 seconds, due to **gate tunnelling leakage** currents. Voltage behavior of the floating net is shown in Fig. 8.13. It is therefore concluded that for nanometer CMOS, gate tunnelling leakage is a dominant player in setting the voltage on the floating net and the final steady state value is independent of the initial state. Furthermore, it is predicted that the time period to reach the steady state will reduce in future technologies and will be in the order of hundreds of μs.

8.3.2 Testing Resistive Open defect

This section summarizes recent research on test techniques for resistive interconnect open defect and the impact of voltage setting on their testability. Resistive open can be modelled as a resistor between two unconnected nodes, since it shows small inductive/capacitive component, which can be neglected for simplicity as used

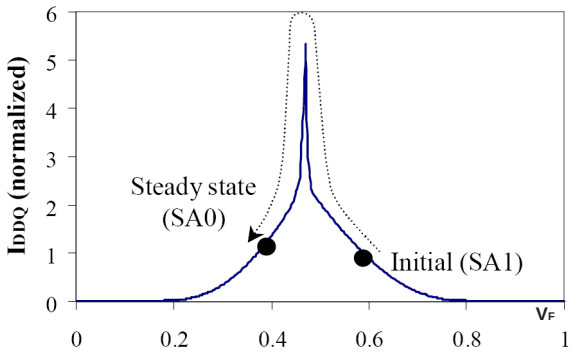

Fig. 8.13: Change in logic value due to gate tunnelling leakage [Arumi et al. 2008a].

in [Kruseman and Heiligers 2006], and [Zain Ali et al. 2006]. Fig. 8.14 shows a typical **resistive open fault model**, where "D" and "S" represent the driver and successor gate respectively.

Fig. 8.14: Circuit Model of Resistive Open Defect.

Resistive open shows timing dependent effects and therefore should be tested using delay tests. Delay fault testing is used to catch defects that create additional than expected delay and thereby cause a malfunction of the IC [Kruseman and Heiligers 2006]. Using delay fault testing, a defect is detectable only when it causes longer delay than that of the longest path in a fault free design. It was shown in [Kruseman et al. 2004] that majority of tested paths show less than one-third delay in comparison to that of the longest path. Therefore a defect in any of these shorter paths can only be detected if it causes higher delay than that of the longest path in the design.

In [Kruseman and Heiligers 2006] the optimal test conditions for testing resistive open is analyzed for non-speed-binned ICs, which are designed to meet timing under worst process and working conditions and typically have a logic depth of 30-70 gates. It is argued that for designs operating at few hundred MHz, one can expect to detect defects with resistance of 100 kΩ or more, while delay caused by smaller resistance defects are of the order of gate delays and does not cause additional delay even if they occur at the longest path. The paper analyses two major sources of open defects, i.e., incompletely filled vias and partial breaks in the poly of the transistor (due to salicidation). Furthermore, it is argued that resistive open shows better detectability on silicon at elevated Vdd settings. This phenomenon is elaborated using

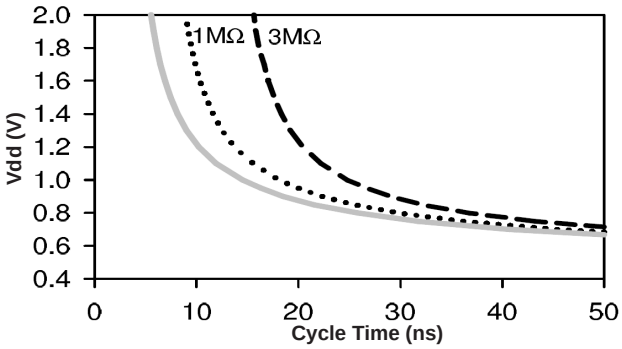

Fig. 8.15: Comparison of path delays due to resistive open defect in the longest path at different supply voltage settings. Solid gray line shows the fault free design, while dotted and dashed lines show path delays using 1 MΩ and 3 MΩ in the longest path [Kruseman and Heiligers 2006].

two examples, shown in Fig. 8.15 and Fig. 8.16 and discussed next. Fig. 8.15 shows the delay caused by two different resistive opens (due to 1 MΩ and 3 MΩ) while considering these defects in the longest path and using different supply voltage settings (1.8 V being nominal supply voltage). The figure also shows the delay of the longest path in fault free design (using solid gray line) and at various voltage settings. As can be seen, the defect induced extra delay added to the expected delay is highest at elevated supply voltage (Vdd = 2.0 V) for both resistive open defects. Also, as expected, higher delay is observed at 3 MΩ than 1 MΩ. Fig. 8.16 shows the effect of resistive open in a shorter path, with half the delay as the longest path in a fault-free design. Defects with same resistance values as Fig. 8.15 are inserted in the shorter path, and the delay is compared with that of the longest path (shown by solid gray line). As can be seen, delay due to 1 MΩ resistance show marginal detectability only at elevated Vdd setting (2.0 V), by causing higher delay than that of the longest path. It becomes undetectable at lower Vdd settings, as it shows lesser delay than that of the longest path. On the other hand, 3 MΩ defect resistance is best detectable at elevated Vdd (2.0 V) and becomes undetectable as Vdd setting is reduced further from 0.9 V. The behavior shown by these two examples (illustrated by Fig. 8.15 and Fig. 8.16) is commonly observed on silicon and is generalized using Fig. 8.17. As can be seen from Fig. 8.17, resistive open in general show better detectability at elevated Vdd setting and becomes undetectable at reduced Vdd. Finally [Kruseman and Heiligers 2006] shows some cases where resistive open defects are better detectable at reduced Vdd setting.

[Zain Ali et al. 2006] has also studied delay behavior for devices operating at multi-Vdd settings. Two types of defects are examined, i.e., transmission gate open and resistive open. Experiments are conducted using 0.35 μm using five (3.3, 3.0, 2.7, 2.5 and 2.0 V) discrete voltage settings on a 4 level carry save adder (shown in Fig. 8.18). Each unit of carry save adder (for e.g., CSA-01) is made up of 5

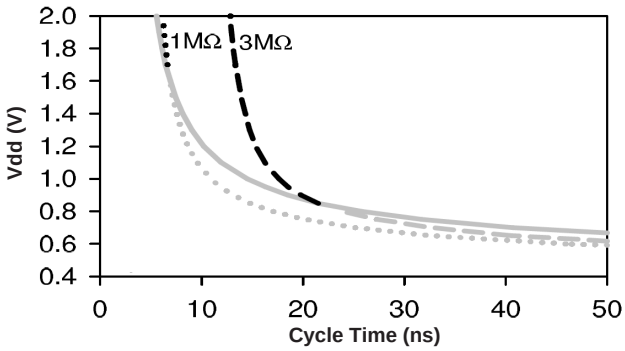

Fig. 8.16: Comparison of path delays due to resistive open defect in a short path at different supply voltage settings. The longest path is shown by a solid gray line (for the fault free design), while dotted and dashed lines show path delays using 1 MΩ and 3 MΩ resistances in a shorter path [Kruseman and Heiligers 2006].

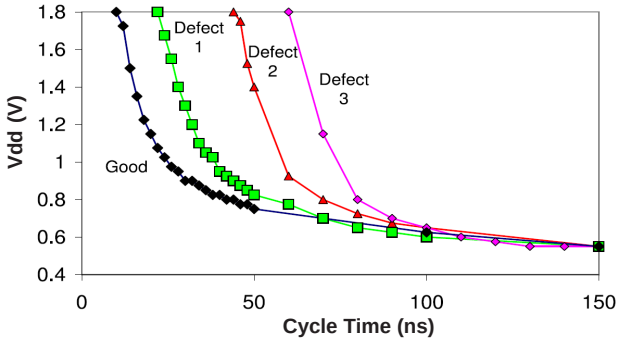

Fig. 8.17: Delay behavior of fault-free design (marked as "Good") in comparison to delay defect behavior due to three different defects [Kruseman and Heiligers 2006].

transmission gates. The impact of transmission gate open is studied first, by inserting two NMOS open defects (one at a time) as shown in Fig. 8.18 (marked as "Fault A" and "Fault B"). The fault site and signal propagation path of inserted defects is shown in Table 8.3. Gate Delay Ratio (GDR) and Path Delay Ratio (PDR)[3] is calculated and results indicate that higher gate/path delay ratio is observed as Vdd setting is reduced and the two faults (transmission gate open) behaves as stuck-at fault (SF) at lower Vdd settings. As expected, increased GDRs for both the faults result in higher PDRs at respective paths as well. Similar observations were reported in [Chang and McCluskey 1996] using 0.6 μm and 0.8 μm technology and similar experimental setup. Study reported in [Chang and McCluskey 1996] has suggested

[3] In [Zain Ali et al. 2006] GDR (PDR) is calculated as a delay ratio between faulty and fault-free signal propagating gate (path) of a design.

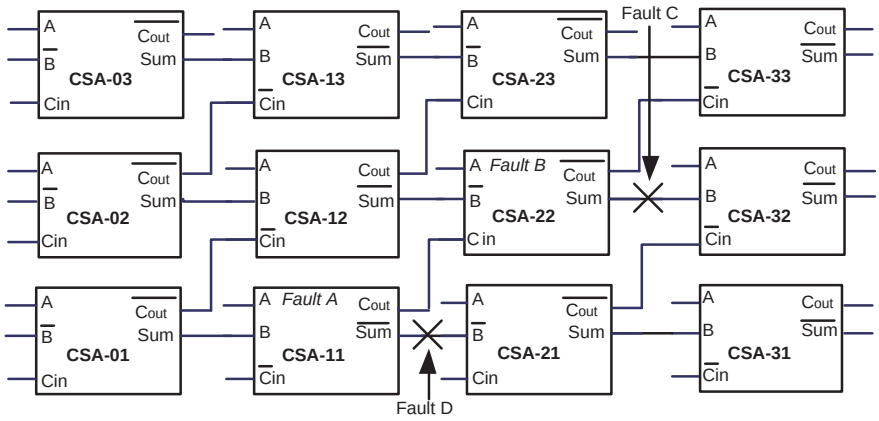

Fig. 8.18: 4-Level Carry-Save Adder, each adder cell is made of five transmission gates [Zain Ali et al. 2006].

using $2V_t$ to $2.5V_t$ (Very Low Voltage (VLV) testing) for detecting defects due to transmission gate open, threshold voltage shift and diminished-drive strength. This explains the SF behavior of transmission gate open at reduced Vdd settings.

Table 8.3: Signal Propagating Path for Faults A and B [Zain Ali et al. 2006].

Fault Site		Signal Propagating Path
A	CSA-11 NMOS Open	CSA-01(A) → CSA-11(B) → CSA-21(B) → CSA-32(Cin) → CSA-32(Cout)
B	CSA-22 NMOS Open	CSA-01(A) → CSA-11(B) → CSA-22(Cin) → CSA-32(B) → CSA-32(Cout)

The impact of interconnect resistive open is also studied in [Zain Ali et al. 2006] by inserting two defects separately in the circuit, marked as “Fault C” and “Fault D” as shown in Fig. 8.18. For this experiment, three different resistance values (25 KΩ, 250 KΩ and 1 MΩ) are used on both locations and results show that Path Delay Ratio (PDR) due to these two faults increases with higher Vdd setting. As expected, PDR is more prominent for 1 MΩ resistance at elevated Vdd setting than the other two resistance values. These findings show that interconnect resistive opens are better detectable at elevated Vdd setting by delay test techniques. On the other hand, transmission gate opens are better detectable at lower Vdd settings. The application of delay test at single Vdd setting reduces test cost by avoiding repetitive tests at other Vdd settings.

8.4 DFT for Low Power Design

Sections two and three outlined test techniques for resistive bridge and resistive open for multiple-voltage designs. In this section, we summarize recent low cost scan techniques for reducing power dissipation during test mode [Nicolici and Al-Hashimi 2003]. These techniques are developed for devices employing multiple-voltage settings.

8.4.1 Multi-Voltage Aware Scan

Designs that employ multiple voltage settings are divided into various voltage domains during physical placement of the design. Each voltage domain feeds various logic blocks and **level shifters** are used to communicate logic values across logic blocks operating under different voltage settings [Shi and Kapur 2004]. The insertion of scan chains across logic block poses a challenge for scan chain ordering in multiple voltage designs due to two main reasons. Firstly, it is desirable to reduce the number of level shifters required to transmit voltage levels from one scan chain to another, placed across different voltage domains. Secondly, power consumption during test can be reduced by fewer voltage domain crossing by the scan cells.

These challenges are met by multi-voltage aware scan cell ordering [Colle et al. 2005]. The proposed methodology arranges scan cells based on respective voltage domains. This is achieved by scan cells ordering in such a way that scan cells operating under the same voltage levels are connected together. This in turn minimizes the number of level shifters that are otherwise required if scan cells are ordered without consideration of multi-voltage designs. Furthermore, it reduces power dissipation by minimizing signal transmission in fewer voltage domain crossing. Experiments are conducted using industrial design with 4 voltage domains and it is shown that multi-voltage aware scan chain ordering shows 93% reduction in the number of level shifters, in comparison to scan chain ordering technique, which connects physically closer scan cells without considering its operating voltage. The proposed scheme has been implemented in Synopsys EDA tools and the DFT flow is shown in Fig. 8.19. As can be seen, DFT Compiler recognizes the voltage/power domains and clusters the scan chains within the respective domains. The number of level shifters in the design are minimized by disabling voltage/power domain mixing, which is managed by “set scan configuration”.

Recently a power-aware scan chain method is presented in [Chickermane et al. 2008] for multi-Vdd designs. The method is implemented using daisy-chaining scan approach to efficiently utilize expensive tester resources (bandwidth) and reduce test cost. The method avoids signal integrity issues during test by employing bypass multiplexers, which allows bypassing signals from power domains that are switched off during test. Daisy-chain implementation along with bypass multiplexers (1, 2, 3 and 4) and four different power domains (A, B, C and D) is shown in Fig. 8.20. As can be seen, bypass multiplexers allow testing of specific power domains in multi-

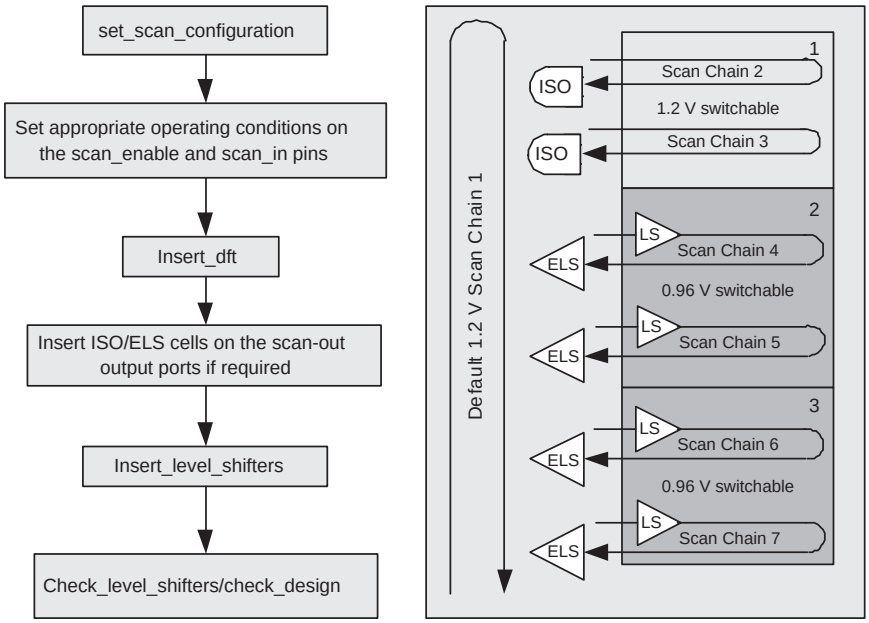

Fig. 8.19: DFT Synthesis flow for Multi-Vdd design using Synopsys Design Compiler [Baby and Sarathi 2008].

Vdd environment. As an example, in a particular power mode, where power domains C and D are ON, while A and B are OFF, muxes 1 and 2 goes in bypass mode, while 3 and 4 are in pass-thru mode. This forms a scan chain between SI, 3, 4 and SO. The bypass multiplexers are placed on always-on power domain. This approach is implemented in Cadence $Encounter^{TM}$ test tools.

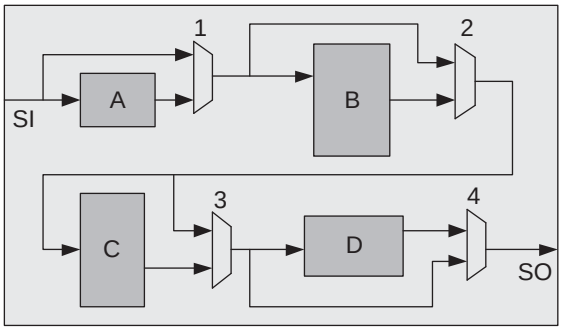

Fig. 8.20: Power-Aware Daisy-chaining scan path [Chickermane et al. 2008].

8.4.2 Power-Managed Scan Using Adaptive Voltage Scaling

Reducing power dissipation during test has been an active area of research for nearly a decade and numerous techniques have been reported [Girard 2002], [Bhunia et al. 2005]. Recently an interesting technique that reduces both dynamic and leakage power during test through the use of adaptive voltage scaling PMScan (Power Managed Scan) has been reported [Devanathan et al. 2007]. The presented methodology is motivated by three factors. Firstly, it is known that dynamic power is proportional to V^2 [Weste and Eshraghian 1994] and gate leakage power is proportional to V^4 [Krishnarnurthy et al. 2002], where V is the operating voltage of the device. Therefore, reduction in supply voltage can significantly reduce total power (dynamic plus leakage) during test. Secondly, infrastructure for adaptive voltage scaling is widely deployed in modern microprocessors to reduce power consumption during functional mode. Therefore, it is suggested in [Devanathan et al. 2007] to reuse voltage scaling infrastructure to reduce implementation (due to physical design and area) overheads. Thirdly, scan shift frequency is usually much slower than the operational frequency of the device, therefore scan shift operation is ideal for voltage scaling during test[4]. Therefore PMScan proposes voltage scaling during test to provide a trade-off between test application time and test power. This is achieved by modifying voltage regulation circuitry (used for adaptive voltage scaling) such that scan shift operation meets acceptable timing, while supply voltage during scan shift is reduced. The voltage regulation circuitry changes the supply voltage to nominal during scan capture mode to ensure at-speed testing.

The conventional voltage scaling circuitry and the one proposed in [Devanathan et al. 2007] are shown in Fig. 8.21. Fig. 8.21(a) shows the conventional adaptive supply voltage circuitry showing the voltage regulation component in the dashed box. It uses feedback control and adjusts the supply voltage 'V' using a dc-dc converter such that the delay of the circuit fits in one clock cycle of the desired clock frequency f_{ref}, which is usually generated using on-chip PLL. The reference circuit is made of a ring oscillator and determines the maximum delay of the design over process, voltage and temperature variations. It determines the maximum frequency 'f' corresponding to the voltage 'V' provided to it. In [Devanathan et al. 2007] the conventional voltage regulation design is modified for voltage scaling during scan shift operation, as shown in Fig. 8.21(b). It is designed such that when the signal LV_scan = 1, the supply voltage 'V' is lowered by 'p'. On the other hand when LV_scan = 0, the output 'U' is applied to the multiplexer as in conventional design. Refer to [Devanathan et al. 2007] for more details on design of such regulator.

Experiments are conducted using 90 nm library with nominal 1.1 V supply voltage using Synopsys *PrimePower*^{TM} for power analysis. The first experiment is conducted using seven different ISCAS 89 benchmarks using reduced Vdd (0.77 V) and at 25 MHz scan shift frequency. Average dynamic, peak dynamic and leakage

[4] Voltage scaling is widely used to reduce power consumption, while ensuring that timing requirements are met. It is therefore more effective for tasks that are less computationally intensive, i.e., tasks that can be completed at a slower speed.

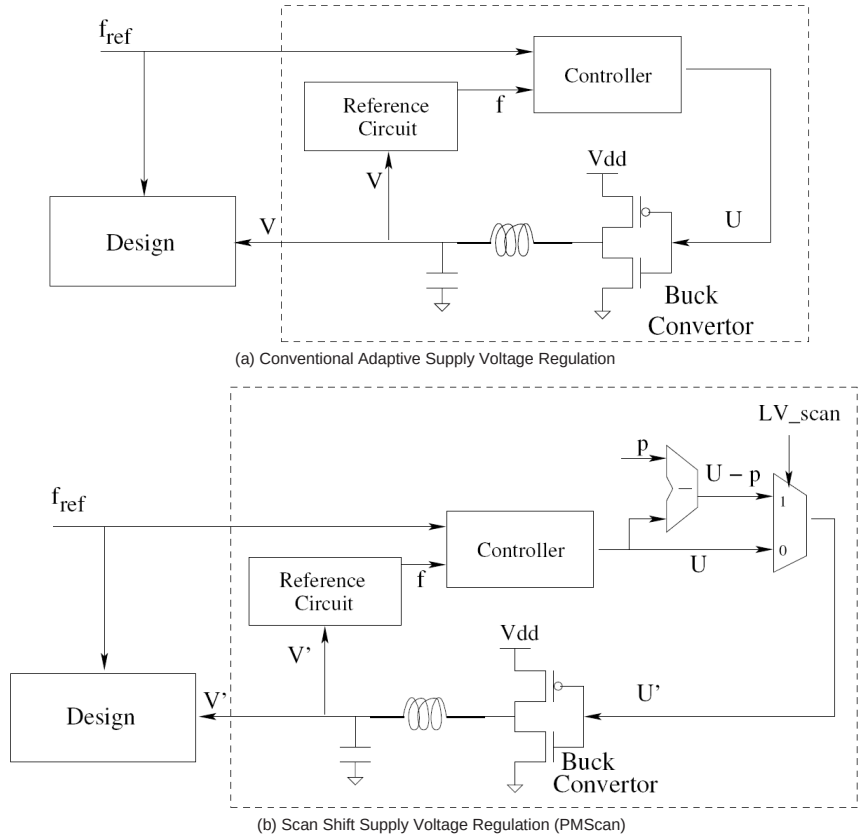

Fig. 8.21: Block diagram of Adaptive Supply Voltage Regulation in: (a) Conventional design, (b) PMScan [Devanathan et al. 2007].

power is compared between proposed PMScan technique with that of conventional scan (unaware of voltage scaling). It is shown that on average PMScan reduces average dynamic power by about 44%, peak dynamic by 42%, leakage power by 91% contributing to overall total power by 64% in comparison to conventional scan. Moreover, it is shown that these results can be further improved by 5%, by using NOR-Gating scheme [Girard 2002][5] along with PMScan. The second experiment analyses test time and test power trade-off. It is conducted using an industrial design (with 9 million gates and 7 unwrapped cores), at three different voltage (1.1 V, 1.0 V and 0.77 V) and scan shift frequency (25 MHz, 75 MHz, and 125 MHz) settings. It is shown that for test application at 0.77 V and 125 MHz scan shift frequency,

[5] NOR gate is used to halt unnecessary toggling of combinational logic (fed by scan flip-flop) during scan shift operation.

test time reduces by 80%, while total power increases by 16%, in comparison to test application at 0.77 V with 25 MHz scan shift frequency.

Another effective technique for reducing leakage power is by employing **state retention logic** [Keating et al. 2007]. Recently a method to test state retention logic is proposed in [Chakravadhanula et al. 2008]. State retention logic is tested by scanning in test patterns, followed by powering down the logic block containing state retention logic and then powering up again. This is followed by scanning out the test patterns, and is matched against the scanned in data for coherency.

8.5 Open Research Problems

Low power design techniques present potential challenges to test and reliability of digital designs. At present there are continuing research efforts world-wide focusing on addressing these challenges. In the following three emerging research problems are highlighted that need to be addressed, to generate high quality and cost effective test solutions for reliable low power designs.

8.5.1 Impact of Voltage and Process Variation on Test Quality

Previous sections have examined the impact of power supply variation on the behavior of manufacturing defects. It appears that test quality is also compromised due to another type of variation, i.e., due to fabrication process. Whilst the impact of process variation on timing and power performance has been extensively investigated in the literature [Bhunia et al. 2007], its effect on test quality is an emerging area of research. In this section we summarize two recent studies that take process variation into account using static and delay test techniques and motivate the need for joint **voltage and process variation** test.

In [Ingelsson et al. 2008] and [Ingelsson 2009], the impact of process variation on static test quality has been investigated for resistive bridge. It is shown that process variation has a negative impact on test quality of such defects leading to test escapes. A Robustness matrix is developed to quantize the impact of process variation on test quality and a test generation method is developed to mitigate the impact of process variation and reduce test escapes. Experiments are conducted using ISCAS 85' and 89' benchmarks and synthesized using 45 nm CMOS technology. Results show that test generation method covers up to 18% more process variation induced logic faults than tests generated without consideration of process variation. In [Lu et al. 2005] the influence of process variation on the longest path of the design has been investigated, while considering structural elements of the design (logic elements and interconnects). The method aims to reduce test cost without compromising on test quality, i.e., fault coverage. This is achieved by identifying minimum number of longest path candidates in polynomial time. Experiments conducted on ISCAS 85'

and 89' circuits show that the number of testable paths are up to 6% of those found by [Tani et al. 1998]. In addition it is 300-3000 times faster than the method proposed in [Tani et al. 1998].

High quality test for next generation Multi-Vdd devices require improved static and delay test techniques capable of mitigating the impact of power supply and fabrication process variation. Such test techniques will need to be developed that will require realistic fault models, for both resistive bridge and resistive open, that mimic actual behavior at the physical level in the presence of voltage and process variation. Such fault models will be used for voltage and process variation aware test generation leading to higher test quality and therefore improve in-field product reliability of future Multi-Vdd devices.

8.5.2 Diagnosis for Multi-Voltage Designs

Diagnosis is a systematic way to uniquely identify the defect causing malfunction in the circuit. It is critical to silicon debugging, yield analysis and for improving subsequent manufacturing cycle. Recently diagnosis procedure for resistive bridge is investigated in [Khursheed et al. 2009b] for ICs employing multiple-voltage setting. The diagnosis procedure [Khursheed et al. 2009b] is based on cause-effect diagnosis scheme [Abramovici et al. 1998] using a pass/fail dictionary [Pomeranz and Reddy 1992] to minimize memory storage. The proposed diagnosis algorithm combines information of resistance interval detection at all voltage settings and achieves overall higher diagnosis accuracy. Experiments are conducted using parametric fault model [Renovell et al. 1996], and ISCAS 85' and 89' benchmarks are synthesized on 120 nm technology. Experimental results show that the lowest Vdd setting achieves highest diagnosis accuracy for single Vdd diagnosis, which is improved up to 38% by using multi-Vdd diagnosis. Furthermore, it establishes that multi-Vdd diagnosis is more effective for resistive bridge than for hard-shorts (bridge with 0 Ω resistance).

It is expected that future diagnosis strategies will need to employ process variation aware fault models to accurately diagnose resistive bridge and resistive open defects. Thereby accounting for test escapes due to process variation in nanometer CMOS and provide accurate diagnosis to DSM designs.

8.5.3 Voltage Scaling for Nanoscale SRAM

The above two open problems are related to test for low-power devices. Recent research indicates that low-power design also affects reliability of the device. One such work that determines optimal voltage setting to operate SRAMs in the presence of soft errors and gate oxide degradation is presented in [Chandra and Aitken 2009]. Nanoscale SRAMs are vulnerable to soft errors and suffer from progressive gate ox-

ide degradation. Soft errors are faults induced by particle hit (alpha particle or neutrons), which can flip the stored data bit. These events are called Single Event Upsets (SEU) and requires data content to be re-written. SRAMs are especially vulnerable to SEU due to small node capacitance and small bit cell size[6]. On the other hand, gate oxide thickness is continuously decreasing with technology scaling in CMOS devices, which has resulted in increased gate tunneling currents. Increased gate tunneling currents result in progressive degradation of gate oxide, which is one of the most important reliability concern in current and future technologies. In [Chandra and Aitken 2009], the optimal voltage setting to operate nanoscale SRAM in the presence of soft errors is investigated. This work has shown following three findings: For a given technology node (65 nm or 45 nm), higher voltage level results in higher immunity of SRAM cells against soft errors in the absence of gate oxide degradation. On the other hand, gate tunneling currents increase with the increase in supply voltage, which in turn contributes to gate oxide degradation. Therefore an optimal voltage is formulated by an equation, for operating nanoscale SRAMs in the presence of gate oxide degradation and soft errors. The optimal voltage reduces with increasing level of gate oxide degradation for nanoscale SRAMs.

It is expected that analytical models will be developed to achieve highest immunity against soft-errors for a given voltage setting value and gate-oxide degradation level, thereby improving reliability of nanoscale SRAMs in future technologies.

8.6 Summary and Conclusions

This chapter has presented an overview of recently reported research in testing strategies for multi-voltage designs. Such strategies aim to reduce test cost and improve defect coverage of Vdd-dependent defects. The cost reduction has been obtained by using the least number (i.e., one) of voltage test setting for Vdd-dependent defects (resistive bridge and resistive open) by avoiding repetitive tests at several Vdd settings. For resistive bridge, the cost reduction is achieved by test point insertion and more recently by gate sizing, which achieves 100% defect coverage at a single (lowest) test voltage. For resistive or full open interconnect defect, elevated Vdd setting achieves better detectability using delay test and therefore repetitive tests at other voltage settings can be avoided.

Low cost scan for multi-voltage design is possible through various techniques. Some techniques focus on reducing implementation cost of scan chains in multi-voltage environment through clustering scan chains according to their respective voltage domain thereby reducing the number of level shifters and also by employing power-aware scan that efficiently utilize expensive tester resources (bandwidth) and reduce test cost. Other technique achieves low power test for multi-voltage devices by reusing the existing functional infrastructure for voltage scaling to reduce power consumption leading to reduced cost. The chapter also outlines a number of

[6] Refer to [Baumann 2005] for further reading on the effect of technology scaling and soft errors on memory and logic components of the circuit.

worthy research problems that need to be addressed to develop high quality and cost effective test solutions for reliable low power devices.

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