Lateral conduction of Si nanorystals by thin film transistor structures

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1. Introduction

Strongly correlated electron systems are attractive candidates for future nano-electronic devices, such as Mott transition field effect transistors [1-3]. Nanocrystals (NCs) acting as the artificial lattice systems would be one of the candidate materials to attain the Mott metal-insulator transition [4-5]. The Si nanocrystals (SiNCs) with a few nanometer diameters are of the great interest in the development of such kinds of devices for integrated circuit applications. However, the basic transport properties of the three dimensional random network formed by the NCs are not completely understood, yet.

In this work, carrier transport characteristics in the size controlled SiNCs have been investigated through thin film transistor structures. Under the modulation of gate voltage (V_g), transport mechanism has been discussed based on the experimental results that conductance show the temperature and voltage dependence.

2. Fabrication Process

Figure 1 (a) shows the structure of the SiNCs thin film transistor. Fabrication processes are as follows: SOI wafers with original SOI thickness of 100 nm and the buried-oxide (BOX) layer thickness of 200 nm were used to start fabrication processes. Firstly, the SOI layer was thermally oxidized and phosphorus ion implanted (10^{19} cm^{-3}). After ion-implantation, drive-in process at a temperature of 1100 ^{0}C was conducted to activate the dopants. An Oxide protection layer for implantation damage was removed after drive-in process. Interdigital electrodes (Twenty-pairs of fingers form 39 channels. Each channel width W_i is 20 μm, length L 150 nm.) were formed by using electron beam lithography, as shown in Fig.1 (b). The electron cyclotron resonance reactive ion etching was conducted to transfer the lithographically defined pattern to the SOI layer with a thickness of 50nm. After etching, size controlled Si nanocrystals with thickness of 250nm, were deposited on substrates at room temperature by Very High Frequency (VHF) plasma deposition of SiH_4 in a plasma cell [6]. The size of SiNCs measured in this work is 8~10 nm in diameter as shown in Fig.1 (c) and SiNC density is about 10^{18} cm^{-3}. Each SiNC is covered by an SiO_2 shell, 1~1.5 nm in thickness, formed by natural oxidation. The SiO_2, with 200 nm in thickness, was deposited on SiNC layer as a protection layer. Aluminum (Al) was chosen to make metal/semiconductor contacts through evaporation methods.

3. Results and Discussion

Measurement results of the drain current-gate voltage (I_{ds}-V_{ds}) for different values of gate voltage (V_g) at room temperature exhibit the non-linear characteristics. Through measuring the structure of *Al/n$^+$-Si/Al*, as shown in the inset of Fig.2 (a), SiNCs covered by SiO_2 shell are supposed to be responsible for the non-linear *I-V* characteristics as shown in Fig.2 (a). Compared with the structures of *Al/SiNC/Al*, devices fabricated by using SOI layers as electrodes show the lower contact resistance, as shown in Fig.2 (b). The SiNCs used in these two devices for the comparison are deposited under the same conditions. In addition, transport mechanism under the modulation of V_g has been investigated through the *I-V* characteristics. The conductance exhibits exponential dependence on $V^{1/2}_{ds}$ with different slopes in the region (A) and (B), shown in Fig.3 (a). By extrapolating conductance to V=0, barrier heights of traps caused the field enhanced detrapping in each V_{ds} region have been gained, shown in Fig.3 (b). At the beginning, most carriers are trapped at E_{TA} (147 meV) due to the carriers are prefer to be trapped at the relatively deeper traps. With V_{ds} increasing, more carriers will be injected into the channels, which are formed by Si core and SiO_2 shell multiple tunnel junctions. Supposing the total number of the trap sites at E_{TB} (103 meV) is larger than that of $E_{TA,}$ more traps will be filled at E_{TB} with further increasing V_{ds} because of the empty trap sites number decreasing at $E_{TA.}$ Thus, with further increasing V_{ds}, the relatively shallow traps E_{TB} begin to dominate the detrapping process. The trapped carriers will form space charge areas influence the field distribution. It is responsible for the phenomenon that increasing V_{ds} makes the slopes of $V^{1/2}_{ds}$ dependence of conductance change. In addition, the hole mobility is evaluated by the expression of $\mu=g_m(L/W)/(C_G V_{DS})$, through measuring I_{ds}-V_g. Here, C_G is capacitance per unit area of gate oxide and g_m transconductance. Mobility shows Poole-Frenkel type transport for temperature and voltage, as shown in Fig.4 (a) and (b). Carriers transport occurs mainly by hopping between adjacent localized states which are induced by the disorder.

4. Conclusion

We have investigated the lateral conduction of SiNC thin films through thin film transistor

structures as functions of temperature and voltage. Device performance has been improved by using highly doped SOI layer as electrodes. Under the modulation of V_g, two kinds of shallow traps dominating the detrapping process have been found. In addition, values of the mobility exhibiting Poole-Frenkel type dependence on temperature and voltage has also been observed.

References

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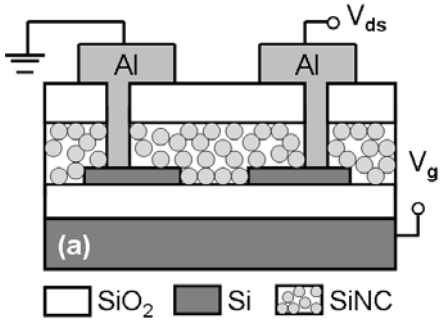

Fig.1 (a), schematic of device structure measured in this work.

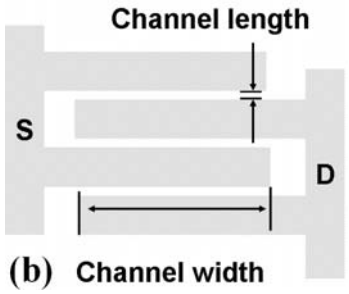

Fig.1 (b), schematic of the interdigital electrodes

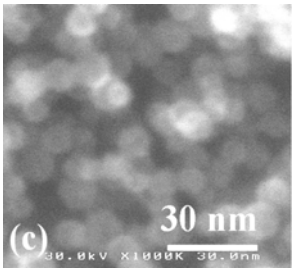

Fig.1 (c), SEM image of the size controlled SiNCs

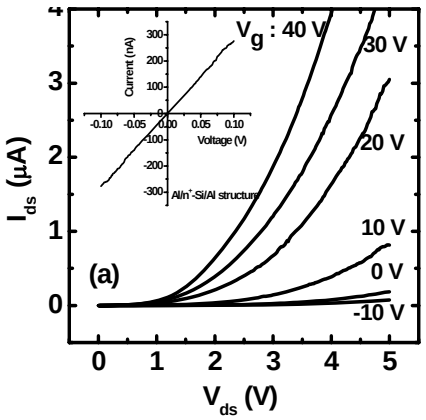

Fig.2 (a), I_{ds}-V_{ds} modulated by various V_g from -10 V to 40 V, measured at room temperature and the inset is *I-V* characteristics of *Al/n*$^+$*-Si/Al* structure

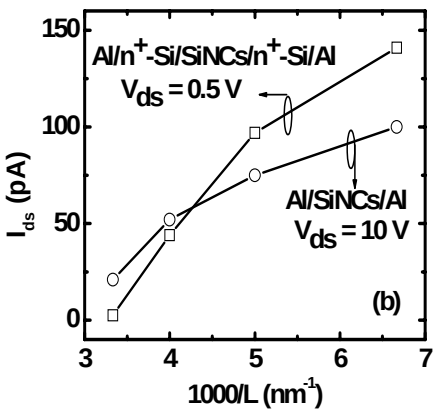

Fig.2 (b), channel length dependence of I_{ds} for devices with and without SOI Ohmic contact layer

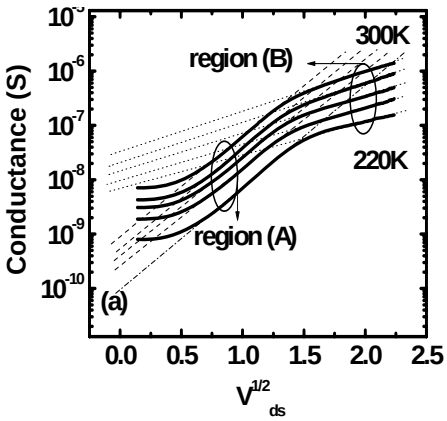

Fig.3 (a), $V^{1/2}$ dependence of conductance with various temperatures at V_g = 40 V

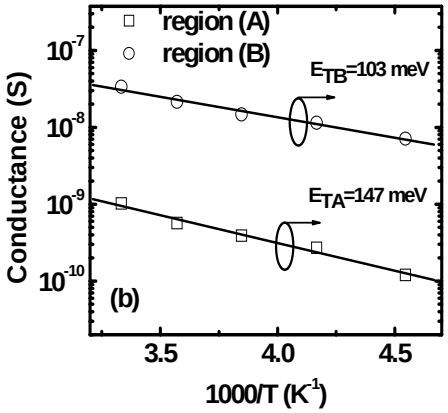

Fig.3 (b), temperature dependence of the conductance obtained from Fig.3 (a) by extrapolating conductance to V_{ds} = 0 for region (A) and (B)

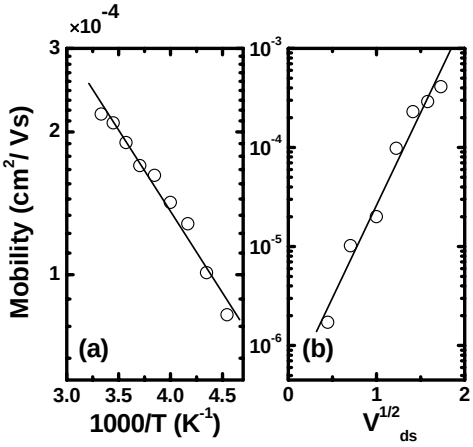

Fig.4 (a) temperature dependence of mobility obtained at V_{ds} = 2 V and (b) $V^{1/2}{}_{ds}$ dependence of mobility at room temperature