Engineering of Heterostructured Tunnel Barrier for Non-Volatile Memory Applications: Potential of Pr-based Heterostructured Barrier as a Tunneling Oxide

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1. Introduction

The trade-off between longer retention time (lower leakage at lower voltage) and faster writing/erasing speed (higher current at higher voltage) has been a critical issue in designing floating-gate-type NVM (nonvolatile memory). To obtain lower leakage and larger writing/erasing current, engineered tunnel barrier structures in place of a single SiO_2 barrier[1][2] were proposed. The SiO_2/high-κ/SiO_2 heterostructure enables both lower leakage and larger writing/erasing current, thanking to the recessed conduction band profile[3]-[6] (Fig. 1). Fig. 2 shows the simulated *J-V* characteristics both for a heterostructured barrier and a single SiO_2 barrier, clearly demonstrating the advantage of the heterostructured barrier in terms of the leakage and the writing/erasing current. Furthermore, thanking to the high dielectric constant of high-κ film, total EOT can be substantially reduced, leading to a better scalability of flash memories.

However, although a variety of high-κ materials, such as HfO_2, ZrO_2, Al_2O_3, La_2O_3, Pr_2O_3, is proposed for CMOS applications, no guiding principle for the selection of high-κ materials for NVM heterostructured barriers is available.

In this paper, the potential of high-κ materials as the heterostructured barriers is firstly studied using the quantum *J-V* simulator in terms of dielectric constant and thickness. After that, the Pr-oxide based heterostructures are fabricated and characterized experimentally.

2. Optimization of heterostructures by simulation

Tunneling current densities J_t through heterostructured barriers were calculated solving the Schrödinger and Poisson's equations in a self-consistent manner. Material parameters such as the dielectric constant κ, the conduction band offset to Si ΔE_c, and thickness $T_{high\text{-}\kappa}$ are varied.

Figure 3 shows the J_t-V characteristics simulated for various κ values. A larger κ results in larger tunneling current in the high *V* region, meaning that the larger κ is better for the writing/erasing operations.

J_t-V characteristics for various ΔE_c are shown in Fig. 4. A smaller ΔE_c lowers the turn-on voltage and steepens the slope simultaneously; smaller ΔE_c is good to lower writing/erasing voltage. However, an excessive reduction in ΔE_c results in a large disturbance during the readout operations because it turns on the current at a low voltage even if a thick high-κ film is employed. It is therefore vital to use ΔE_c about 1.0 eV.

Figure 5 shows J_t-V characteristics for various $T_{high\text{-}\kappa}$. Thicker $T_{high\text{-}\kappa}$ reduces the J_t only at the lower voltage region; thicker $T_{high\text{-}\kappa}$ is better in terms of retention, whereas it is worse in terms of EOT. Therefore as thin as possible $T_{high\text{-}\kappa}$ which can reduce leakage enough at the lower voltage region is required to attain thinner EOT.

These results manifest the heterostructures should simultaneously meet both a large κ and a smaller ΔE_c which is also required to be greater than 1.0 eV. Pr_2O_3 has the κ value of about 30 and the ΔE_c of about 1.0 eV[7]. Therefore we selected Pr_2O_3 as one of the most suitable materials for the engineered heterostructured tunnel barrier.

3. Fabrication and characterization of heterostructures

The MOCVD method with $Pr(EtCp)_3$ as a source material and O_2 as an oxidant was employed to grow Pr-oxide films. On the 1-nm or 2-nm SiO_2 grown on p-type 0.1-Ωcm Si substrate, Pr-oxides were deposited at the temperature of 350 °C and the pressure of 2.0 Torr The other SiO_2 film is deposited on top of the Pr-oxide films without exposure to the atmosphere by using the LPCVD method with $SiH(NEtMe)_3$ as a source material and O_3 as an oxidant at the temperature of 300 °C, and the pressure of 2.0 Torr.

The XPS spectra for SiO_2(1 nm), Pr-oxide(4 nm)/SiO_2 (1 nm), and SiO_2(1 nm)/Pr-oxide (4 nm)/SiO_2(1 nm) measured by SSX100 are shown in Figs. 6 and 7. After Pr-oxide deposition, there was virtually less increase of interfacial layer at 103.4 eV in Fig. 6, and less noticeable Pr-silicate peak in Fig. 7. These results indicate less detectable interface layer increment. For more detailed discussion on the interface layer, the XPS with a higher resolution such as ESCA300 is required. After SiO_2 deposition, a strong peak of not the Pr-Silicate but the SiO_2 appears at 103.4 eV. Therefore we conclude from the XPS results that the SiO_2/Pr-Oxide/SiO_2 heterostructure is successfully fabricated with very thin interfacial layers.

The tunneling current density properties of the SiO_2(2 nm)/Pr-oxide(4 or 8 nm)/SiO_2(2 nm) heterostructure are shown in Fig. 8. Between the characteristics of two heterostructures, there was no noticeable difference in the current density in the high-voltage region, but that in the low-voltage region was found remarkably suppressed for a thicker Pr-oxide. This is consistent result with Figure 5.

Compared to SiO_2, the on-off ratios observed for the heterostructures are much larger. This is also a unique feature of the heterostructured tunnel barrier. From these results, we conclude that the SiO_2/Pr-oxide/SiO_2 stacks were successfully engineered with the electrical properties suitable for the nonvolatile memory applications.

4. Conclusion

It was clarified by using the simulation that larger dielectric constants and ΔE_c about 1.0 eV are demanded for the heterostructured tunnel barrier, and Pr_2O_3 is one of the best materials. The SiO_2/Pr-oxide/SiO_2 heterostructures were successfully fabricated, and their excellent electric characteristics as a heterostructured tunnel barrier were demonstrated.

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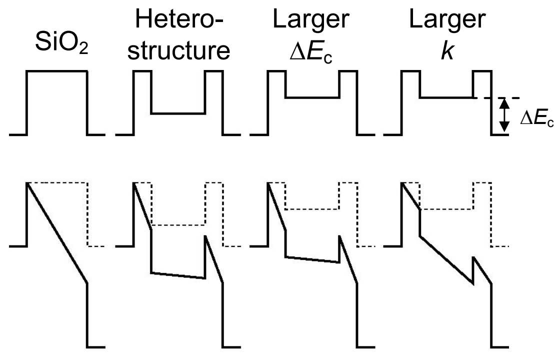

Figure 1 : Band diagram of Heterostructured tunnel barrier

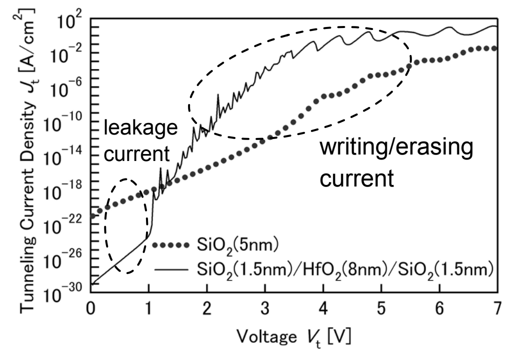

Figure 2 : comparing of tunneling current density of Heterostructured tunnel barrier and SiO_2

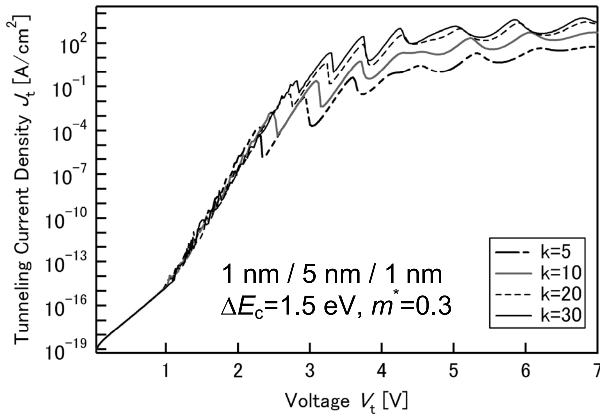

Figure 3 : tunneling current dependant on dielectric constants

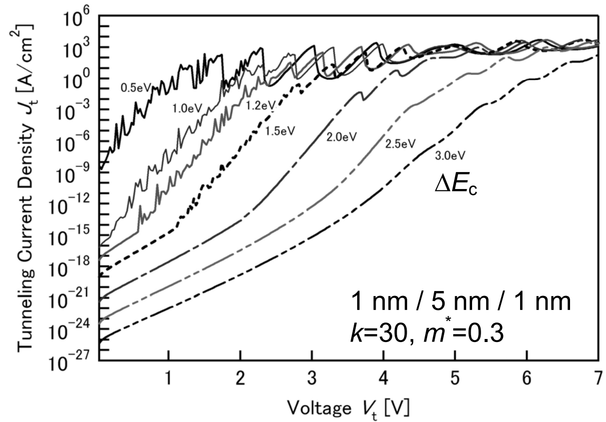

Figure 4 : tunneling current dependant on band offsets

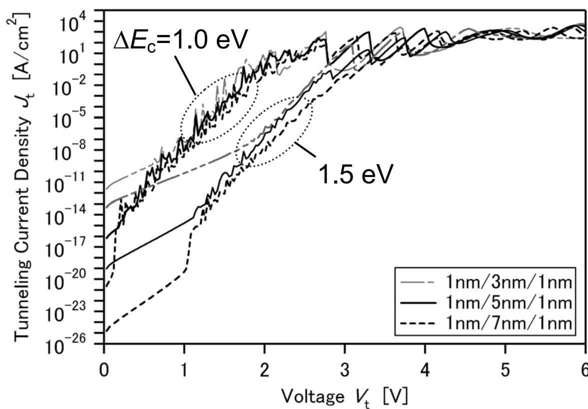

Figure 5 : tunneling current dependant on high-*k*

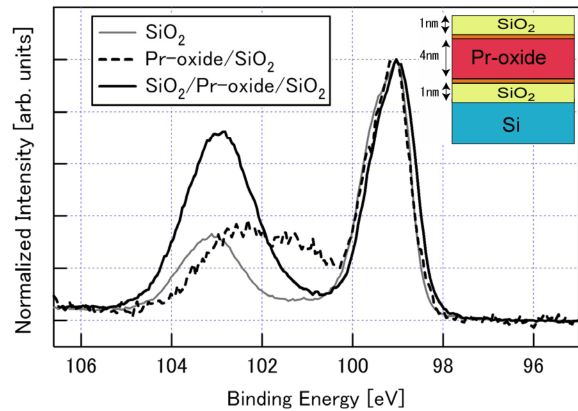

Figure 6 : Si2p XPS Spectra of heterostructure

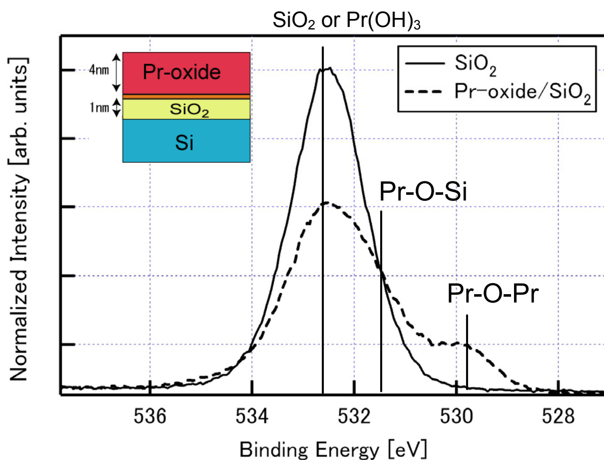

Figure 7 : O1s XPS Spectra of Pr-oxide/SiO_2 stack

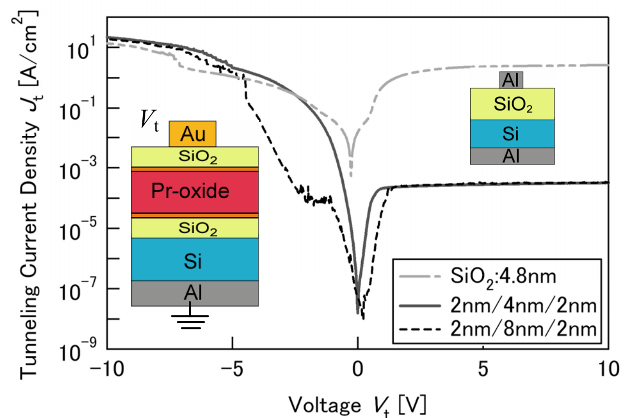

Figure 8 : electrical characteristics of fabricated heterostructures