A Self-Aligned Silicidation Technology for Surround-Gate Vertical MOSFETS

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Abstract-**We report for the first time a silicidation technology for surround gate vertical MOSFETs. The technology uses a double spacer comprising a polysilicon spacer for the surround gate and a nitride spacer for the silicidation. Silicided 120 nm n-channel devices show a 30% improvement in drive current in comparison to non silicided devices, but this is accompanied by a small degradation in sub-threshold slope and DIBL. This problem is solved using a frame gate architecture in which the pillar sidewalls are protected from the silicidation process. Silicided frame gate transistors show a similar increase in drive current without any significant degradation of sub-threshold slope or DIBL. For a 120 nm channel length, silicided frame gate vertical nMOSFETs show a 30% improvement in the drive current with an excellent sub-threshold slope of 78mV/decade and a DIBL of 30 mV/V. For an 80 nm channel length, a 43% improvement in the drive current is obtained.**

1. INTRODUCTION

Thin pillar, fully depleted vertical MOS transistors are being researched as candidates for end-of-roadmap CMOS technology because they offer advantages such as improved short channel effects and improved drive current [1-3]. Surround-gate thick pillar vertical MOSFETs are also of interest because they offer a high drive current per unit silicon area [4] and can be easily integrated in a mature CMOS technology to provide low cost RF transistors. The challenges of vertical MOSFETs for this application are high overlap capacitance, susceptibility to dry etch damage and the lack of an appropriate silicidation technology. We have previously reported a CMOS compatible Fillet Local Oxidation (FILOX) process for reducing the overlap capacitance [5] and also reported a novel FILOX compatible frame gate architecture (Fig. 1), which eliminates device degradation due to dry etch damage [6]. However, to date there have been no reports in the literature on silicidation technologies for surround gate vertical MOSFETs..

In this article we report a silicidation process for vertical MOSFETs. The process is applied both to conventional surround-gate devices and frame gate devices. An improved drive current is obtained for both device types, but a small degradation in subthreshold slope and DIBL is observed for the conventional surround gate devices. For a 120 nm channel length, a 30% improvement in drive current is obtained and for an 80 nm channel length, a 43% improvement is obtained.

2. DEVICE FABRICATION

Boron-doped (0.75-1.25 Ω.cm) (100) wafers were taken as the starting material and a p-type body was formed by boron implantation and a high temperature drive-in. The FILOX (Fillet Local Oxidation) process [5] used a 70 nm wide nitride fillet on the pillar sidewalls and a 65 nm oxide layerwas thermally grown at 1100°C. The source/drain electrodes were implanted (arsenic, 3×10^{15} cm^{-2}, 110 keV, 7 degree tilt, 4 times) and the nitride fillets and pad oxide were subsequently removed. A 2.5nm gate oxide was then grown at 700°C and a 230 nm in-situ doped (P, $1\times10^{20}/cm^3$) polysilicon gate was deposited and patterned by dry etch. An RTA at 1100°C for 10 or 30 sec was then performed for dopant activation. In the silicided wafers, the underlying FILOX oxide was also dry etched just after the gate-etch. A 20 nm oxide layer and a 80 nm nitride layer were deposited and subsequently the nitride layer was dry etched to leave nitride spacers around the pillar sidewall. The 20 nm oxide layer was wet etched just prior to Ni deposition and subsequently a 20 nm Ni layer was deposited. A silicidation anneal of 30 sec at 450°C was performed and the unreacted Ni was removed using a piranha solution. In this way, the source/drain regions and the horizontal portions of the polysilicon gate were silicided.

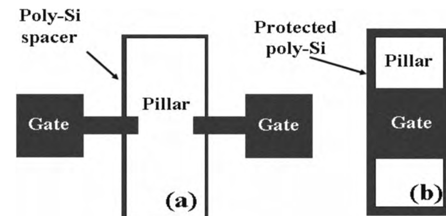

Fig.1: Schematic plan views of fabricated vertical MOSFETs; a) surround gate device b) frame-gate device.

Two different device designs were fabricated, as shown in Fig. 1. In the surround gate device, a polysilicon surround gate is created using deposition and anisotropic etch, whereas in the frame gate (FG) device [6], a polysilicon frame is lithographically defined around the perimeter of the pillar. The frame gate architecture has the potential disadvantage of a higher overlap capacitance, but this is compensated by the use of the FILOX process which reduces overlap capacitances.

3. PROCESS CHARACTERISATION

Fig. 2 shows a SEM micrograph of a pillar just after FILOX oxidation. The figure clearly shows the 70 nm nitride spacer and the presence of the FILOX oxide at the top and bottom of the pillar. The FILOX oxide is 65 nm, in agreement with expectations. Oxide encroachment of 75 nm can be seen at the pillar top but there is no such encroachment at the pillar bottom.

Fig. 3 shows SEM micrographs of the devices just after the nitride spacer process prior to silicidation. For the surround gate device (Fig. 3(a)), the gate poly silicon spacer thickness at the pillar bottom is 200 nm and there is a 75 nm over-etch at the pillar top. The nitride spacer on the polysilicon fillet can be easily seen. It has thicknesses of 25 nm and 70 nm at the pillar top and bottom respectively. The remaining FILOX oxide thickness at the pillar bottom is 35 nm. For the frame gate device (Fig. 3(b)), the polysilicon thickness on horizontal surfaces is 230 nm and on the pillar sidewall is 200 nm. The nitride spacers on the vertical sidewalls of the polysilicon gate can be seen and the thickness of the FILOX

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oxide beneath the poly frame overlap region on the pillar top and bottom is 40 nm.

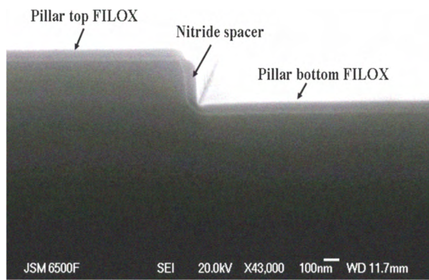

Fig. 2: SEM cross-section of the FILOX process directly after the FILOX oxidation.

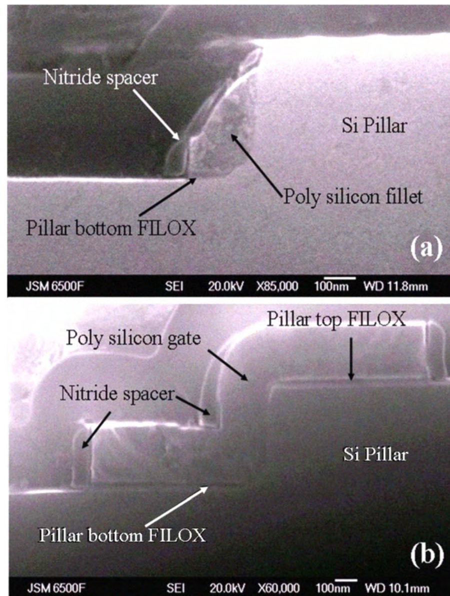

Fig. 3: SEM cross-section of the nitride spacer process prior to silicidation for a) surround gate device and b) frame gate device.

The channel length has been estimated from device wafers by stain etching in a $HF:HNO_3$ =1:400 solution to delineate junctions. For a 10 second RTA at 1100°C, a channel length of 120 nm is obtained for a 350 nm pillar height. For a 30 second RTA at 1100°C, a channel length of 80 nm is obtained.

4. ELECTRICAL RESULTS

Fig. 4 shows the output characteristics of 120nm surround gate vertical MOSFETs with and without silicidation. For the drain-on-top mode of operation in Fig. 4(a), the silicided transistors show a significantly improved drive current. The drive currents for a gate voltage over-drive of 1V and a V_{DS} of 1.5 V are found to be 180 and 240 μA/μm for non-silicided and silicided transistors respectively, indicating a 30% drive current improvement. Below V_{DS}=1V, a non-linear transistor turn-on effect can be seen in the characteristic of the silicided device. In contrast, for source-on-top mode of operation in Fig. 4(b), it can be seen that the drive current of the silicided device is significantly lower than that of the non-silicided device. Possible explanations for this behaviour will be discussed later.

Fig. 5 shows the effects of silicidation on the transfer characteristics of surround gate vertical MOSFETs with a channel length of 120 nm. For the non-silicided device a sub-threshold slope of 78 mV/decade and a DIBL of 20mV/V are observed. A gradually increasing off-state leakage current is found with increasing negative gate bias which can be attributed to gate induced drain leakage (GIDL) due to the high body doping of $10^{18}/cm^3$ and the source/drain doping of $10^{21}/cm^3$. For the silicided device, a small degradation of the sub-threshold slope and DIBL are observed with values of 85 mV/decade and 40 mV/V. The off-state leakage is also higher in the silicided device.

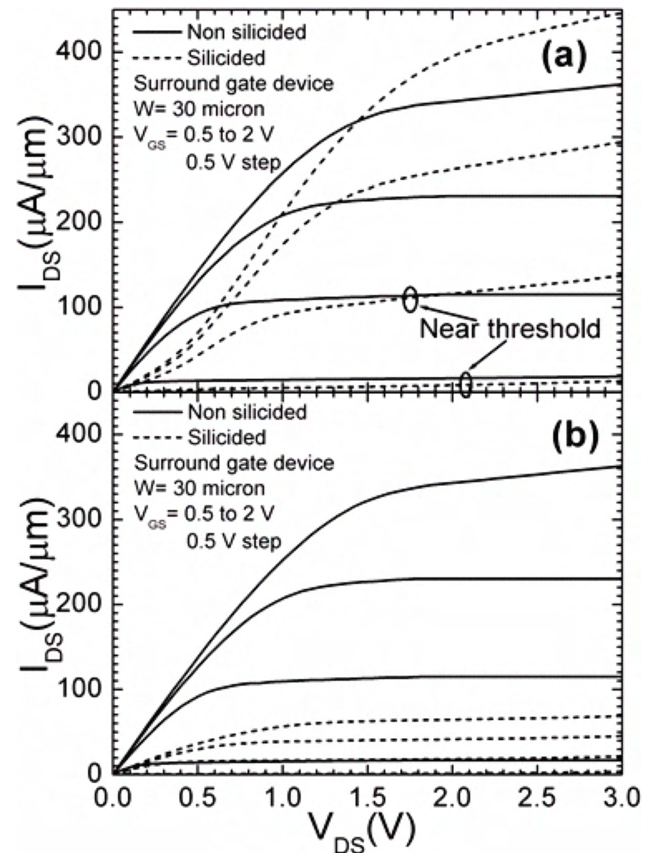

Fig. 4: Output characteristics of n-channel surround gate vertical MOSFETs with and without silicidation for a channel length 120 nm, a) drain-on-top and b) source-on-top mode of operation.

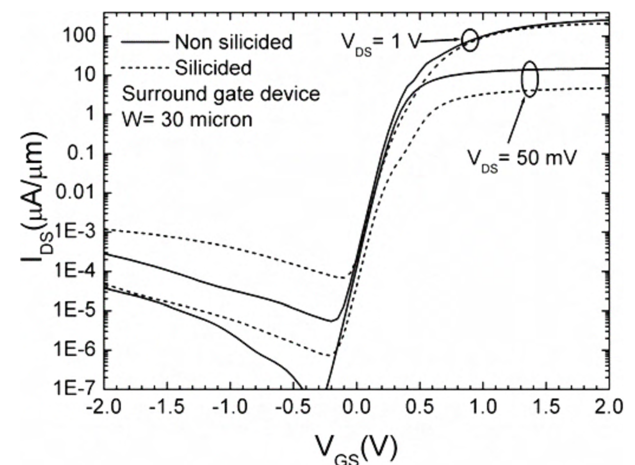

Fig. 5: Transfer characteristics of n-channel surround gate vertical MOSFETs with and without silicidation for a channel length 120 nm. The results are presented for drain-on-top mode of operation.

Fig. 6 shows the effects of silicidation on the transfer characteristics of frame gate devices for a channel length of 120 nm and for the drain-on-top mode of operation. The non-silicided and silicided devices exhibit similar sub-threshold slopes and DIBL characteristics with values of 77 and 78 mV/decade and 35 and 30 mV/V respectively. The silicided devices show a significantly improved drive current at both low and high drain biases.

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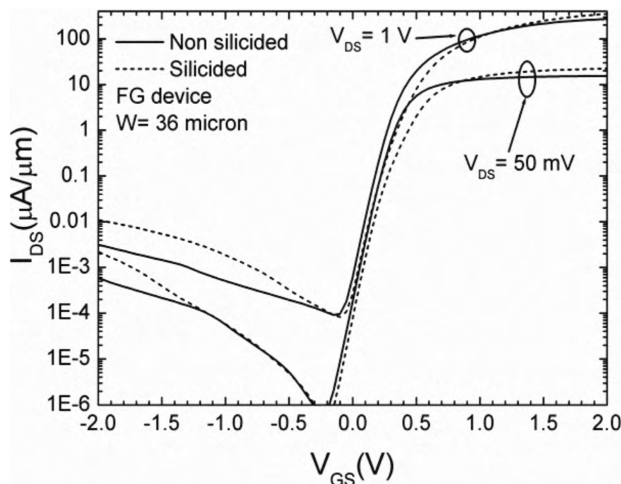

Fig. 6: Transfer characteristics of n-channel frame gate vertical MOSFETs with and without silicidation for a channel length 120 nm. The results are presented for drain-on-top mode of operation.

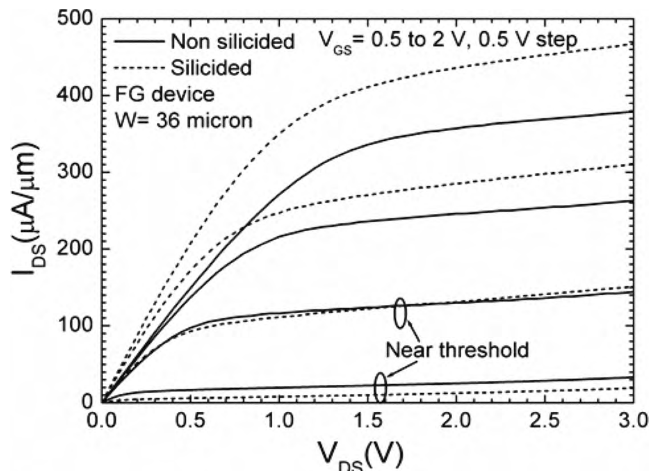

Fig. 7: Output characteristics of n-channel frame gate devices with and without silicidation for a channel length 120 nm. The results are presented for drain-on-top mode of operation.

Fig. 7 shows the output characteristics of frame gate devices with and without silicidation for a channel length 120 nm and for drain-on-top mode of operation. A significant improvement in the drive current can be seen for the silicided devices and there is no non-linear transistor turn-on effect in the characteristic, as was seen in Fig. 4(a) for the surround gate device. The drive currents for a gate voltage over-drive of 1V and a V_{DS} of 1.5 V are found to be 190 and 250 μA/μm for non-silicided and silicided transistors respectively, indicating a 30% drive current improvement in the silicided device. Identical behaviour is observed during source-on-top mode of operation.

Fig. 8 shows the effects of silicidation on the transfer characteristics of frame gate devices for a channel length of 80 nm and for the drain-on-top mode of operation. As for the longer channel length transistors, the drive current of the silicided devices is again significantly improved. However, the leakage current at negative gate biases is higher than that observed in Fig. 5 for the device with a longer channel length. This result can be explained by the deeper S/D junctions created with the 30 second RTA at 1100ºC. Hence, the GIDL will be higher due to the increased gate-S/D overlap.

Fig. 9 shows the output characteristics of frame gate devices with and without silicidation for a channel length 80 nm and for drain-on-top mode of operation. A significant drive current improvement can again be seen in the silicided devices. The drive currents at a gate voltage over-drive of 1V and at a V_{DS} of 1.5 V are 230 and 330 μA/μm for non-silicided and silicided tranistors respectively, indicating a 43% drive current improvement in the silicided device. Similar behaviour is observed during source-on-top mode of operation.

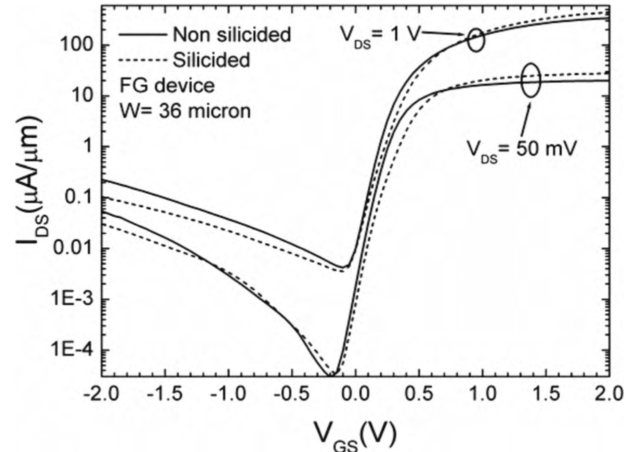

Fig. 8: Transfer characteristics of n-channel frame gate vertical MOSFETs with and without silicidation for a channel length 80 nm. The results are presented for drain-on-top mode of operation.

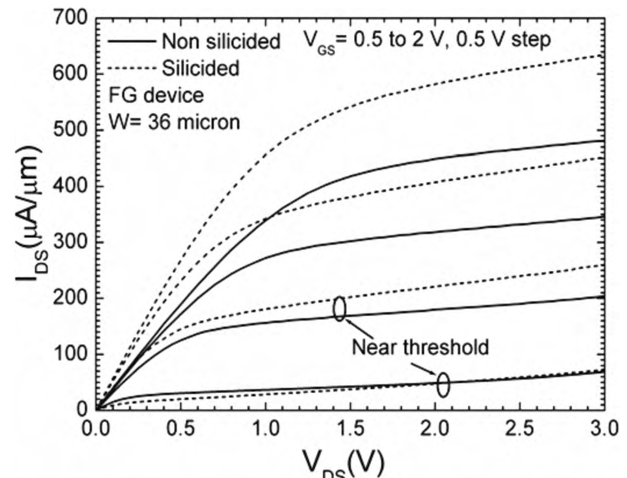

Fig. 9: Output characteristics of frame gate devices with and without silicidation for a channel length 80 nm. The results are presented for drain-on-top mode of operation.

5. DISCUSSION

The above results show that the silicidation process has given an improvement in drive current for both conventional surround-gate vertical MOSFETs and frame gate vertical MOSFETs. Table I compares electrical results of these two types of device with other results reported in the literature. The data has been taken from [4] and updated with more recent results. To ensure a meaningful comparison, fully depleted, thin pillar vertical MOSFETs are excluded from the table, because improved drive would be expected from these devices due to the volume inversion from the action of the dual or surround gates. I_{on} has been calculated for V_{DS}=V_{DD} and for a 1V gate-overdrive. As can be seen, the silicided frame gate devices have an improved drive capability as well as maintaining state of the art values of sub-threshold slope and DIBL. It is worth mentioning at this point that scaling the pillar thickness in the fully depleted regime though has been shown to deliver excellent sub-threshold and DIBL characteristics, the expected improvement in drive current

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has only been demonstrated for pillar diameters of less than 20 nm, where a very strong volume inversion exists in the channel [1-3]. When only moderate volume inversion is present, the drive current is usually limited by severe S/D series resistance effects and the drive current is generally ≤200 μA/μm at the bias conditions presented in table I [1-2]. This indicates that the above silicidation process has delivered a performance comparable to that achievable in fully depleted MOSFETs.

Table I: Comparison of the silicided surround gate and frame-gate devices with reported results from the literature

Parameter	L (nm)	t_{ox} (nm)	N_A (10^{17}/cc)	V_{DD} (V)	Ion (μA/μm)	S (mV/dec)	DIBL (mV/V)
Schulz et al [4]	100	3	20	1.5	240	102	70
Schulz et al [4]	50	3	70	1.5	80	166	300
VRG [7]	100	2.8	35	1.5	140	90	30
VRG [7]	50	2.8	35	1.5	100	105	90
Mori et al [8]	100	7	20	1.5	160	100	73
Gili et al [5]	125	3	40	1.5	127	107	80
Previous report [6]	100	2.6	10	1.5	160	70-80	30-35
Silicided surround gate (this work)	120	2.5	10	1.5	240	85	40
Silicided frame gate (this work)	120	2.5	10	1.5	250	78	30
Silicided frame gate (this work)	80	2.5	10	1.5	330	85	70

The results in table I show that an improved drive current is achieved by the above silicidation process for both surround gate and frame gate transistors. However, the silicided surround gate transistors exhibit a non-linear transistor turn-on in drain-on-top operation and a dramatically reduced drive current in source-on-top operation (Fig. 4). At first sight, these results suggest that the metal contacts on the top of the pillar in the silicided surround gate transistors are rather poor. However, the silicided surround gate devices were measured on the same wafer as the silicided frame gate devices, which have excellent metal S/D contacts, as can be seen from the improved values of drive current compared with unsilicided devices (Fig. 7). It can therefore be concluded that the non-linear transistor turn-on effect observed for silicided surround gate transistors (Fig. 4) is not due to poor metal S/D contacts on the top of the pillar. An alternative explanation for this behaviour is structural differences between the frame gate and conventional devices. As can be seen in Fig. 3, for the frame gate transistor the silicided region is far from the pillar sidewall and the S/D junction, whereas for the conventional surround gate transistor it is very close to the top junction around the pillar sidewall. This reasoning suggests that the non-linear transistor turn-on is directly due to the silicidation process on the pillar sidewall. The doping concentration near the junction on the pillar sidewall is lower than that on the pillar top. Hence the silicidation process on the pillar sidewall may be less effective than on the top of the pillar and as a result, a Schottky contact could be formed on the pillar sidewall. This rectifying contact could explain both the Schottky-like behaviour in Fig. 4(a) and the low drive current in Fig. 4(b). This problem can be solved by giving a longer RTA to create a deeper junction. For a 30s RTA, the non-linear transistor turn-on is not present in the surround gate transistors and a drive current of 402 μA/μm is obtained at the bias conditions presented in table I. Additionally, the silicidation process may introduce some trapping states on the pillar sidewall. Some evidence of the presence of trapping states can be seen in the small degradation of the sub-threshold slope in the silicided surround gate transistors. A further contribution to trapping states could come from the additional dry etch step that was used in the silicided transistors to remove the FILOX layer after gate etch [6]. However, the frame gate architecture provides an excellent solution for siliciding vertical MOSFETS. The main disadvantage of the frame gate architecture is increased gate/source and gate/drain overlap capacitance where the polysilicon frame overlaps the top and bottom of the pillar. However, combining frame gate architecture with the FILOX process, as in the current work, provides a thick oxide (typically 20 times thicker than the gate oxide) at the top and bottom of the pillar that compensates for this disadvantage. The overlap capacitance can also be controlled by minimising the polysilicon overlap at both the pillar top and bottom.

6. CONCLUSIONS

A silicidation technology for surround gate vertical MOSFETs has been described for the first time. The technology used a nitride spacer on top of the polysilicon spacer that is used as the surround gate. The silicided transistors showed a significant improvement in drive current in drain-on-top operation, but a degraded drive current in source-on-top operation. These results have been shown to be due to the silicidation process on the pillar sidewalls at the top of the pillar. This problem has been solved using a frame gate architecture that protects the pillar sidewall during silicidation. Silicided frame gate vertical MOSFETs showed a promising improvement in the drive current. This improvement was 30% for transistors with a channel length of 120 nm and 43% for transistors with a channel length of 80 nm.

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REFERENCES

[1] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki, "Ultrathin channel vertical DG MOSFET fabricated by using ion-bombardment-retarded etching," IEEE Trans. Electron Devices, vol. 51, pp. 2078-2085, December 2004.

[2] H. Cho, P. Kapur, P. Kalavade and K. C. Sarasawat, "A Low-power, highl scalable, vertical double-gate MOSFET using novel processes," IEEE Trans. Electron Devices, vol. 55, pp. 632-639, February 2008.

[3] B. Yang, K. D. Budhdharaju, S. H. G. Teo, J. Fu, N. Sing, G. Q. Lo and D. L. Kwong, "CMOS compatible gate-all-around vertical silicon-nanowire MOSFETs," in 38th Conference of European Solid-State Device Research (ESSDERC), 2008, pp: 318 – 321.

[4] T. Schulz, W. Rösner, L. Risch, A. Korbel, and U. Langmann, " Sort-channel vertical sidewall MOSFETs," IEEE Trans. Electron Devices, vol. 48, pp. 1783–1788, August 2001.

[5] E. Gili, C. H. Groot, V. D. Kunz, T. Uchino, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang, P. L. F. Hemment, "Single, Double & Surround Gate Vertical MOSFETs with Reduced Parasitic Capacitance"" Solid State Electronics, vol.48, pp. 511-519 . April 2004.

[6] M. M. A. Hakim, L. Tan, T. Uchino, O. Buiu, W. R. -White, S. Hall and P. Ashburn, "Improved Sub-threshold Slope in RF Vertical MOSFETS using a Frame Gate Architecture," in 38th European Solid-State Device Research Conference (ESSDERC), 2008, pp. 95-98.

[7] J. M. Hergenrother et al, "The vertical replacement (VRG) MOSFET: A 50 nm vertical MOSFET with lithography-independent gate length," in IEDM Tech. Dig., 1999, pp. 75–78.

[8]K. Mori, A. Duong and W. F. Richardson, "Sub-100 nm vertical MOSFET with threshold voltage adjustment," IEEE Trans. Electron Devices, Vol. 49, pp. 61-66, January 2002.

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