DC–35 GHz low-loss MMIC switch using 50 nm gate-length MHEMT technology for ultra-low-power applications

C.-J. Hwang, H.M.H. Chong, M. Holland, I.G. Thayne and K. Elgaid

A broadband low-loss, ultra-low-power consumption transmit/receive switch using high-performance 50 nm gate-length metamorphic high electron mobility transistors (MHEMTs) is presented. The single pole double throw (SPDT) monolithic switch utilises a drain contact electrode sharing concept using a two-finger MHEMT. An optimal gate width of the MHEMT was chosen for low-loss, high-isolation performance and circuit compactness. The switch shows a broadband operation from DC to 35 GHz with insertion loss less than 1.9 dB, isolation better than 27 dB, and P_{1dB} better than 12 dBm with DC power consumption of less than 6 μW.

Introduction: The development of millimetre-wave circuits has been reported using HEMTs of various materials including InP-based HEMTs and GaAs pseudomorphic HEMTs (PHEMTs). The InP-based HEMTs have demonstrated high-frequency and low-noise performance compared to the GaAs PHEMTs. However, InP-based HEMTs have the mechanical fragility of the substrate and higher device cost. In recent decades, GaAs MHEMTs have been applied to millimetre-wave circuits for overcoming device cost and frequency performance of InP-based HEMTs and GaAs PHEMTs [1–3]. The use of metamorphic buffers on GaAs substrates was introduced to accommodate the lattice mismatch between the substrate and active layers as well as to avoid InP substrates. By using the metamorphic buffers, unstrained InAlAs-InGaAs heterostructures could be grown over a wide range of indium contents for the InGaAs channels, therefore the MHEMT devices exhibit device performance comparable to those of InP-based HEMT devices.

In this Letter, 50 nm gate-length MHEMTs with a δ-doped $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$-based SPDT switch is demonstrated for low loss and high isolation as well as ultra-low-power consumption over a broadband frequency range [4]. The optimal gate widths of series MHEMT switches are simulated with the extracted device parameters to realise low insertion loss and high isolation performance. The simulated insertion loss and isolation characteristics agree well with the experimentally measured results.

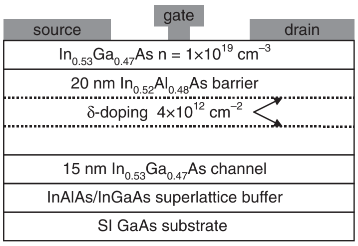

Fig. 1 *Device cross-section of 50 nm gate-length MHEMTs with δ-doped $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$ profile*

Device description: The 50 nm GaAs MHEMT structures with δ-doped $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$ profile, as shown in Fig. 1, were grown by molecular-beam epitaxy on semi-insulating GaAs substrates. The double δ-doped strategy was used to increase drive current, reduce access resistance and enhance linearity. The 1200 nm metamorphic buffer was graded linearly from GaAs to $In_{0.53}Ga_{0.47}As$ and was followed by a 72 nm-thick $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$ superlattice prior to the growth of the device layers. In the process of the device, the reduction of ohmic contact resistance is important for switch circuits because ON-state resistance (R_{ON}) is represented by the sum of ohmic contact and channel resistances. The separation of the source to drain terminals is also an important device process for the switch circuit because ON-state resistance (R_{ON}) and OFF-state capacitance (C_{OFF}) are controlled by the separation. Ohmic contact resistances as low as 0.06 Ω mm were obtained using an annealed 150 nm-thick Au:Ge:Ni-based metallisation. Devices were realised using a 1.1 μm source to drain terminal. As to the MHEMT DC performance, the drain to source current (I_{ds}) against drain to source voltage (V_{ds}) curve and the transconductance (g_m) curve are shown in Fig. 2. It exhibits excellent device pinch-off characteristics and the maximum I_{ds} and g_m are 41 mA (820 mA/mm) and 1010 mS/mm, respectively.

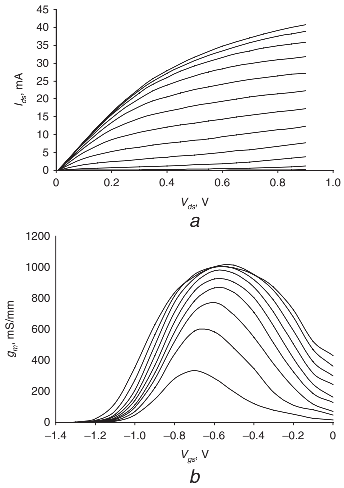

Fig. 2 *I–V curve and transconductance (g_m) curve of 2 × 25 μm, 50 nm gate-length MHEMTs with δ-doped $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$ profile (V_{ds} = 0.1 V to 0.9 V and V_{gs} = 0V to −1.4 V, 0.1 V step)*

a I–V curve
b Transconductance curve

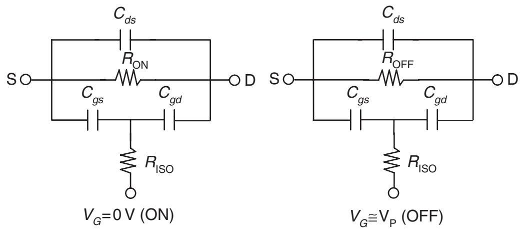

Fig. 3 *ON and OFF states simplified equivalent circuits of MHEMTs in switch circuit*

SPDT switch design: In this work, the device layer structure, topology and layout were all taken into consideration to realise a high-performance switch targeted at wireless sensor networks. The design issues associated with the optimisation of the series SPDT MHEMT switch are strongly influenced by choice of device width. Increasing the device width will result in smaller values of R_{ON}, and therefore lower insertion loss in the ON-state. This reduction of insertion loss will be at the expense of reduced isolation in the OFF-state owing to the increase of C_{ds} and C_{gs}. Therefore a trade-off for low loss, high isolation and circuit compactness is essential for high performance. In this work, a single, two-finger MHEMT in a coplanar waveguide (CPW) configuration was used as the switch and it optimised the gate width at 25 μm for low loss and high isolation. The independent bias of each gate finger controls the routing of the RF signal from the drain terminal to the source terminal. This layout technique also eliminates impedance mismatch between the CPW and the device [5]. Cold HEMT operation was utilised to minimise power consumption. Fig. 3 shows the equivalent circuits of the SPDT switch. In the ON-state, C_{ds}, C_{gs}, and C_{gd} are not critical parameters compared with R_{ON}, therefore an equivalent circuit can be represented by R_{ON}. In the OFF-state, R_{OFF} has an adequately large value for applying an open circuit; consequently, C_{ds}, C_{gs}, and C_{gd} are dominant parameters for OFF-state switch performance [6, 7]. Extracted values of R_{ON} and C_{OFF} for ON ($V_G = 0$ V) and OFF ($V_G = -1.8$ V) states are 2–3 Ω and 6–7 fF, respectively. The circuitry controlling the gate bias included a 1 kΩ resistor R_{ISO} to attenuate unwanted RF signal leakage via the gates. Fig. 4 shows a microphotograph of the series SPDT MMIC switch with a 25 μm gate-width, 50 nm gate-length MHEMT fabricated using CPW MMIC technology. The total chip area including probe pads is 1.5 × 1.2 mm^2.

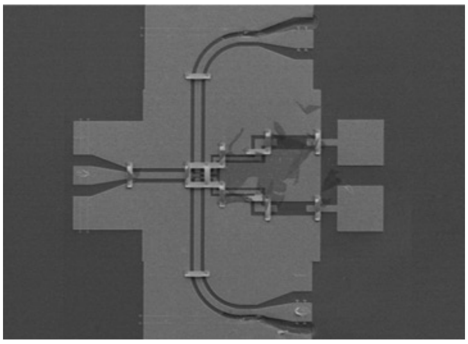

Fig. 4 *Microphotograph of fabricated SPDT MMIC switch*

Total chip size including probe pads is 1.5 × 1.2 mm^2

Results: For MMIC switch fabrication, a gate width of 25 μm was chosen as this met the required insertion loss and isolation required for the intended application. The switch was designed to achieve broadband characteristics from DC to 35 GHz to cover the range of ISM bands being targeted, especially a 24 GHz RF transceiver with ultra-low-power consumption for wireless sensor networks. Fig. 5 compares the simulated and measured insertion loss and isolation responses of the MMIC switch utilising the 50 nm GaAs MHEMT with 25 μm width. The insertion loss is less than 1.9 dB and isolation is greater than 27 dB across the frequency range from DC to 35 GHz. There is good agreement between simulated and measured results. Fig. 6 shows the insertion loss and isolation response against input power at 24 GHz. The measured P_{1dB} responses of insertion loss and isolation are observed at input powers of 14 and 12 dBm, respectively. With signal input power of −10 dBm, a leakage current of less than 1.3 nA is observed. This DC power consumption in the ON-state is less than 0.1 nW. The OFF-state voltage is −1.8 V, with gate leakage current of less than 3.22 μA, leading to a maximum power consumption of less than 6 μW.

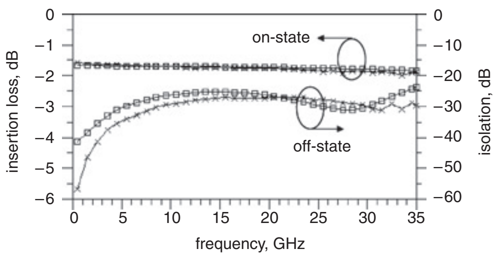

Fig. 5 *Simulation and measurement results of series SPDT switch using 2 × 25 μm, 50 nm gate-length MHEMTs*

□ simulation

× measurement

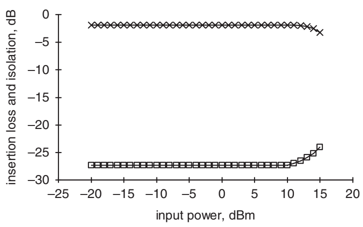

Fig. 6 *Measured insertion loss and isolation against input power at 24 GHz*

□ insertion loss

× isolation

Conclusions: This letter reports a 50 nm GaAs MHEMT SPDT switch with low DC power consumption and low insertion loss over a broadband frequency range. The DC power consumption of the switch is less than 6 μW, the insertion loss is less than 1.9 dB and isolation is more than 27 dB from DC to 35 GHz. These results demonstrate the outstanding potential of 50 nm GaAs MHEMT device technology for ultra-low-power applications.

13 March 2009

doi: 10.1049/el.2009.0684

C.-J. Hwang, M. Holland, I.G. Thayne and K. Elgaid (*Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow G12 8LT, United Kingdom*)

E-mail: cjhwang@elec.gla.ac.uk

H.M.H. Chong (*Nano Research Group, School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom*)

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