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Double-polysilicon self-aligned lateral bipolar transistors

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Abstract A new lateral bipolar junction transistor that utilises a double-polysilicon self-aligned structure to maximise high-frequency performance is introduced. Silicon-on-oxide (SOI) wafers are used to isolate devices from the substrate and to minimise parasitic substrate capacitances (C_{JCS0}) around 1.3–2.6 fF (substrate is ground). A SOI thickness of 0.2–0.5 μm combined with 0.13–0.25 μm lithography could allow a reduction of transistor dimensions down to (0.2–0.5) × (0.13–0.25) μm^2 and give an estimated minimum emitter/base junction capacitance (C_{JE0}) of 0.54–1.36 fF. Simple device isolation is predicted to produce a small collector/base junction capacitance (C_{JC0}) of 0.42–2.00 fF. Furthermore, use of a double base contact can help reduce base resistance (R_B) to 0.43–1.17 kΩ and a wide collector window directly contacted to the collector is estimated to result in around 0.66–1.58 kΩ collector resistance (R_C). By taking all parameters into account a cut-off frequency (f_T) of 69–116 GHz and maximum oscillation frequency (f_{max}) of 61–128 GHz is predicted for this design, in addition a gain of 47–101 (using minimum gain enhancement) and roughly 10.6–21.0 ps ECL propagation delay time, at a current of 0.4–1.0 mA could be achieved. Our simulations indicate that this new doubled-polysilicon self-aligned structure could outperform all other silicon bipolar transistors that have been reported.

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1 Introduction

With high consumer demand in the wireless communication market, technology is not just focused on higher performance but also on the reduction of manufacturing costs. BiCMOS (HBTs) and RFCMOS (NFETs) technologies are perhaps the main contenders in this market stream [1].

An emerging new design is the lateral bipolar transistor technology (LBJT) based on Silicon-on-oxide (SOI) substrates [2, 3], high performance LBJTs, that provide f_t/f_{max}—16/46 GHz and are more compatible to CMOS fabrication processes, allow potential integration into BiCMOS technologies on SOI. This LBJT technology might be expected to lower the cost of fabrication and possibly helps to compensate the additional cost of the SOI wafer. This paper introduces a new design of lateral bipolar transistor that combines double polysilicon deposition and a new self-aligned technique that is expected to improve the high-frequency performance of devices. Physics and characteristic predictions of the new design have been investigated.

2 Process design

Figure 1 shows a schematic diagram of the new lateral BJT. We start with a 200–500 nm thick SOI wafer that is initially n-type material and in itself suitable to act as the collector of the transistor. Low temperature oxide (LTO) is deposited on the top of SOI wafer, with thickness of 200 nm, isolating the collector from further processes.

An oxide window is then opened for boron implantation and an annealing process drives-in a thin highly p+ region of 4×10^{18} cm^{-3} to form base strip under the top oxide. The 90–120 nm junction depth of collector/base junction

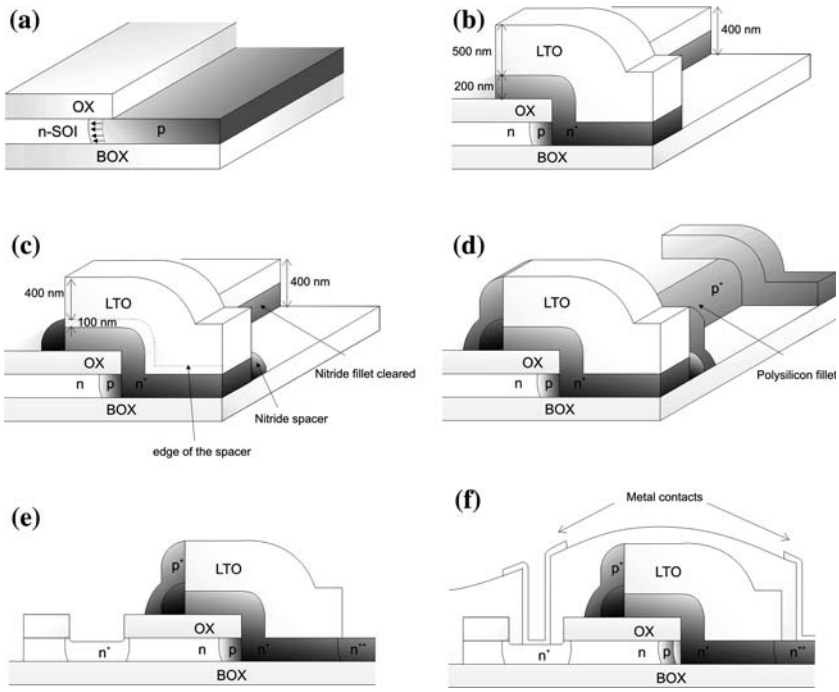

Fig. 1 Schematic diagram of the new lateral bipolar transistor fabrication process

roughly measured from the edge of the opened window (Fig. 1a) significantly reduces the extrinsic base resistance. Next, a deep silicon anisotropic etch by a plasma etching process opens a sidewall for emitter and base contacts. At this stage, 200 nm of polysilicon is deposited and an arsenic implant for emitter doping concentration of 1×10^{20} cm^{-3} is carried out followed by a second LTO deposition with a thickness of 500 nm. The LTO layer and the n+ polysilicon are then patterned in order to localise the emitter area (Fig. 1b). The next stage is a nitride deposition of 100 nm followed by anisotropic plasma etch to leave nitride spacers protecting the perimeter of the n+ polysilicon, the difference between the thickness of the LTO and the base wall makes this possible (Fig. 1c). It can be seen that margin on the thicker of LTO will give more control on the timing of the etch and this is important since exposure of extrinsic base along with existence of the spacer is paramount. The next stage is the deposition of a p+ extrinsic polysilicon base contact. By using anisotropic plasma etch and mask protection for the metal contact area, the polysilicon base contact will be perfectly formed (Fig. 1d). This self-aligned polysilicon base contact is extremely useful and helps reduction of extrinsic base resistance especially in this particular design, since use of this side contact base the extrinsic base resistance can be very high due the small cross-section area. However the use of multi base contact will give additional help by reducing the base resistance. After this critical process, the oxide window will be opened for both collector and emitter contact areas followed by the implant of high n+ dopant to provide ohmic contacts. Then device isolation is performed followed by oxide passivation and contact windows will be opened (Fig. 1e). Annealing process and titanium-silicide of all contacts completes the device (Fig. 1f). This fabrication method could produce transistors with a base width (W_B) of 0.016–0.03 μm and an emitter width (W_E) of 0.06–0.01 μm.

3 Physics of the device and characteristic prediction

Figure 2 shows the top view of the device and Fig. 3 also shows three-dimensional cross-section of active areas of the device. These are used to evaluate all important parameters and figures of merit of the transistor. The simplicity of the device structure allows traditional one dimension prediction of all resistances and capacitances of the transistor's three terminals and we can estimate extrinsic and intrinsic base resistance as

$$R_{BX} = \frac{\rho_B \frac{L_0}{W_{Bx}d} + R_{BCON}}{n_B} \quad (1)$$

$$R_{Bi} = C\frac{\rho_B \frac{L_1}{W_{Bi}d}}{n_B^2} \quad (2)$$

where n_B is number of base contact windows and C is a constant which takes the value of 1/3 at low current [4]. It can be seen that this design structure has gained benefits from multi-base contact design.

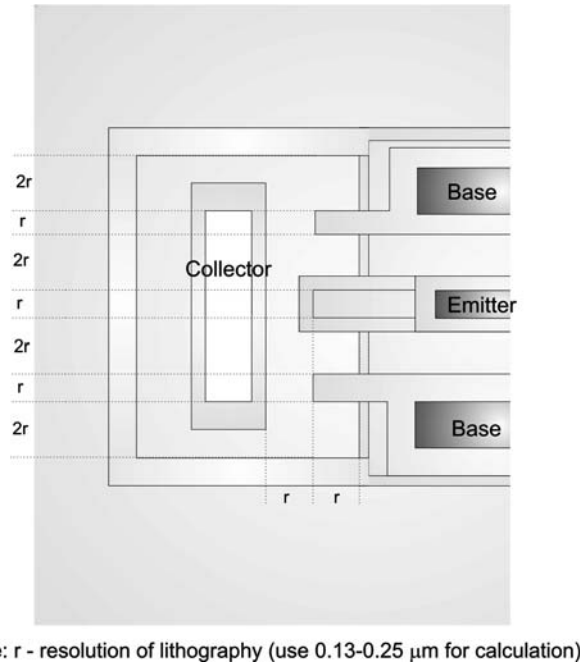

Fig. 2 Schematic diagram of top view design

The use of the polysilicon emitter contact means that the emitter resistance will be significantly higher than for a conventional emitter. We presume the use of polysilicon emitter as just a metallurgic contact and epitaxially regrown emitter [5] is used in our design, thus the emitter resistance can be estimated

$$R_E = \frac{\rho_E \frac{W_E + W_{Poly}}{L_1 d} + R_{ECON}}{n_E} \tag{3}$$

Considering the collector resistance, the lateral transistor structure gives the advantage of direct contact to the collector and this helps a reduction of the many fabrication processes that are required for collector contact formation in conventional vertical bipolar transistors. However a large resistance of the collector is a draw back since collector width is specified by lithography resolution (r). Fortunately, use of a widened collector contact will help to significantly reduce the total R_C. Figs. 3a and b show schematic diagrams of the resistance components of the collector. Both extrinsic collector resistances (R_{Cx}) help to improve current drive by their parallel formation to intrinsic collector resistance (R_{Ci}). R_C can be approximated by:

$$R_C = \frac{\rho_C W_C}{d n_E (L_1 + L_2)} + R_{CCON} \tag{4}$$

where n_E is the number of emitter contacts used.

Taking heavy doping effects and polysilicon emitter contact into account, the collector and base currents are calculated using effective doping concentrations in both the base and the emitter and the base current has been modified with an effective recombination velocity (S_{EFF}) [5] to take an interfacial oxide layer at the polysilicon/silicon interface into account. Cut-off frequency f_T and f_{max} estimates are derived from the small-signal hybrid- π model [4].

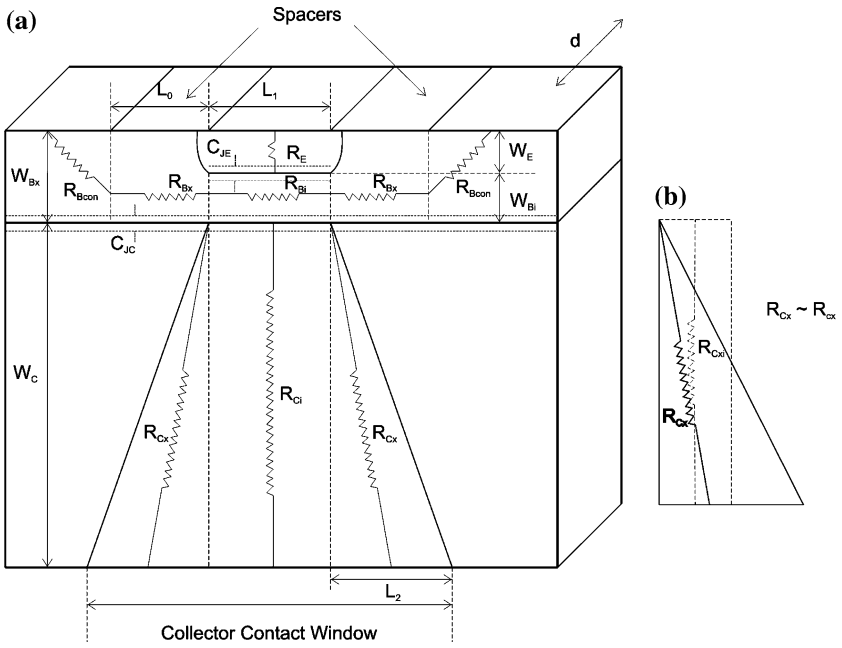

Fig. 3 Schematic diagrams of the device show transistor's components that used in calculations

Table 1 Comparison of results Nii, our calculated values for the device described by Nii and our proposed device

Parameter	Nii (2000)	Calculation	New device
Lithography	–	–	0.13–0.25 μm
A_E	0.12 × 3.0 μm^2	0.12 × 3.0 μm^2	(0.2–0.5) × (0.13–0.25) μm^2
h_{FE}	88	76	47–101
Peakf_T	12 GHz	12.3 GHz	69–116 GHz
Peakf_{max}	67 GHz	66 GHz	61–128 GHz
R_E	36 Ω	31 Ω	22–51 Ω
R_B	270 Ω	108 Ω	0.43–1.17 kΩ
R_C	850 Ω	873 Ω	0.66–1.58 kΩ
C_{JE0}	1.5 fF	1.56 fF	0.28–1.36 fF
C_{JC0}	1.4 fF	1.33 fF	0.42–2.00 fF
C_{JCS0}	2.5 fF	2.7 fF	1.3–2.6 fF (Sub. GND)
Va	17.5 V	–	–
BV_{CEO}	5.3 V	5.27 V	<5.27

Note: Use double emitter contacts and triple base contacts for calculation of the new devices

$$f_T = \frac{1}{2\pi\left(\tau_F + R_C C_{JC} + \frac{kT}{qI_C}(C_{JE} + C_{JC})\right)} \quad (5)$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{JCR_B}}} \quad (6)$$

where τ_F is forward transit time, which is a combination of each transit time in base, emitter and collector/base depletion region. ECL propagation delay has been estimated by use expression of $\tau_D = \sum_i K_i R_i C_i + \sum_j \tau_j$ [6].

To evaluate our device and validate our calculations we have applied similar techniques to the device described by Nii et al. [7] as a reported example of a lateral SOI transistor. The results of our calculations are compared to the reported measurements [7] are shown in Table 1 and indicate that our calculation processes are reasonably accurate.

These models also benefit from our earlier work [8] which used commercial simulation packages, to compared double polysilicon lateral SiGe heterojunction bipolar (HBT) designs with a conventional vertical SiGe HBT [9].

Finally, figure 4 shows the outcome of one of our first development processes aimed at building our proposed device. In this case the scanning electron microscope (SEM) of the cross-section of a device sidewall shows the growth of a thin SiGe layer and a polysilicon layer, in this case using SiGe allowed us to closely observe the features of the sidewall but also indicates the feasibility of our designs including applicability to the formation of Si/SiGe HBT.

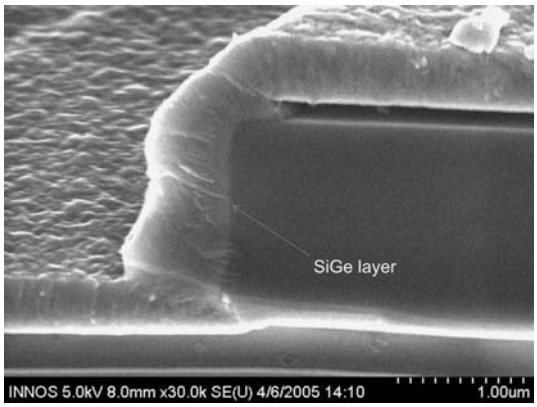

Fig. 4 Scanning electron microscope photograph of development batch of the device show polysilicon deposition on SOI sidewall

4 Summary

In this work, a lateral Si BJT with a double polysilicon-emitter and polysilicon-base contact is presented. The transistor design is based on SOI sidewall formation and multi contacts of emitter and base. Calculation results show this design of the lateral transistor to improve high frequency performance overall which could possibly achieve f_T/f_{max} of 116/128 GHz with 14.2 ps ECL propagation delay time at around collector current of 0.7 mA on 0.13 μm lithographic node highlighted the feasibility of the design. Further improvements in the transistor design and characterization of impurity implantation on the sidewall would allow the transistor to operate at maximum cut-off frequency with low current density among Si BJT technology which also adds significant benefit of SOI based ICs over conventional bulk silicon.

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