Design of New Logic Architectures Utilizing Optimized Suspended-Gate Single-Electron Transistors

Benjamin Pruvost, Ken Uchida, Hiroshi Mizuta and Shunri Oda

***Abstract*— The operation and performances of the suspended-gate single-electron transistor are investigated through simulation. The movable gate is 3-dimensionally optimized so that low actuation voltage (0.4V), fast switching (1 ns) and ultra-low pull-in energy (0.015 fJ) are simulated. A two-state capacitor model based on the 3D results is then embedded with a single-electron transistor analytical model in a SPICE environment to investigate the operation of the device. Through the control of the Coulomb oscillation characteristics, the position of the movable gate enables a background charge insensitive coding of the information. New circuit architectures with applications in cellular non-linear network and pattern matching are also proposed and simulated.**

***Index Terms*— Nanoelectromechanical system (NEMS), cantilever switch, movable gate, single-electron transistor (SET), 1D and 3D modeling.**

I. Introduction

SINGLE-electron transistors (SETs) can potentially be applied to general purpose Boolean logic while delivering high device density and power efficiency. However, whereas the problem of the inherent low fan-out can be overcome by combining the SET with conventional FET [1], its sensitivity to background charge still makes the practical implementation of SET in logic circuits problematic. By altering the island potential, a random background charge can indeed alter the operating characteristics of the device, thereby making the output from the device unreliable. Attempts to fabricate devices free of background charge have not been sufficiently successful and tuning each island to compensate for the corresponding change is considered to be ineffective, especially for a circuit containing many islands or in presence of dynamic background charges. Neural network concepts [2], which use hardware redundancy to teach the network to cope with charges, require larger circuits, while a problem of the feedback control [3] is that the loop needs to be itself insensitive to the background charge, since any charge appearing near the node created to charge the feedback capacitor will result in an error. Rather than trying to suppress these effects, one solution is to make logic information insensitive to them by getting the necessary redundancy from the amplitude or the periodicity of the oscillations, which are not altered by the background charges [4]. For the encoding of the logic information, suspended-gate nanoelectromechanical systems (NEMS) combined with SETs were suggested in [5], and we previously investigated the design optimization of the gate [6]. The experimental observation of such SET transport modulation via the switching of the NEMS device remains however quite challenging, although a first demonstration has been recently reported [7]. The purpose of this work is to evaluate the potential of the device through simulation. The performances of the device, such as scaling, speed, and power dissipation, are analyzed, and optimized device parameters are obtained. It is shown that low switching energy (0.015 fJ) and nanosecond delay can be simulated at low actuation voltage (0.4 V). New circuit architectures utilizing the unique features of both SETs and NEMS are also proposed and simulated.

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II. Device Structure and Design Considerations

A. Operating Principle

The principle of the suspended-gate SET (SG-SET) is depicted in Fig. 1; it combines a NEMS switch with a SET. The NEMS switch is composed of two electrodes: a suspended one, which also acts as a gate for the SET, and a fixed one, which is called the surface electrode and should not interfere with the SET island. As the voltage applied between these two electrodes is increased, the spacing between them continuously decreases until the pull-in effect occurs. Since the spacing between the two electrodes also determines the spacing between the movable gate and the island of the SET and hence the corresponding gate capacitance, the NEMS switch actually acts as a two-state tunable gate capacitor for the SET. The periodicity of the Coulomb oscillations governing the SET characteristics being given by e/C_{Gi}, and their amplitude by e/C_{Σ} (where e/C_{Gi} is the capacitance between the sweeping gate i and the island, and e/C_{Σ} the total island capacitance), one can define two distinct states by switching the gate: one state up with low frequency and/or high amplitude, one state down with high frequency and/or

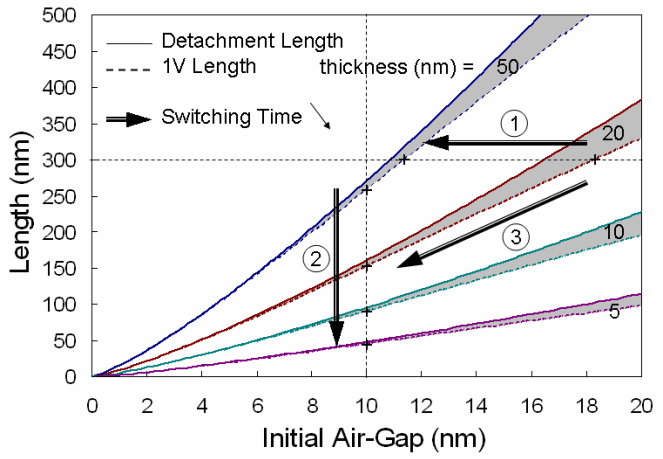

Fig. 2. Detachment length (maximal length due to Casimir force) and length providing 1V pull-in voltage as a function of the initial air-gap for different thicknesses of a conventional silicon cantilever given by the 1D lumped model. The <1V actuation window (grey area) becomes narrower when scaling down the cantilever. Symbols + and arrows 1, 2 and 3 correspond to the sets described in Fig. 3.

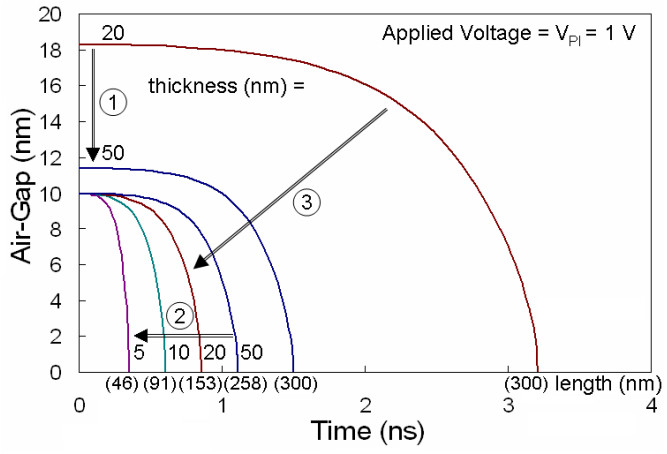

Fig. 3. Switching time for several cantilevers having 1V pull-in voltage. The switching time decreases with: 1- decrease of air-gap and increase of thickness for a given length; 2- decrease of length and thickness for a given air-gap; 3- decrease of length and air-gap for a given thickness. The switching time decreases when scaling down the cantilever.

low amplitude. Since the periodicity and the amplitude of the oscillations are not altered by the random background charges, these two states, which can be decoded by using a filter or a rectifier, are also insensitive to background charges.

B. Gate Design and Performances Analysis

First, we use the methodology and the models and equations described in [6] to determine the dimensions needed to get a nanosecond delay under an actuation voltage lower than 1V. Figure 2 shows the <1V actuation windows (in grey) calculated from the 1D lumped model, including the Casimir force, for Si conventional cantilevers. As expected in [6], the windows become extremely narrow as the dimensions are decreased below 10 nm in the current nanoscale technology. It practically means that for such small dimensions, it is difficult to achieve a low pull-in voltage without the cantilever collapsing under the Casimir force. Figure 3 was obtained by solving the dynamic equation of motion for each of the three sets of cantilevers shown by symbols + and arrows on Fig. 2. It shows that for a given pull-in voltage (1V in this case), the switching time decreases when scaling down the cantilever. Increasing the length of the cantilever to reduce the pull-in voltage is therefore not a viable option for two reasons: because of the area constraint and because it would slow down the switching. The only solution to achieve the nanosecond pull-in under 1V is therefore to reduce the thickness and the initial air-gap below 10 nm.

The design of the movable gate in a 3D environment is essential to further investigate the performances of the device. We use a scaled down version of the cross-shaped structure proposed in [6], which combines large overlap area and certain flexibility, and we provided it with a tip bump in order to decrease the travel range [8]. The electrodes together with the island are modelled and simulated using the finite element analysis provided by COMSOL Multiphysics [9]. Figure 4 shows the dimensions of the considered structure. It is 75 nm long, 5 nm thick and made of silicon, so that the total area occupied by the device is 0.005 μm^2. The air-gap is only 10 nm high at the hinges level and 7 nm at the tip. This extremely reduced air-gap enables to decrease the pull-in voltage to 0.4 V (Fig. 5(a)) and to simulate the nanosecond delay (Fig. 5(b)). To evaluate the movable gate capacitance C_{G2}, we model an ellipsoidal island with the dimensions 4 nm $\times$ 4 nm $\times$ 3 nm, along the x, y and z axes respectively, assuming a 2 nm thick oxide layer covering this island. The capacitance is then calculated using the energy-storage distribution in the electric field and integrating over the considered volumetric domain for each voltage iteration. The gate capacitance is estimated to be around 0.05 aF when the electrode is in the up position and the 0.6 aF in the down position. As a consequence, the other capacitances associated with the quantum island have preferably to be much smaller than the difference between these two capacitances to allow a substantial change in the total island capacitance C_Σ and hence in the amplitude of the Coulomb oscillations. Figure 6 shows a device geometry that could meet this requirement. The fixed gate, the drain and the source capacitances are also calculated with COMSOL and respectively estimated to be C_{G1}=C_D=C_S=0.1aF. Note that the self-capacitance of the island is estimated to be 0.28 aF, which is typical at these dimensions and significant compared to the other capacitances. It acts as a parasitic capacitance which may result in an unfavorable decrease of the oscillations amplitude.

By drastically reducing the tip speed when hitting the island, the bump enables to reduce the switching current to 25 nA (Fig. 7). Note that to simplify, we assumed in this simulation a zero source resistance in series with the cantilever, but in practice, a 1 MΩ resistor is needed to reduce the current density to a reliable range in the cantilever because of its extremely reduced cross section. As a consequence, ultra-low energy consumption (0.015 fJ) is simulated (Fig. 8). For comparison, the minimum switching energy achieved by the present CMOS technology is 0.1 fJ [10], that is almost 7 times

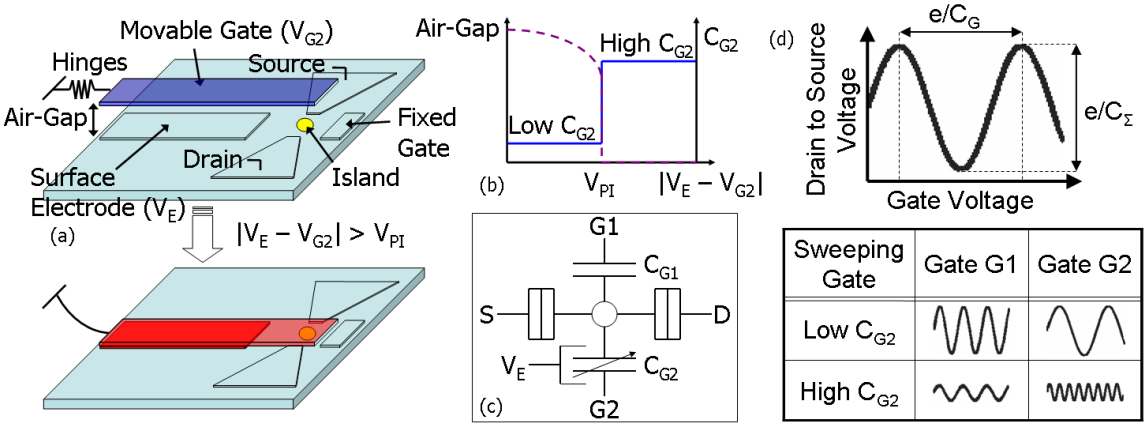

Fig. 1. (a) Concept of the suspended-gate SET device; V_{PI} denotes the pull-in voltage; (b) Gate displacement and corresponding capacitance vs. actuation voltage; (c) Electrical equivalent schematic; (d) Information encoding principle: sweeping Gate G1: encoding in amplitude; sweeping Gate G2: encoding in periodicity.

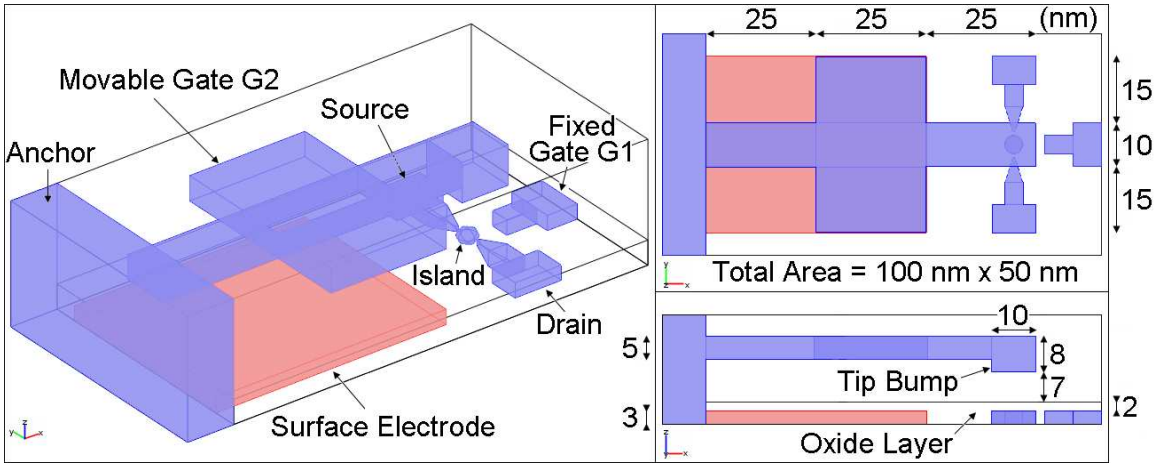

Fig. 4. Sketch of a cross-shaped structure simulated with COMSOL [9].

higher. It is interesting to note that due to the speed of the movable gate, the kinetic energy accounts for a non-negligible part of the switching energy, which emphasizes the role of the bump. Furthermore, because of the small gap capacitance, the electrostatic energy involved in the switching is much lower than the mechanical energy. Charging the load capacitance C_L would require an extra energy $E_{charge} = C_L V_{OUT}^2$, where V_{OUT} is the output voltage of the device, but for a load capacitance of 3 aF (five times the gap capacitance) and an average output voltage of 0.3 V, the charging energy would be only 0.27 aJ, which is not significant compared to the total switching energy for the same reason.

C. Manufacturing Considerations

Fig. 9 shows a possible fabrication process flow for the device, even though we acknowledge that the fabrication of both the genuinely nanoscale cantilever switch and the room-temperature working SET using current technology is still very challenging. First, the transistor and the surface electrode are patterned on the top conductive layer of an SOI substrate, by using for instance the method described in [11] which enables to grow ultra thin (∼1-2 nm) oxide barrier between the island and the leads (Fig. 9(a)). The silicon oxide isolating layer and a silicon nitride sacrificial layer are then successively deposited above the conductive layer and a hole is etched just over the island to form the tip bump (Fig. 9(b)). Finally, a polysilicon layer is deposited on the sacrificial layer and the cantilever is patterned (Fig. 9(c)) before removing the sacrificial layer (Fig. 9(d)).

In addition to the feasibility issues, we can mention the difficulty to correctly align the gate with the island by using such vertical multilayer surface processes, and more generally, the issues faced by NEMS switches associated with stiction and reliability. The tip bump, which prevents the entire cantilever from contacting the surface, or the treatment of the surface in order to reduce the energy adhesion, are possible solutions to the stiction problem. However, moving components are inevitably prone to fracture or breakage, and reliability issues need to be further investigated.

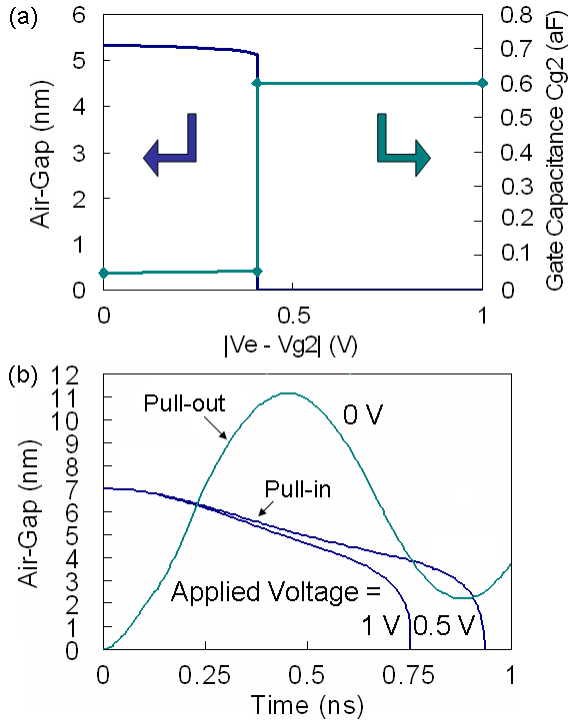

Fig. 5. (a) Static pull-in and corresponding gate capacitance. The displacement is defined at the cantilevers tip. Note that the initial air-gap is smaller than 7 nm because of the attractive Casimir force. (b) Dynamic pull-in and pull-out under standard atmospheric pressure.

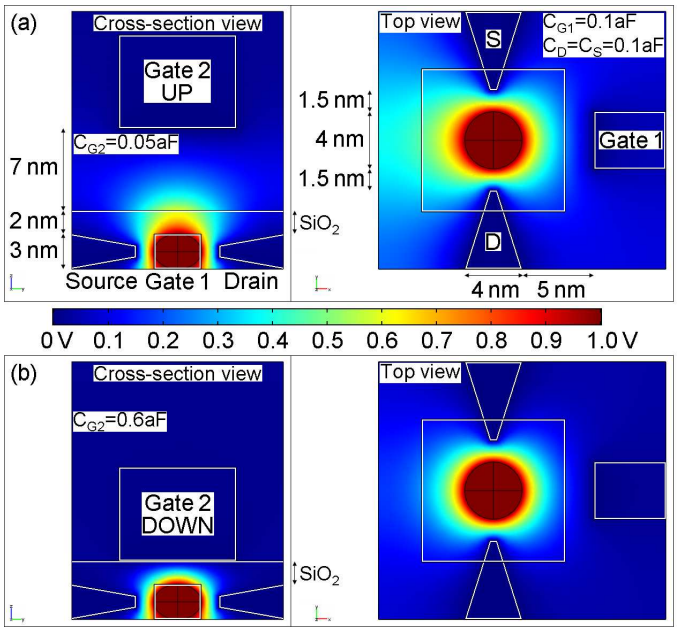

Fig. 6. Electric potential for a voltage difference of 1 V between the island and the electrodes, simulated with COMSOL [9]: (a) when the movable gate is pulled-out and (b) when the movable gate is pulled-in. The finite element simulation yields to the up and down movable gate, fixed gate, drain and source respective capacitances: C_{G2low}=0.05 aF, C_{G2high}=0.6aF, C_{G1}=C_D=C_S=0.1 aF.

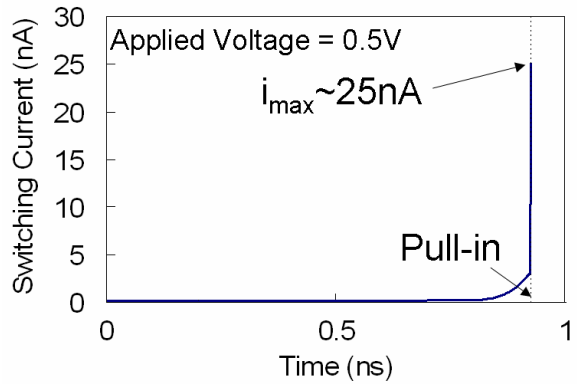

Fig. 7. Current $i = V\frac{dC_{gap}}{dt}$ charging the total gap capacitance C_{gap} during the switching process, for an applied voltage V = 0.5V.

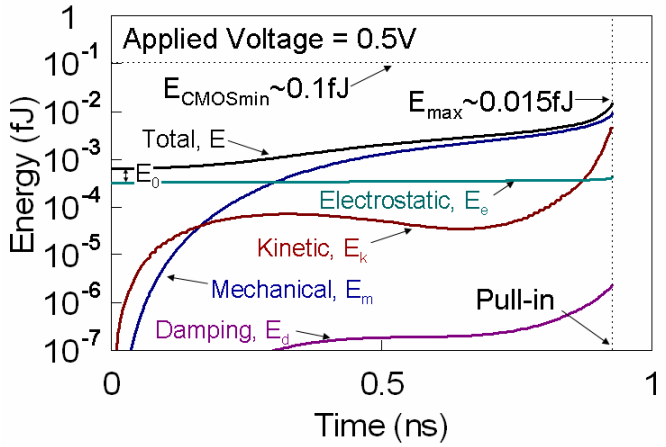

Fig. 8. Variation of the total energy and its components during the switching process.

III. Suspended-Gate SET Based Circuit Architectures

A. Suspended-Gate SET Building Block

1) Toward Background Charge Insensitive Devices: Random fluctuations of background charges are a serious problem faced by the single-electronic devices. To illustrate this effect, let us consider Fig. 10, which depicts a basic building block using the SG-SET. It comprises a bias current source I_S and an output capacitor C_L. We couple the analytical model [12] with a two-state tunable capacitor model corresponding to Fig. 5(a) (we assume no hysteresis) and embed them in professional simulator SmartSpice [13] to simulate its electrical characteristics. Although it is not taken into account in our simulation, the electrons tunnelling through the SET have a back action on the motion of the cantilever. When the SET is used to read out the motion of a nanomechanical resonator [14], [15], the oscillations that occur around the equilibrium position are critical for the precision of the measurement. However, in our case, the gate is not used as an oscillator but as a switch actuated via a third electrode, which is ideally independent from the island potential. The influence of tunneling electrons on the gate should be negligible at least in the pulled-in state since the gate remains attracted

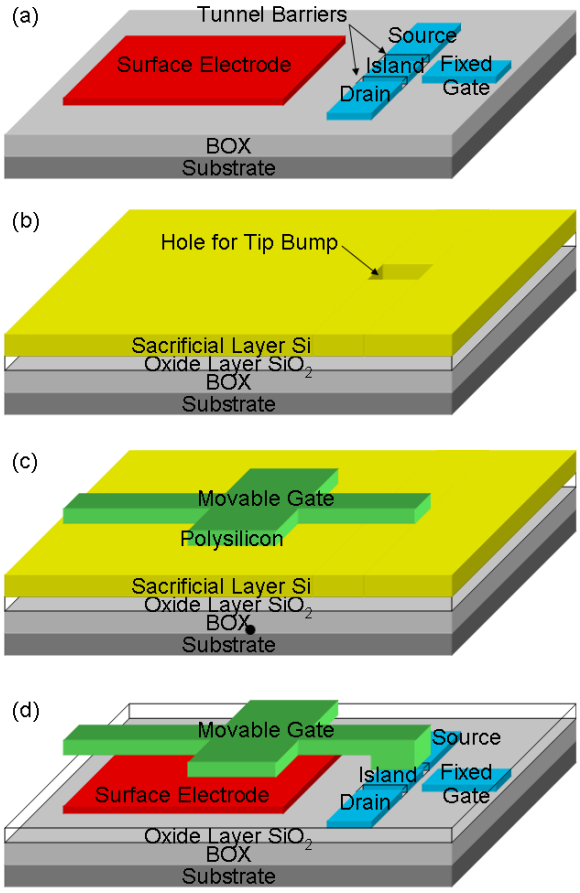

Fig. 9. (a)-(d) Possible fabrication process flow for the SG-SET.

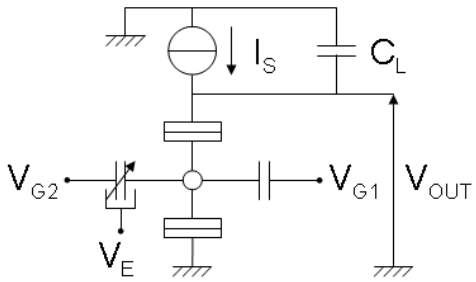

Fig. 10. Example of building block using the SG-SET. I_S denotes the bias current source and C_L the load capacitance.

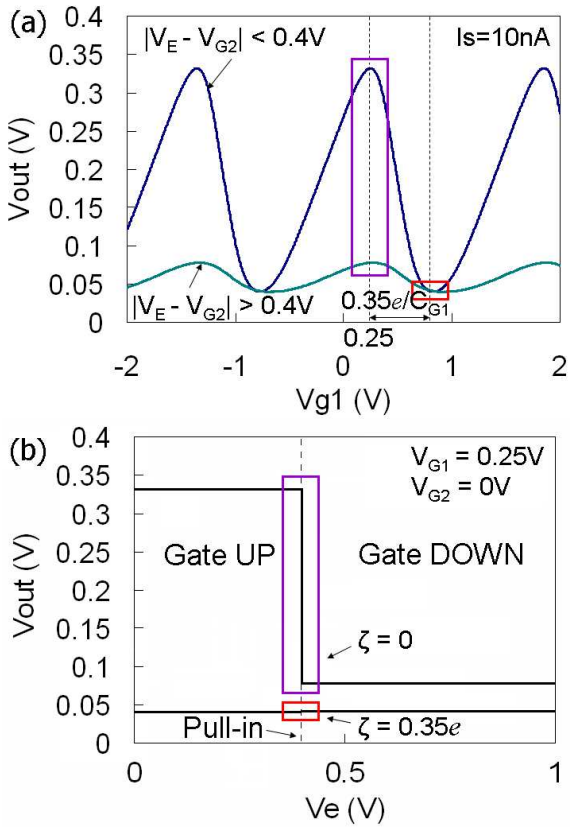

Fig. 11. Cell output voltage (a) as a function of the fixed gate voltage, for both movable gate positions; (b) as a function of the surface electrode voltage, for two values of background charge. Simulations are performed with the following parameters: T=300K, I_S=10nA, R_S=R_D=1MΩ, C_{G1}=C_D=C_S=0.1aF. C_{G2} is given by Fig. 5(a) and V_{PI} denotes the pull-in voltage.

to the substrate. When the gate is pulled-out, there may be slight oscillations around the equilibrium position due to the thermal bath formed by the electrons, but in view of the capacitance two-state profile, it should not have a critical effect for the considered logic applications. Nevertheless, interested readers may refer to [16] for detailed analysis of the dynamics of coupled SET-cantilever system. Simulations are performed with the following parameters: T=300K, I_S=10nA, R_S=R_D=1MΩ, C_{G1}=C_D=C_S=0.1aF, where R_S and R_D are respectively the source and drain resistances, and C_{G1}, C_D and C_S the first gate, drain and source capacitances. Figure 11(a) shows the output voltage V_{OUT} of the cell as a function of the fixed gate voltage V_{G1}, for both positions of the movable gate G_2. As expected, the amplitude of the oscillations may be tuned according to the gate position, that is according to the voltage V_E applied to the surface electrode. For instance, as it is shown on Fig. 11(b), for the bias V_{G1}=0.3V and V_{G2}=0V and assuming no background charge, the level of the output voltage V_{OUT} can be switched between two values by changing V_E. However, let us now assume that a background charge $0.35e$ (where e is the elementary charge) appears near the island. It induces in the oscillation a phase shift $\zeta = 0.35\frac{e}{C_{G1}}$ along the axis V_{G1} (Fig. 11(a)). As depicted on Fig. 11(b), the information is almost completely destroyed by the background charge. Because of this instability, single-electronic logic devices have heretofore been considered to be impractical.

A possible solution to circumvent these effects is to use the Coulomb oscillations to store and transmit logic states [4]. The amplitude or the periodicity, which remain unchanged even after the appearance of a charge, can indeed be used to code the information and sweeping the gate over several periods provides a simple way to get the necessary redundancy. For instance, Fig. 12 shows how an appropriate saw-tooth signal can be used as input gate voltage to output the Coulomb oscillations over several periods. Sweeping the first (fixed) gate enables to code the information into the amplitude, and the peak of the output signal may be obtained using a rectifier. In order to compare with Fig. 11, we assume that

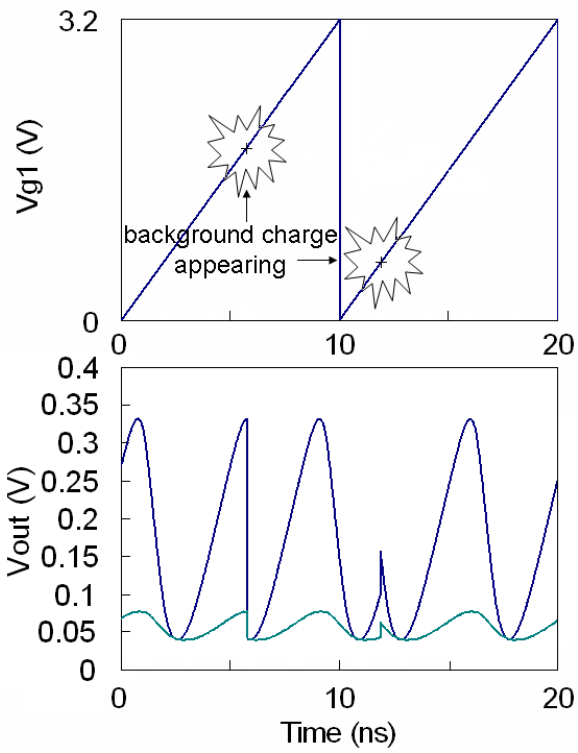

Fig. 12. Sweeping of the first (fixed) gate G_1 over several periods to get the redundancy in presence of dynamic background charge. The information can be extracted as long as one peak is reached during the measurement.

the same background charge $0.35e$ appears just at the peak of the signal, around 6 ns. As explained previously, this causes a phase shift of the output voltage to its minimum value. However, contrary to the direct encoding, this shift actually has no effect because the maximum voltage has been reached just before the background charge appeared. The background charge appearing around 12 ns is more problematic since it prevents the signal to reach its maximum. Nevertheless, as long as one peak is reached during the sweep in time, the information can be extracted. Note that sweeping the movable gate instead of the fixed one would result in coding the information into the periodicity and would require an extra filter to decode the frequency.

2) Speed and Power Consumption: Such information coding has to be slower than a direct coding into current or voltage levels, because one needs to sweep the input gate over several periods to determine a logic state. However, since the speed of quantum mechanical tunneling is a sub-picosecond process, the switching speed of the SG-SET will be much more limited by the gate movement ($\sim$ 1 ns). This limits the operation frequency of the SG-SET to the GHz range at best and makes the device a priori slower than current MOSFETs. However, this relative low-speed may be compensated by taking advantage of the SET multi-input abilities so that operations involving several inputs are performed with one single device.

One of the advantages of the SET, besides its nano feature size, is its ultra-low power consumption. For simplicity, we estimated the power dissipated in the cell by adding to the

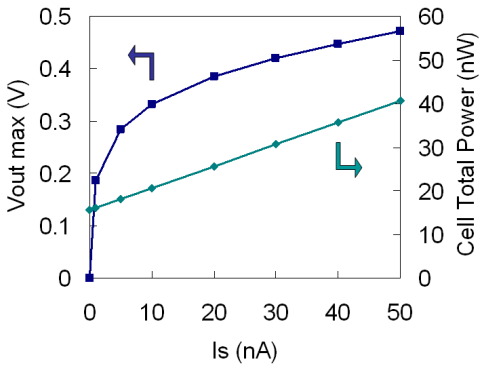

Fig. 13. Maximum output voltage and total power dissipation per cell (including NEMS and source resistor dissipations) as a function of the current source amplitude.

NEMS and source resistor dissipations the average current supplied by the bias source multiplied by the supply voltage (1V). As shown on Fig. 13, there is a trade-off between large fan-out and low power consumption. Assuming the average power dissipated in the network is 20 nW/cell, a processor with 30 million units would dissipate around 600 mW. In comparison, a 1 Ghz, 0.18-μm CMOS processor that contains an equivalent number of transistors dissipates 30 W on average for a 1.7 V power supply.

B. Cellular Non-linear Network (CNN)

The cellular non-linear network (CNN) [17] is a parallel computer network capable of exceptional speed and power, having promising applications in associative memory and image processing. Whereas a basic cell of a CNN requires a large number of linear resistors, capacitors, and non-linear sources in its usual implementation in MOS IC technology, the non-linearity provided by the suspended-gate enables to realize it with a single device. A possible implementation of a SG-SET based neuron is depicted on Fig. 14. The rectifier outputs the maximum of its input voltage so that the cell is insensitive to background charge. The inputs summation, which determines the functionality of the CNN, can simply be made via capacitive synapse so that the voltage V_E applied to the surface electrode is the sum of input voltages V_i weigthed with the capacitances C_i:

$$V_E = \frac{\sum_i C_i V_i}{\sum_i C_i} \tag{1}$$

Simulated results for different input conditions of a three inputs neuron cell are shown on Fig. 15. Figure 16 shows that the threshold may also be purposely tuned by choosing the bias V_{G2}.

Such cells are directly cascadable to build the networks described in [18], on condition one chooses the right capacitive template and interconnection scheme. The low fan-out remains however a problem that can be solved by combining the SET with CMOS [5].

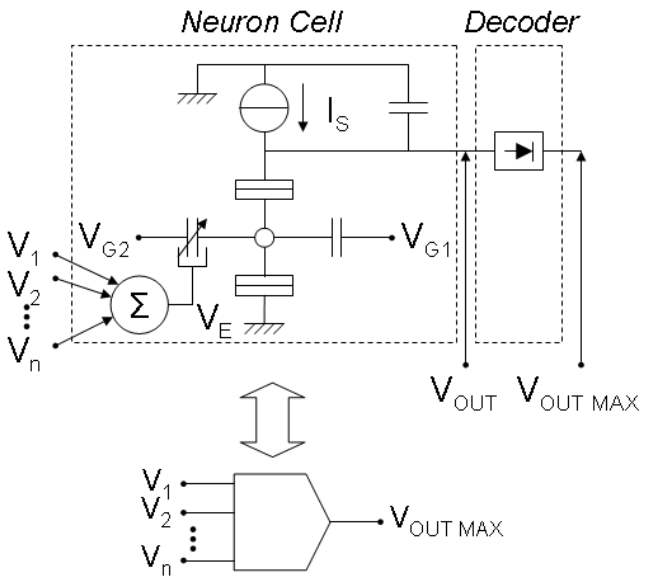

Fig. 14. Schematic structure of a SG-SET based neuron cell for application in CNN circuits.

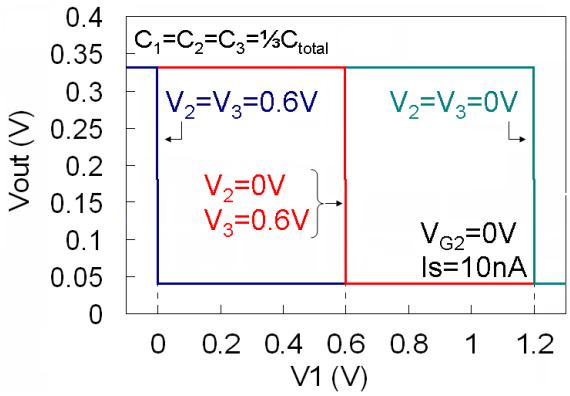

Fig. 15. Maximum output voltage of a three inputs neuron cell as a function of the first input gate voltage, for different values of the second and third input voltages. C_{total} denotes the sum of the input capacitances. All the inputs have the same capacitive weight and the decision is made according to the inputs level.

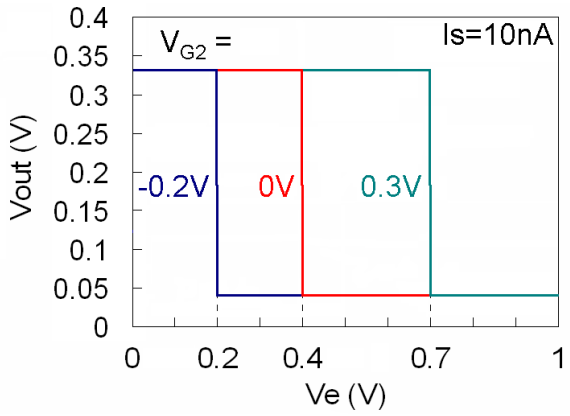

Fig. 16. Maximum output voltage of a cell as a function of the surface electrode voltage, for different biases of the second gate. The second gate may therefore be used to tune the threshold voltage.

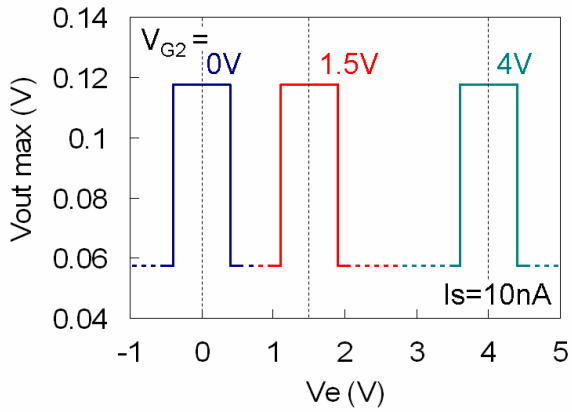

Fig. 17. Maximum output voltage of a cell as a function of the surface electrode voltage, for different biases of the second gate. The oscillation amplitude is maximum if V_E is close enough to V_{G2}.

C. Pattern Matching

As we saw previously, the maximum of the output voltage is obtained when the gate is up, that is when the absolute value of the difference between the movable gate voltage V_{G2} and the surface electrode voltage V_E is zero. In other words, the output voltage is maximum if V_E is close enough to V_{G2} (Fig. 17). Therefore, the SG-SET can be used to build compact associative processors for pattern matching, where the pair input/template would consist of these two voltages. For comparison, a basic CMOS implementation of such distance calculation requires 16 transistors to compute the corresponding subtraction and the absolute value [19]. Moreover, assuming that n pairs can be implemented on the same device, a single SG-SET device would be able to perform the job of an equivalent CMOS implementation of $16n$ transistors.

For example, let us consider a triple-SG-SET, having three movable gates as depicted on Fig. 18. Its output voltage is inversely proportional to the number of gates pulled-in (Fig. 19), that is proportional to the closeness of the input (movable gates) with the template data (surface electrodes), so that a maximum is obtained when the two match. Now, by assigning each gate to one RGB component and assuming a preliminary colors encoding, it becomes possible to identify the color combination of red, green and blue in a set of encoded colors. Regarding this encoding, let us consider the "web-safe" 216 colors palette. This palette allows exactly six shades each of red, green, and blue ($6 \times 6 \times 6 = 216$). Therefore, by coding each these six possible shades into a voltage between 0V and 5V, one can attribute to each one of the 216 colors a unique set of three voltages (V_R, V_G, V_B) (Fig. 20(a)).

Let us now suppose an associative processor composed of 216 devices. The 216 possible template sets (V_{Rt}, V_{Gt}, V_{Bt}) are respectively applied to the gates of the devices, so that each device becomes able to solely identify the color corresponding to its applied template. Let us assume we need to identify an orange pixel. The "orange color" being defined by the set (5V,3V,0V), these voltages are respectively applied to the three surface electrodes of each device. Since one device's output is maximum when the input (V_{Ri}, V_{Gi}, V_{Bi}) is equal to the

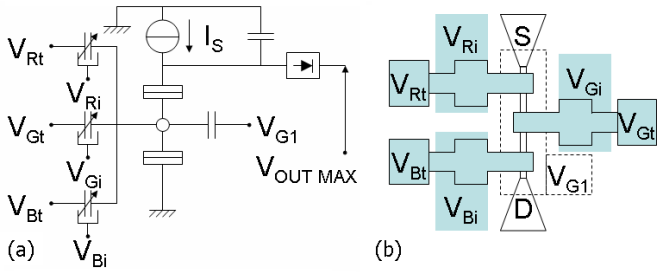

Fig. 18. (a) Schematics and (b) possible layout for the triple-SG-SET.

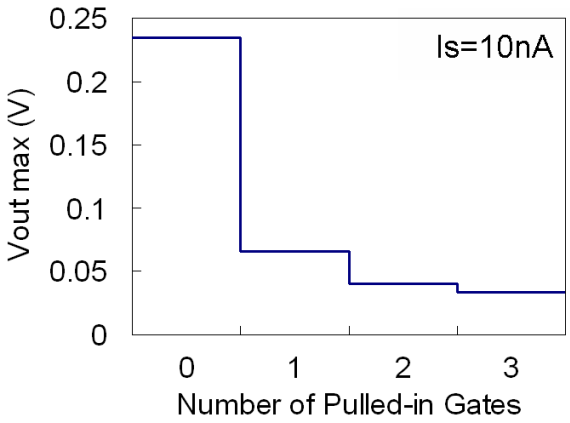

Fig. 19. Output voltage of the triple-SG-SET as a function of the number of pulled-in gates.

applied template (V_{Rt}, V_{Gt}, V_{Bt}), the output voltage of the device corresponding to the orange template is the highest, and the orange color can be identified (Fig. 20(b)).

A similar concept based on single-hole transistors has been proposed and demonstrated in [20], where the bell-shape of the Coulomb oscillation is used to perform *analog* pattern matching. Because of the abrupt non-linear characteristics of the SG-SET, the matching resolution is in our case limited to 0.8 V ($2\times V_{PI}$) at best and only *digital* matching is possible. However, one advantage of the present device compared to [20] is its ability to calculate the distance of several elements (three in this case) at the same time on the same device, so that gain in terms of area may be expected. Another benefit is that it does not require any preliminary and individual adjustment of the peak position or any data storage since it is simply and dynamically controlled via the voltages applied to the switch electrodes.

IV. Conclusion

A comprehensive study of the suspended-gate SET performances was conducted through simulation. The movable gate design was optimized so that low actuation voltage (0.4 V) and nanosecond delay can be simulated. The expected pull-in energy is therefore drastically reduced to 0.015 fJ. The electrical characteristics of the optimized device were embedded in a SPICE simulator and it was shown through simulation that this device enables to evade the problem of the background charge inherent to the SET thanks to a different information encoding. New circuit architectures, such

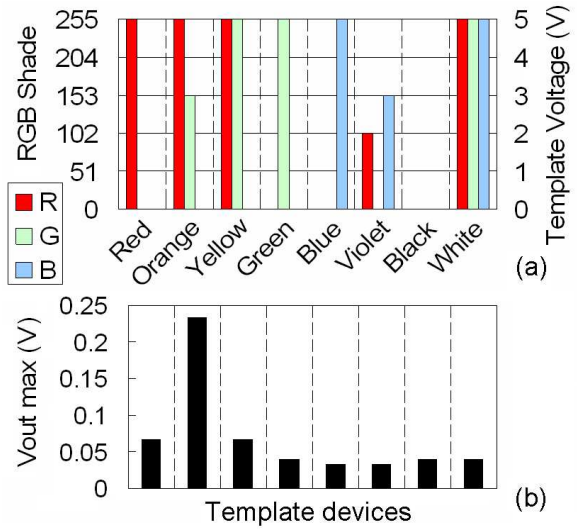

Fig. 20. (a) Encoding of some of the "web-safe" colors into sets of three voltages (V_R, V_G, V_B). (b) Identification of the orange color by the corresponding template devices: (V_{Ri}, V_{Gi}, V_{Bi}) = (V_{Rt}, V_{Gt}, V_{Bt}) = (5V, 3V, 0V)

as cellular non-linear network and pattern matching, were also proposed and simulated.

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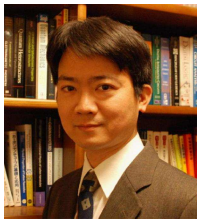

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