HSPICE implementation of a numerically efficient model of CNT transistor

Tom J Kazmierski, Dafeng Zhou and Bashir M Al-Hashimi
School of Electronics and Computer Science, University of Southampton, Southampton, SO17 1BJ, UK
dz05r,tjk,bmah@ecs.soton.ac.uk

***Abstract*—This paper presents the algorithms of an implementation of a numerically efficient carbon nanotube transistor (CNT) model in HSPICE. The model is derived from cubic spline non-linear approximation of the non-equilibrium mobile charge density. The spline algorithm exploits a rapid and accurate solution of the numerical relationship between the charge density and the self-consistent voltage, which results in the acceleration of deriving the current through the channel without losing much accuracy. The output I-V characteristics of the proposed model have been compared with those of a recent HSPICE implementation of the Stanford CNT model and published experimental I-V curves. The results show superior accuracy of the proposed model while maintaining similar CPU time performance. Two versions of the HSPICE macromodel implementation have been developed and validated, one to reflect ballistic transport only and another with non-ballistic effects. To further validate the model a complementary logic inverter has also been implemented using the proposed technique and simulated in HSPICE.**

I. Introduction

Transistors using carbon nanotubes (CNTs) have shown the potential of becoming the basis of next generation integrated circuits (ICs) [1], [2]. A number of theoretical models have been proposed to describe the different physical phenomena within the nanotube channel and their effect on the performance of the device [3], [4], [5], [6], [7], [8]. The standard modelling methodology relies on repetitive numerical evaluation of the Fermi-Dirac integral to obtain the drain-source current for a given set of terminal potential. Recently improved approaches have been proposed where the slow iterative process is replaced by direct calculations using numerically efficient approximations while still maintaining good accuracy compared with the basic theory [6], [9]. These new techniques rely on piece-wise approximation of charge densities, either linear [6] or non-linear [9] to simplify the numerical calculation. The improved models have been implemented and tested in MATLAB and VHDL-AMS [10]. Here we propose a more practical implementation using the HSPICE macromodelling language [11]. The model has been validated using sample transistor circuits and logic gates and demonstrated to compare favourably in terms of accuracy with the recently released Stanford HSPICE CNT model. The HSPICE model proposed here has been demonstrated to have the potential of including non-ballistic effects in the evaluation of the drain current.

II. Calculation of the self-consistent voltage

When voltages are applied to the drain and the source of a CNT transistor as illustrated in figure 1, a non-equilibrium mobile charge is generated in the carbon nanotube channel, which can be described in 1as follows[1], [12], [13]:

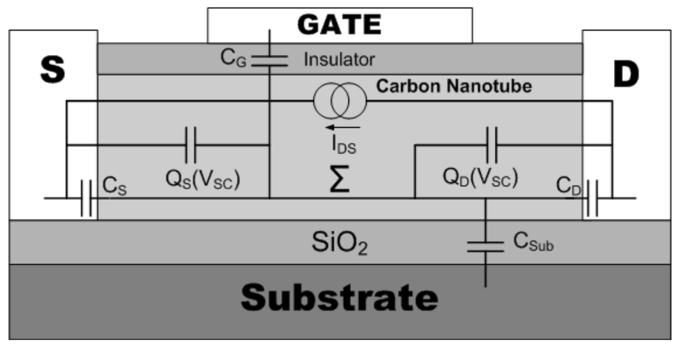

Fig. 1. Structure layout of a top-gate CNT transistor showing components of the proposed equivalent circuit model with the virtual node for V_{SC}.

$$\Delta Q = q(N_S + N_D - N_0) \quad (1)$$

where N_S is the density positive velocity states filled by the source, N_D is the density of negative velocity states filled by the drain and N_0 is the equilibrium electron density. These densities are determined by the Fermi-Dirac probability distribution:

$$N_S = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E-U_{SF})dE \quad (2)$$

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E-U_{DF})dE \quad (3)$$

$$N_0 = \int_{-\infty}^{+\infty} D(E)f(E-E_F)dE \quad (4)$$

where $D(E)$ is the density of states, f is the Fermi probability distribution, E represents the energy levels per nanotube unit length, and U_{SF} and U_{DF} are introduced as

$$U_{SF} = E_F - qV_{SC} \quad (5)$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS} \quad (6)$$

where E_F is the Fermi level, q is the electronic charge and V_{SC} represents the self-consistent voltage [1] whose presence in these equations illustrates that the CNT energy band is affected by external terminal voltages. The self-consistent voltage V_{SC} is determined by the device terminal voltages and charges at terminal capacitances by the following non-linear algebraic equation [1], [6]:

$$V_{SC} = -\frac{Q_t + qN_S(V_{SC}) + qN_D(V_{SC}) + qN_0}{C_\Sigma} \quad (7)$$

where Q_t represents the charge stored in terminal capacitances and is defined as

$$Q_t = V_G C_G + V_D C_D + V_S C_S + V_{Sub} C_{Sub} \quad (8)$$

where C_G, C_D, C_S, C_{Sub} are the gate, drain, source and substrate capacitances correspondingly and the total terminal capacitance C_Σ is

$$C_\Sigma = C_G + C_D + C_S + C_{Sub} \quad (9)$$

$$C_{ox} = 2\pi k_1 \varepsilon_0 / ln(\frac{2t_{ox} + d}{d}) \quad (10)$$

$$C_{Sub} = 2\pi k_2 \varepsilon_0 / ln(4H_{Sub}/d) \quad (11)$$

where d is the diameter of the carbon nanotube, H_{Sub} is the thickness of the SiO_2 layer on the substrate, t_{ox} is the thickness of the gate insulator and k_1, k_2 are the relative permittivities of the gate and the substrate respectively [14]. Meanwhile, the capacitances between terminals can be obtained as follows as reported previously [15].

$$C_G = C_{ox} \quad (12)$$

$$C_S = 0.097 C_{ox} \quad (13)$$

$$C_D = 0.040 C_{ox} \quad (14)$$

According to the ballistic CNT ballistic transport theory [1], [15] the drain current caused by the transport of the non-equilibrium charge across the nanotube can be calculated using the Fermi-Dirac statistics as follows:

$$I_{DS_0} = \frac{2qkT}{\pi\hbar}\left[\mathcal{F}_0(\frac{U_{SF}}{kT}) - \mathcal{F}_0(\frac{U_{DF}}{kT})\right] \quad (15)$$

where $\mathcal{F}_0$ represents the Fermi-Dirac integral of order 0, k is Boltzmann's constant, T is the temperature and $\hbar$ is reduced Planck's constant.

The numerical efficiency of the ballistic CNT transport model presented above hinges on an efficient calculation of the non-equilibrium mobile charge. Piecewise approximation of the mobile charge based on cubic splines significantly accelerates calculations without losing much accuracy [9]. The mobile charge can be presented as a function of a single variable, the self-consistent voltage V_{SC}:

$$Q(V_{SC}) = \frac{q}{2}\int_{-\infty}^{+\infty} D(E) f(E - E_F - V_{SC}) dE \quad (16)$$

Hence, a simple spline structure, using n equally spaced points, can easily be constructed approximate the mobile charge dependence on V_{SC}. If cubic splines are used the individual polynomial pieces have the following form

$$Q(V_{SC}) = a_i V_{SC}^3 + b_i V_{SC}^2 + c_i V_{SC} + d_i \quad (17)$$

where a_i, b_i, c_i and d_i, $i = 1, \ldots, n-1$ are spline coefficients. This enables a closed-form solution of the self-consistent voltage equation (7) as, for each piece, it now becomes a a polynomial equation of the third order. Thus, the need for costly Newton-Raphson iterations and evaluations of Fermi-Dirac integrals is eliminated. Once the self-consistent voltage V_{SC} is efficiently calculated from the closed-form solutions of equation (7), the total drain current can be directly obtained from equations (5), (6) and (15).

Figure 2 shows I_{DS} characteristics obtained from a MATLAB simulation, where an example model that uses three cubic splines, $n = 4$, and two linear pieces at the ends was compared with the theoretical curves calculated by FETToy from equations (3) and (4) correspondingly.

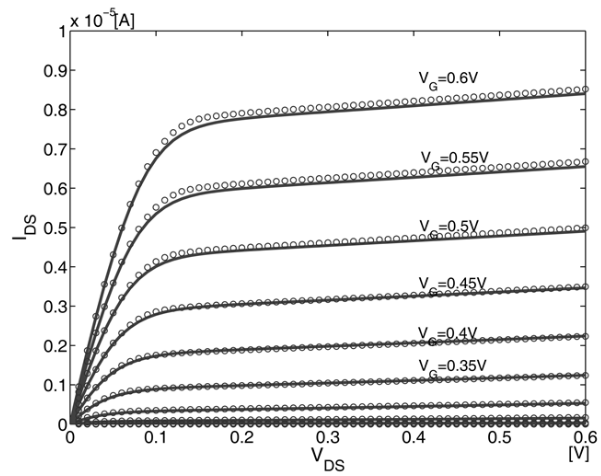

Fig. 2. Drain current characteristics at $T = 300K$ and $E_F = -0.32eV$ for FETToy(solid lines) and 3 pieces cubic spline approximation (dashed lines).

To solve the resulting 3rd order polynomial equations, Cardano's method [16] is applied to determine the appropriate root which represents the correct value of V_{SC}. Since the self-consistent voltage V_{SC} is directly obtained from the spline model, the evaluation of the drain current poses no numerical difficulty as energy levels U_{SF}, U_{DF} can be found quickly from equations (5), (6) and I_{DS} can be calculated using equation (15).

III. HSPICE MACROMODEL IMPLEMENTATION

Having implemented the spline-based numerical model in MATLAB, HSPICE macromodels of an n-type-like and p-type-like CNT transistor have been developed. Figure 3 shows the I_{DS} characteristics of the n-type-like transistor implemented in HSPICE compared with the output current of a recently reported CNT transistor SPICE model from Stanford University [17], [18]. DC sweep simulations were carried out with the gate voltage of $0V$ to $0.6V$ with $0.1V$ step and drain-source voltage $0V$ to $0.6V$ with $0.01V$ step. Both models implement near-ballistic transport. Discrepancies in the I_{DS} current values can be explained by the fact that the Stanford model considers subband effects which reduce the current [17], [18].

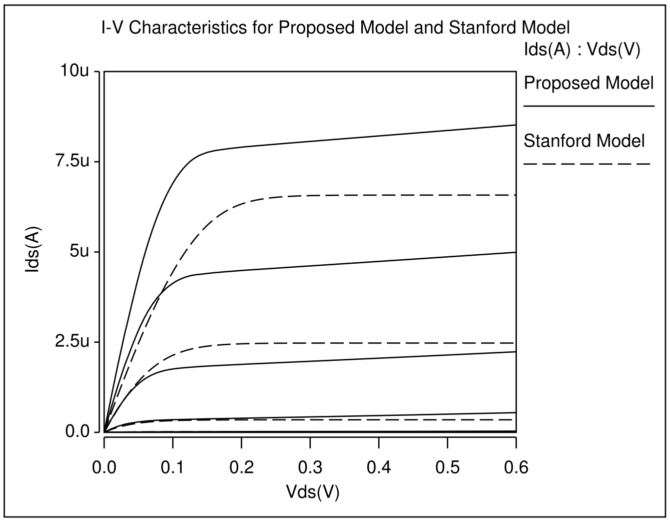

Fig. 3. Comparison of Drain current characteristics at $T = 300K$ and $E_F = -0.32eV$ for the proposed HSPICE macromodel and the Stanford circuit-level model [17], [18].

The spline model has the potential to include arbitrary non-ballistic effects in and therefore can be used to predict the performance of non-ideal CNT transistors. Figure 4 shows the I_{DS} characteristics of the n-type-like CNT transistor implemented in HSPICE with the elastic scattering effect [18] and the strain effect on the channel region [19]. Neither of these effects is included in the Stanford model. The strain effect can change the band gap of the CNT channel and thus reduce the drain current, which matches the output results of the model. It can be seen from the graphs in Figure 4 that the proposed HSPICE model matches more closely the experimental results presented in Figure 5, especially in terms of the saturation region region slope, than the Stanford model.

Additionally, to verify the accuracy of the proposed macromodel, recently reported experimental characteristics [20] were compared with the spline-based model for $d = 1.6nm, t_{ox} = 50nm, T = 300K$ and $E_F = -0.05eV$ and presented in Figure 5. It also shows the performance of the Stanford model under the same conditions. The results show a close match between the proposed cubic spline macromodel and experimental measurements, which is more accurate than the Stanford model while maintaining similar speed as shown in Table I.

A corresponding p-type-like CNT transistor has also been implemented in HSPICE and Figure 6 illustrates the corresponding I_{DS} characteristics. Both n-type-like and p-type-like models were used in an analysis of a complementary CMOS-like CNT inverter. The bulk voltage has also considered to take into account the effects on the charge densities generated by the substrate voltage, which is important to reflect correctly the behaviour of p-type-like CNT transistor.

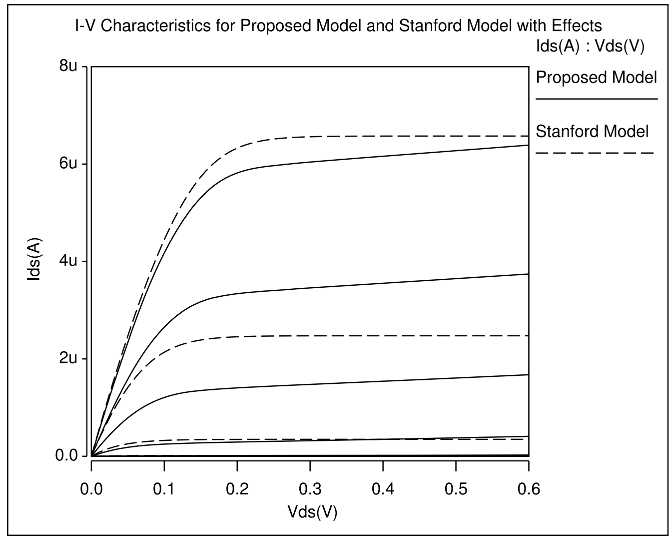

Fig. 4. Drain current characteristics at $T = 300K$ and $E_F = -0.32eV$ for the proposed HSPICE macromodel with the strain effect [19].

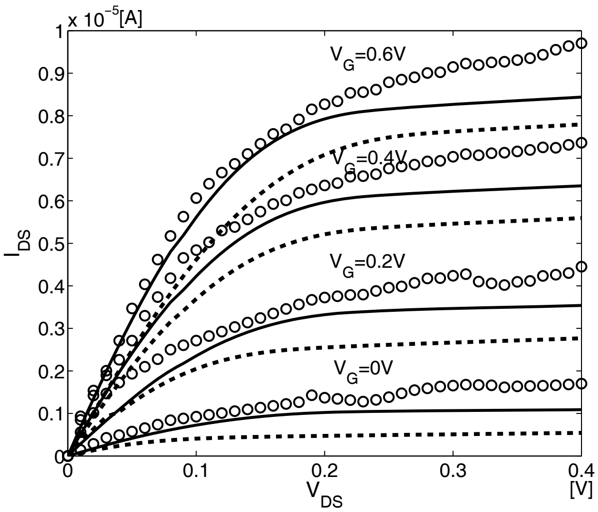

Fig. 5. Comparison to the experimental results(circlet lines) of the proposed cubic spline model with $n = 4$ (solid lines) and Stanford model (dashed lines) for $d = 1.6nm, t_{ox} = 50nm, T = 300K$ and $E_F = -0.05eV$.

The HSPICE simulation results of the complementary inverter are shown in figure 7. The figure shows the transfer characteristic calculated by using a ramp voltage as the input signal.

The HSPICE macromodel code for the parameter library and transistor macromodel is shown below.

TABLE I

AVERAGE RMS ERRORS AND CPU TIME IN I_{DS} COMPARISON TO THE EXPERIMENTAL RESULTS OF FETTOY MODEL AND THE PROPOSED NON-BALLISTIC (NB) MODELS FOR $d = 1.6nm, t_{ox} = 50nm, T = 300K$ AND $E_F = -0.05eV$.

$V_G[V]$	**Proposed Macromodel $n = 4$**	**Stanford Model**
0.2	13.3%	35.7%
0.4	12.5%	29.6%
0.6	11.3%	25.2%
CPU Time[s]	40.32	47.60

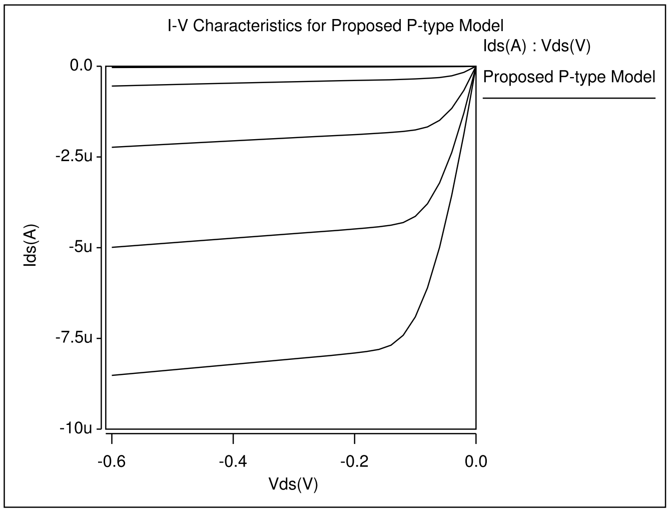

Fig. 6. Drain current characteristics for a p-type CNT transistor HSPICE macromodel.

```
*   Library name: param.lib

**************************************************
* Global parameters
**************************************************

.PROTECT

.PARAM q=1.60e-19   $ Electronic charge
+ Vcc='3.0*q'       $ The carbon PI-PI bond energy
+ acc=0.142e-9      $ The carbon PI-PI bond distance
+ a=0.2495e-9       $ The carbon atom distance
+ pi=3.1415926      $ PI, constant
+ h=6.625e-34       $ Planck constant
+ h_ba=1.0552e-34   $ h_bar
+ KB=1.380e-23      $ Boltzmann constant
+ epsr=8.854e-12    $ Dielectric constant in vacuum
+ k=3.9             $ Relative dielectric constant
+ t0=1.5e-9         $ The gate dioxide thickness
+ L=3.0e-8          $ Length of the cnt
+ N0=1.1431e3       $ Flat band mobile charge density
+ Cso=0.097         $ Source capacitance coefficient
+ Cdo=0.040         $ Drain capacitance coefficient
+ Ef=-0.32          $ Fermi level
+ dcnt=1e-9         $ Diameter of CNT
+ T=300             $ Temperature
+ lambda_op=15e-9
$ The Optical Phonon backscattering mean-free-path
+ lambda_ap=500e-9
$ The Acoustic Phonon backscattering mean-free-path

.UNPROTECT


**************************************************
```

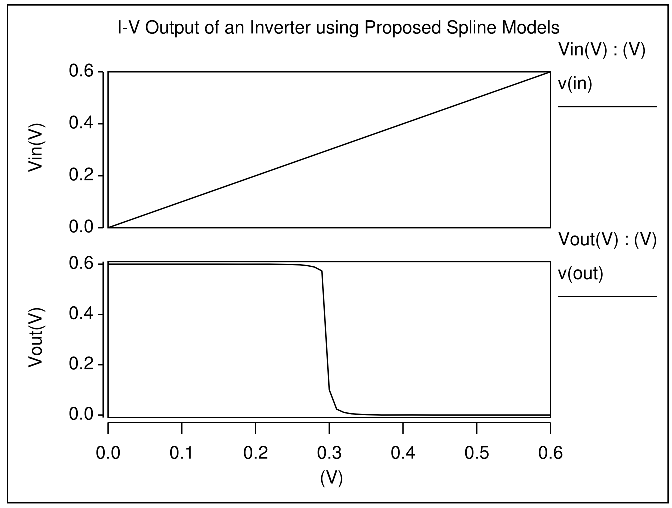

Fig. 7. Inverter simulation result in HSPICE; input ramps from $0V$ to $0.6V$.

```
* CNT transistor model using 4-piece cubic spline
*
* File name: cntmodel.sp
**************************************************

* Library file CNmodel.lib provides the spline coefficients
* and the sub-circuit description of the proposed macromodel,
* which sets the node of the device and calculate the current
* of the model.

.TITLE 'IV Characteristics for CNT Transistor'

.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
*.options GSHUNT=1e-20 RMIN=1e-20
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13

.param   TEMP=27

.lib 'CSmodel.lib' CSmodel

**************************************************
*Beginning of circuit and device definitions

*Supplies and voltage params:
.param Supply=0.6
.param Vg='Supply'
.param Vd='Supply'

*Some CNFET parameters:
.param t0=1.5e-9
.param L=3.0e-8
.param Ef=-0.32
.param dcnt=1e-9

**************************************************
* Define power supply

Vdd     Drain    Gnd     Vd
Vss     Source   Gnd     0
Vgg     Gate     Gnd     Vg
Vsub    Sub      Gnd     0

**************************************************
* Main Circuits

* nFET
CNT Drain Gate Source Sub nCNT Lch=L  Efi=Ef  dia=dcnt  Tox=t0

**************************************************
* Measurements
```

```
* test nFETs, Ids vs. Vgs
.DC      Vdd   START=0     STOP='Supply'   STEP='0.01'
+ SWEEP  Vgg   START=0     STOP='Supply'   STEP='0.1'

**************************************************

.print I(Vdd)

.end
```

The complete code for the proposed HSPICE model is now available on the Southampton Carbon Nanotube Transistor Modelling website [21] and available for public use.

IV. Conclusion

This paper proposes an HSPICE implementation of the cubic spline based numerically efficient CNT transistor model. HSPICE simulation results match closely those from MATLAB simulations and also recently published experimental measurements. Results show that the accuracy of the proposed HSPICE implementation is superior to that of the state-of-the-art CNT SPICE model developed at Stanford University, while maintaining similar simulation speed. The accuracy of the proposed model can be further increased by inclusion of other physical effects, specifically non-ballistic transport. To demonstrate the feasibility of adding non-ballistic effects, a version of the model has been developed and implemented in HSPICE to include elastic scattering and the strain effect.

V. Acknowledgement

This project has been funded in part by the EPSRC (UK) grant EP/E035965/1.

References

[1] Anisur Rahman, Jing Guo, Supriyo Datta, and Mark S. Lundstrom. Theory of ballistic nanotransistors. *Electron Devices, IEEE*, 50(9):1853–1864, September 2003.

[2] Phaedon Avouris, Joerg Appenzeller, Richard Martel, and Shalom J. Wind. Carbon nanotube electronics. *Proceedings of the IEEE*, 91(11):1772–84, November 2003.

[3] Arash Hazeghi, Tejas Krishnamohan, and H.-S. Philip Wong. Schottky-Barrier Carbon Nanotube Field-Effect Transistor Modeling. In *Sixth IEEE Conference on Electron Devices*, volume 54, Lausanne, Switzerland, March 2007.

[4] Thao Dang, Lorena Anghel, and Regis Leveugle. Cntfet basics and simulation. In *IEEE Int. conf. on Design and Test of Integrated Systems in Nanoscale Technology (DTIS)*, Tunis, Tunisia, 5-7 September 2006.

[5] Chris Dwyer, Moky Cheung, and Daniel J. Sorin. Semi-empirical SPICE models for carbon nanotube FET logic. In *4th IEEE Conference on Nanotechnology*, Munich, Germany, 16-19 Aug. 2004.

[6] Hamidreza Hashempour and Fabrizio Lombardi. An efficient and symbolic model for charge densities in ballistic carbon nanotube FETs. *IEEE-NANO*, 1:17–20, June 2006.

[7] Bipul C. Paul, Shinobu Fujita, Masaki Okajima, and Thomas Lee. Modeling and analysis of circuit performance of ballistic CNFET. In *2006 Design Automation Conference*, San Francisco, CA, USA, 24-28 July 2006.

[8] A. Raychowdhury, S. Mukhopadhyay, and K. Roy. A circuit-compatible model of ballistic carbon nanotube field-effect transistors. *Applied Physics Letters*, 23(10):1411–20, October 2004.

[9] Tom J. Kazmierski, Dafeng Zhou, Bashir M. Al-Hashimi, and Peter Ashburn. Numerically efficient modeling of cnt transistors with ballistic and non-ballistic effects for circuit simulation. *IEEE Transactions on Nanotechnology*, 8, March 2009.

[10] Dafeng Zhou, Tom J. Kazmierski, and Bashir M. Al-Hashimi. VHDL-AMS implementation of a numerical ballistic CNT model for logic circuit simulation. In *Specification, Verification and Design Languages, 2008. FDL 2008. Forum on*, Stuttgart, Germany, 23-25 September 2008.

[11] Synopsys. Cadence openbook se 5.3, ic 4.4.5 and lvd 3.0, 2005. http://www.cadence.com.

[12] Ming-Hsun Yang, Kenneth B. K. Teo, Laurent Gangloff, William I. Milne, David G. Hasko, Yves Robert, and Pierre Legagneux. Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors. *Applied Physics Letters*, 88(11):113507–1–3, March 2006.

[13] Paul L. McEuen, Michael S. Fuhrer, and Hongkun Park. Single-walled carbon nanotube electronics. *Nanotechnology, IEEE Transactions*, 1(1):78–845, March 2002.

[14] Jie Deng and H.-S.Philip Wong. Modeling and analysis of planar-gate electrostatic capacitance of 1-d fet with multiple cylindrical conducting channels. *IEEE Transactions on Electron Devices*, 54:2377–2385, September 2007.

[15] Anisur Rahman, Jing Wang, Jing Guo, Sayed Hasan, Yang Liu, Akira Matsudaira, Shaikh S. Ahmed, Supriyo Datta, and Mark Lundstrom. Fettoy 2.0 - on line tool, 14 February 2006. https://www.nanohub.org/resources/220/.

[16] Ulrich K Deiters. Calculation of densities from cubic equations of state. *AIChE Journal*, 48(4):882–886, April 2002.

[17] Jie Deng and H.-S.Philip Wong. A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its application - part i: model of the intrinsic channel region. *IEEE Transactions on Electron Devices*, 54:3186–3194, December 2007.

[18] Jie Deng and H.-S.Philip Wong. A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its application - part ii: full device model and circuit performance benchmarking. *IEEE Transactions on Electron Devices*, 54:3195–3205, December 2007.

[19] E. D. Minot, Yuval Yaish, Vera Sazonova, Ji-Yong Park, Markus Brink, and Paul L. McEuen. Tuning carbon nanotube band gaps with strain. *Physical Review Letters*, 90(15):156401/1–4, April 2003.

[20] Ali Javey, Ryan Tu, Damon Farmer, Jing Guo, Roy Gordon, and Hongjie Dail. High performance n-type carbon nanotube field-effect transistors with chemically doped contacts. *Nano Letters*, 5:345–348, February 2005.

[21] Dafeng Zhou, Tom J Kazmierski, Bashir M Al-Hashimi, and Peter Ashburn. Southampton CNT resources, 6 August 2008. https://www.cnt.ecs.soton.ac.uk.