

Effect of Variability in SWCNT-Based Logic Gates

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Abstract—This work is concerned with Carbon Nanotube diameter variations and the resulting uncertainties on the behavior of logic gates made from Single Walled Carbon Nanotubes (SWCNTs). Monte Carlo simulations were performed for logic gates based on CNTs of different mean diameters using the Stanford CNFET model. Delay characteristics of logic gates (NOT, NAND, NOR) are studied. This work reveals that logic gates employing SWCNTs with mean diameters greater than about 1.2 nm, show less variation in their timing characteristics, provided that a CNT diameter standard deviation of less than 0.1nm can be guaranteed by a technology process.

Index Terms—Single Walled Carbon Nanotube (SWCNT), Carbon Nanotube Field Effect Transistor (CNFET), Design Variability

I. INTRODUCTION

With the continuous trend of reducing feature sizes, and employing continuously smaller components on integrated circuits, new challenges arise on the way of silicon CMOS circuits and devices [1]. Researchers have turned to new and novel devices to keep this trend of downscaling going. Emerging “nanodevices” promise increased integration density and reduced power consumption for future electronics. The Carbon NanoTube (CNT) is one such device, becoming the focus of much research in recent years [2]. These emerging and new devices, partially due to their extremely small dimensions, show large variations in their behaviour, governed by quantum physics [1], resulting in unpredictability and unreliability in circuits made from them.

The present work is concerned with a study of the effects of diameter variation on delay characteristics of SWCNT-based logic gates. This work is a step towards the process of designing reliable CNT-based logic circuits. To the best of our knowledge, this is the first study of SWCNT-based logic gate timing characteristics with respect to CNT diameter variation and the first such design rule being put forward towards the implementation of CNT-based logic gates and circuits.

II. CNFET STRUCTURE

Geometrical properties of a CNT, i.e. its diameter and chiral angle have a direct effect on the CNT’s energy band gap which in turn affects its current voltage characteristics. A random distribution of CNT chiral angles produces roughly 2/3 semiconducting and 1/3 metallic CNTs [3] with a significant diameter variation around a mean diameter. Recent CNT growth techniques can achieve as high as 96% semi-conducting CNTs [18]. This work assumes only semiconducting CNTs are

used in the design of a CNFET. Diameter variation in manufactured CNTs affects the electrical properties of the transistors, and hence logic gates made from them in terms of delay and power consumption. It has been proven that at low operating voltages, the effect of chirality variation on device electrostatics is negligible [4]; hence, in this study we concentrate only on the effects of CNT diameter variation on logic gates characteristics. The most commonly used statistical CNT diameter models adopt Gaussian distribution [5, 6].

Two alternative CNFET configurations are prominent; Schottky Barrier (SB) FET [7] or MOSFET-like FETs [8, 9]. SB-CNFETs show ambipolar behavior [10] which is undesirable as far as complementary logic design goes [10]. MOSFET-like CNFETs exhibit unipolar behavior and as far as fabrication is concerned they are easier to make.

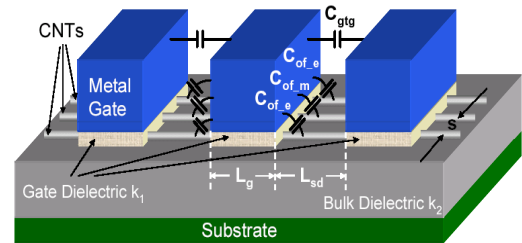


Figure 1. CNFET with multiple CNTs [12]

For this work we have used a CNFET model developed by Stanford [13]. The model implements a circuit-compatible compact model for CMOS-like single-walled CNFETs and is implemented in HSPICE. It is superior to previous compact models as it accounts for scattering in the channel region, the resistive source/drain, the Schottky barrier resistance and the parasitic gate capacitances. Also by adding a full trans-capacitance network, it produces better predictions of the dynamic performance and transient response. Previous models used one or more lumped static gate capacitances and an ideal ballistic transport model [8, 11]. The CNFET structure used in this work is shown in Figure. 1. Each CNFET employs 3 SWCNTs under its gate. The CNTs under the same gate are assumed to be identical. The section of the SWCNT directly under the gate is intrinsic; for the doped source/drain extension regions, the doping level is taken as 0.8% which is above the first conduction band of the SWCNT. The inter-CNT spacing (s) is 20nm. At this separation the charge screening effect that each CNT under the gate has on its neighboring CNT and its effect on drive current and device performance is negligible [12]. The model assumes equal electron and hole mobility in CNTs.

III. SIMULATION CONDITIONS

To be consistent with previous work done in our group [6], different values for mean diameters in the range 1.01 nm to 1.71 nm were taken into account. Considering the inaccuracy of fabrication techniques, a standard deviation (STD) from the mean in the range of 0.04nm to 0.2nm [6] was introduced for each mean diameter value. Diameter distribution is assumed as Gaussian; a reasonable assumption for large numbers of fabricated CNTs [5, 6]. We also consider a positive distribution as the diameter of a CNT always has a positive value.

Our focus is on CNFET circuit performance benchmarked with the standard digital library cells. NOT, NAND and NOR gates have been implemented and simulated using HSPICE. Monte Carlo simulations were run with varying CNT mean diameters and STDs. For each run, diameter distribution properties were varied within the ranges mentioned above. Five different samples for mean diameter were taken into account. For each mean diameter sample, five categories of STD in the range 0.04nm to 0.2nm were considered. As long as CNT diameter is less than 3 nanometers (nm) (typical for CNT devices) and the transistor is taken to be a short-channel device, where CNT length under the gate is less than 100nm, only the first conduction/valence bands have a significant effect on current with a power supply of less than 1V [11]. A physical channel length of 32nm and an oxide thickness of 4 nm are assumed. This channel length is short enough for the device to be assumed short channel and long enough for the model to correctly simulate the device (CNFETs with channel lengths under 10nm can't be simulated correctly by the model). The physical metal gate width is assumed to be 48nm. This width affects the parasitic capacitance but the on current depends on the actual *effective* gate width which is determined by the number of CNTs under the gate and the spacing between them. A power supply voltage of 0.9V is used according to the ITRS roadmap for 32nm technology [14]. 10,000 samples were taken and Monte Carlo iterations were run for each mean diameter and STD considered. All simulations are run for the 32nm technology node.

We use the following definitions of delays [15]: *Propagation delay*: maximum time from the input crossing 50% to the output crossing 50%. We have taken this as the high to low output transition for NAND gates and low to high output transition for NOT and NOR gates.

Rise time: time for a waveform to rise from 10% to 90% of its steady-state value

Fall time: time for a waveform to fall from 90% to 10% of its steady-state value

The test circuit structure for all gates considered is shown in Figure 2. Alternative fan-in/fan-out combinations were also tested; similar behavior (to be discussed in the next section) was observed regarding timing variations. Due to space restrictions only results with a fixed fan-in/fan-out are shown.

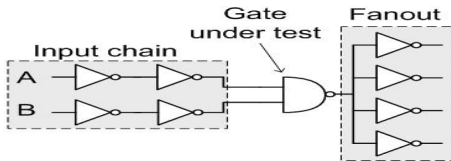


Figure 2. Test Circuit

IV. RESULTS

This section presents the simulation results for basic logic gates with the conditions specified in Section III.

A. NOT Gate

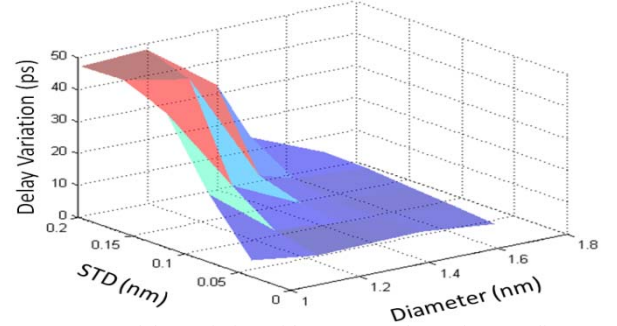


Figure 3. Inverter delay variation with respect to change in CNT diameter and STD

Figure 3 shows variation of delay of an inverter with respect to CNT diameter and STD. It can be observed from the plot that for smaller STDs, variation in delay is in the order of a few picoseconds (ps). As STD increases delay variation also increases. The variation in delay becomes quite significant for bigger STDs and smaller CNT mean diameters. Results show that there is greater delay variation at smaller diameters of CNTs. As the energy band gap of a CNT is inversely proportional to its diameter [16], CNTs with larger diameters have smaller band gaps. A smaller band gap means that a transistor made of CNTs with larger diameters can exhibit higher on-currents; this translates into shorter delay times. CNTs with smaller diameters have higher source/drain resistance which can be explained by the fact that at small diameters only the first sub-band is degenerate [13].

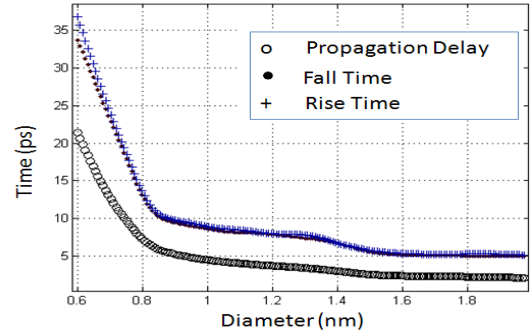


Figure 4. Delay variation of NOT gates with respect to Diameter variation

Figure 4 shows the timing characteristics of the simulated inverters. The gates' fall and rise times are almost identical. This is due to the assumption that holes and electrons have equal mobility in CNTs [12]. It is observed from Figure 4 that below a diameter of around 0.85nm delay dependency on diameter increases resulting in a rapid rise in delay variation.

B. NOR Gate

Figure 5 shows that for the NOR gates again delay variation rises significantly at smaller mean diameters and greater STD values. Fall time is reached almost twice as fast as rise time for

the NOR gates. The pull up network consists of two p-type CNFETs in series. The pull down network is made of two n-type CNFETs in parallel. Carriers experience less resistance through the two parallel n-type transistors of the pull-down network and as hole and electron mobility is equal fall time is reached almost twice faster than rise time (Figure 6).

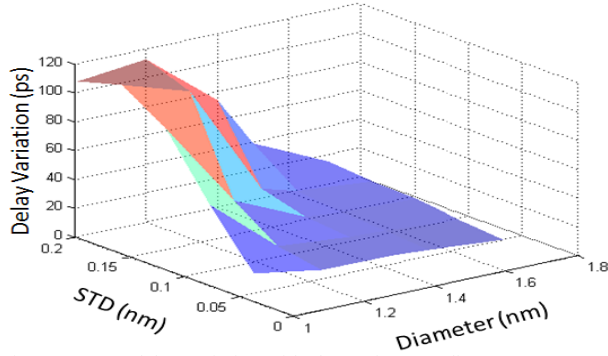


Figure 5. NOR delay variation with change in CNT diameter & STD

As far as delay variation is concerned a great variation for diameters smaller than around 0.85nm is observed in Figure 6.

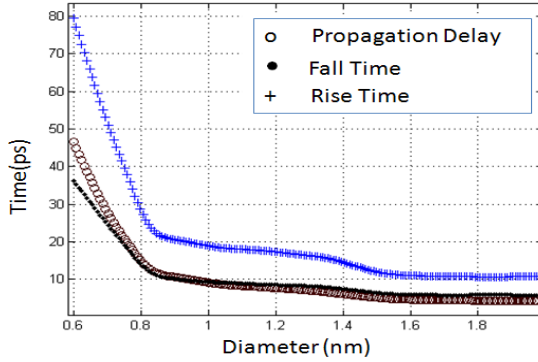


Figure 6. NOR delay variation with respect to Diameter variation

C. NAND Gate

Similar to previous cases, Figure 7 shows that for NAND gates delay variation also rises significantly at smaller mean diameters and greater STDs. It can be observed from the plot that delay variation ranges from around 5 ps at larger mean diameters with small STDs to over 100ps at small mean diameters with large STDs.

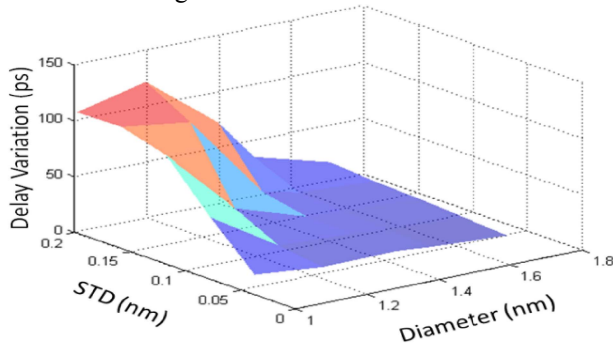


Figure 7. NAND delay variation with respect to change in CNT mean diameter and STD

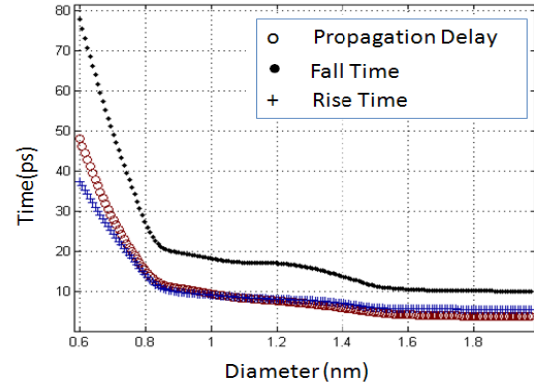


Figure 8. NAND delay variation with respect to diameter variation

Figure 8 shows the delay variation of NAND gates with respect to changing CNT diameter. In this case, rise time is almost twice less than the fall time which is the expected result as the pull up network of a NAND gate consists of two parallel p-type CNFETs which have half the resistance of the two n-type CNFETs in the pull down network (due to the equal electron and hole mobility), hence rise time in this type of gate is faster than fall time. As far as timing variation is concerned we see far less variation for CNT diameters greater than around 0.85nm.

V. DISCUSSION

Our simulation results show that delay variations in all considered CNFET-based gates depend on both CNT mean diameter and STD. As an illustrative example in Figure 9 multiple Probability Density Function (PDF) curves are depicted for propagation delay of NAND gates with a CNT mean diameter of 1.5nm and various STDs, normally distributed in the range of 0.04nm to 0.2nm. It can be observed that as STD increases, the distribution of possible propagation delay values rises. The same PDF plots for smaller CNT mean diameters show far greater variations in propagation delay, a result which is expected as the same STD values for smaller mean diameters translate into greater deviations from the smaller mean diameters compared with larger mean diameters and hence greater drive current and delay variations. A conclusive table of such measurements for different gates with different mean diameters and STDs is presented for a sample set of our simulation results in Table 1.

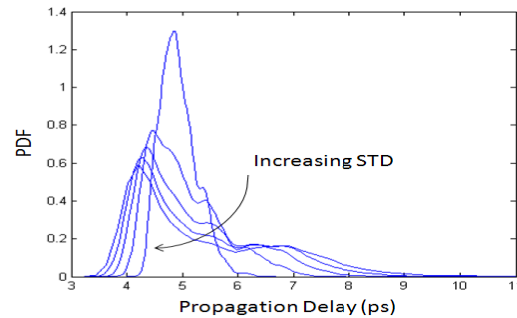


Figure 9. NAND delay variation with respect to diameter & STD

TABLE I. DELAY BEHAVIOUR WITH STD = 0.2nm

Gate	Mean Diameter(nm)	Min Delay (ps)	Max Delay (ps)	Delay Variation (ps)
NOT	1.01	4.82	51.57	46.75
	1.4	4.821	37.25	32.439
	1.71	4.931	9.539	4.608
NAND	1.01	5.382	111.4	106
	1.4	5.523	76.68	71.157
	1.71	5.169	20.48	15.311
NOR	1.01	6	113	107
	1.4	5.48	78.76	73.28
	1.71	6.2	20.71	14.5

In Table I, mean diameters for the 3 different gates are chosen with a fixed STD of 0.2nm and min/max worst case fall/rise time delays are shown for each gate at chosen diameters. Our results show that inverter delay variation shows a 10 times improvement as mean diameter is increased from 1.01nm to the maximum mean diameter of 1.71nm. In the cases of NAND and NOR gates delay variation shows an improvement by a factor of 7, suggesting that it is well worth employing CNTs with larger diameters if one desires to minimize delay variations.

Results for all simulated gates as seen in Figures 4,6 and 8 show that for all cases diameter should be kept above 0.85nm to ensure more consistent timing characteristics; hence:

$$d_{\mu} - \Delta d \geq 0.85nm \quad (1)$$

where, d_{μ} is mean CNT diameter and Δd is diameter variation given by:

$$\Delta d = d_{\mu}x, \quad (2)$$

x being a process-dependent constant defining the manufacturing tolerance for fabrication of CNTs. Thus:

$$d_{\mu} \geq \frac{0.85nm}{1-x} \quad (3)$$

For instance, if we assume a process with a 30% manufacturing tolerance [19], for reliable timing operation we need a mean diameter defined by (3):

$$d_{\mu} \geq \frac{0.85nm}{1-0.3} \cong 1.2nm \quad (4)$$

The relation tells us that we need to choose our mean CNT diameter larger than 1.2nm.

VI. CONCLUSION

We have shown that larger CNT diameters and smaller STDs provide us with more reliable timing operation and faster delay times. We have also proposed a relation by which a minimum mean diameter can be chosen to ensure minimum delay variation for various CNT-based logic gates. In order to propose an optimum CNT diameter for logic design a tradeoff between fast operation and power consumption should be taken into account. This is the direction of our future work.

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