Electromechanical Simulation of Switching Characteristics for Nanoelectromechanical Memory

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The static switching properties and readout characteristics of proposed high-speed and nonvolatile nanoelectromechanical (NEM) memory devices are investigated. By conducting a three-dimensional finite element mechanical simulation combined with an electrostatic analysis, we analyze the electromechanical switching operation of a mechanically bistable NEM floating gate by applying gate voltage. We show that switching voltage can be reduced to less than 10 V by reducing the zero-bias displacement of the floating gate and optimizing the cavity structure to improve mechanical symmetry. We also analyze the electrical readout property of the NEM memory devices by combining the electromechanical simulation with a drift-diffusion analysis. We demonstrate that the mechanically bistable states of the floating gate can be detected via the changes in drain current with an ON/OFF current ratio of about 3×10^4.
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1. Introduction

Over the past few decades, silicon nanofabrication techniques for very large scale integrated circuit (VLSI) have been developed, and the performance of a complementary metal–oxide–semiconductor (CMOS) circuit has drastically been improved. The development of microfabrication technologies have also enabled the fabrication of micro-electro-mechanical systems (MEMSs) such as cantilever beams and membranes, and their applications to sensors, resonators, and so on.[1,2] In addition, MEMSs have recently been miniaturized to sub-micron/nanoscale, which are called nanoelectromechanical systems (NEMS), whose mechanical and electrical properties have extensively been investigated.[3–6] For example, an oscillation frequency of over 1 GHz has already been reported for a 1.1-μm-long SiC-based beam.[6] Since the operation speed of NEMS increases primarily inversely proportional to their characteristic lengths, extremely fast NEMS with a switching time close to that of electronic devices may be realized by reducing their dimensions into the 100-nm regime. It may therefore be worthwhile to consider integrating NEMS components into conventional Si devices in order to add new functionality.[7,8)]

We have proposed a new fast and nonvolatile memory device[9] based on the bistable operation[10,11] of a sub-μm-long NEMS structure, combined with nanocrystalline (nc-) Si quantum dots.[12] A basic concept of nonvolatile memory based on the mechanical bistability of a micromachined bridge has been reported.[13] Our NEMS memory features a suspended SiO_2 beam formed in the cavity as a floating gate, which incorporates nc-Si dots for charge storage (Fig. 1). Once an electron is stored in such a small Si nanodot, another electron transfer probability into the dot is strongly reduced owing to the Coulomb blockade effect even at room temperature.[14] The amount of charge in the beam can

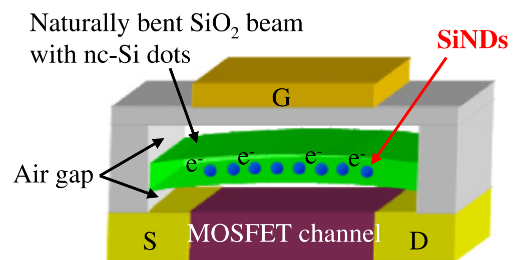

Fig. 1. (Color online) Schematic illustration of a NEMS memory device featuring a buckled floating gate suspended in the cavity above the sense MOSFET.

therefore be determined by the number of nc-Si dots. We use a very high frequency digital plasma process for nc-Si deposition that facilitates the deposition of nc-Si dots of 8 ± 1 nm in diameter.[15,16] The density of the 8 nm nc-Si dots is typically about 10^{11}–10^{12} cm^{-2} in a monolayer. We can control the amount of the nc-Si dots precisely by adjusting the deposition condition. In order to inject electrons into the nc-Si dots, we apply a high voltage to the gate electrode for initialization. Then, the electrons are injected into the nc-Si dots through the sidewalls, or the gate electrode contacts the floating gate and the electrons are injected through the SiO_2 of the floating gate. The beam is buckled either upward or downward, and its both ends are clamped at the cavity sidewalls. When the gate voltage is applied, the charged beam moves in the cavity via electrostatic interactions between the gate electrode and the charge stored in the beam. A positional displacement of the beam changes the surface potential of the metal–oxide–semiconductor field-effect transistor (MOSFET) placed underneath and is therefore sensed as a shift of its threshold voltage. Write and erase operations of the NEMS memory are not associated with charge tunneling via the gate oxide and therefore do not cause any gate oxide deterioration, which limits the endurance cycles of a conventional flash memory. On the

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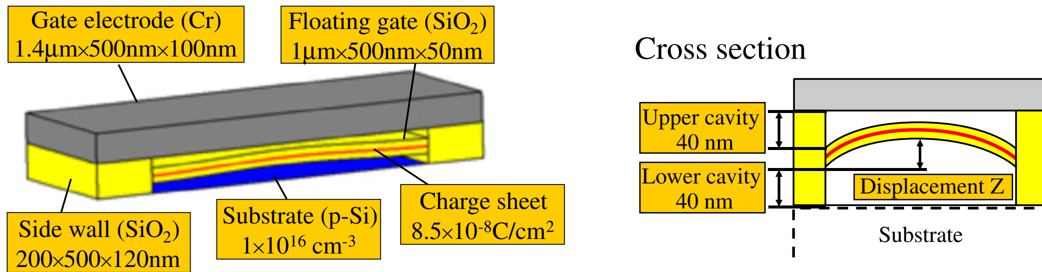

Fig. 2. (Color online) Structure and structural parameters used for simulation.

other hand we obviously need to quantify the impact of mechanical fatigue of the beam on the endurance cycle for our NEMS memory. However, amorphous SiO_2 that we use to fabricate the beam is supposed to be mechanically robust as demonstrated by a recent experimental study of high-frequency mechanical vibration characteristics of a SiO_2 wire.[17)]

In a past experiment[18)] we fabricated a 3-μm-long free-standing SiO_2 single beam using a Si undercut etching technique. The mechanical bistability of the beam was successfully demonstrated using the nanoindentor loading system.[19)] We also performed a mechanical simulation of the three-dimensional finite element method (FEM) and obtained the mechanical properties of the floating gate for switching operations.[20)] However, in an actual switching operation of NEMS memory, the floating gate switches by applying the gate voltage. In this study, therefore, we conduct a three-dimensional finite element analysis by combining mechanical and electrostatic simulations, and investigate the switching operation via an electric field applied across the beam. We also show the readout properties of the NEMS memory by electromechanical simulation combined with drift-diffusion analysis.

2. Switching Operation via Electrostatic Interaction

In order to observe the switching phenomenon of the floating gate by applying electrostatic force, we should consider the deformation of structures and the electrostatic potential distribution. Therefore, we solved Navier's equation and Poisson's equation simultaneously. We used the finite element method simulator COMSOL Multiphysics[21)] to solve these two equations. Figure 2 shows the three-dimensional structure used for the present simulation. Sidewalls and the floating gate are formed using silicon dioxide. For simplicity, we ignored the effects of Si nanodots on the beam mechanical property. The electrode was assumed to be chromium. Young's modulus values and Poisson's ratios are 70 GPa and 0.17 for SiO_2, and 140 GPa and 0.21 for Cr, respectively. The dielectric constants are 4.2 and 11.9 for SiO_2 and Si, respectively. In the mechanical simulation, the bottom of the sidewalls was assumed to be physically fixed. The internal compressive stress was introduced into the floating gate to take account of the residual stress caused during the thermal oxidization process. We were not able to measure the residual stress of our floating gate. However, we observed the buckling of the floating gate by SEM measurement. We compared the measurement result with the simulation result of the buckling, and we used a compressive stress of 670 MPa as the internal stress. In the electrical simulation, the bottom of the sidewalls was grounded electrically. On the silicon substrate surface, the surface potential ψ_S and the surface charge Q_S satisfy the following equation,

$$Q_S = \mp \frac{\sqrt{2}kT}{qL_D} F\left(\psi_S, \frac{n_{p0}}{p_{p0}}\right) \quad (\psi_S > 0 \rightarrow -, \psi_S < 0 \rightarrow +), \tag{1}$$

where L_D is the Debye length, and n_{p0} and p_{p0} are the electron and hole densities in the p-type substrate, respectively.[22)] For simplicity, we assumed that the floating gate sandwiched a charge sheet instead of nc-Si dot layer as stored charges. The electrostatic force F_{es} applied to the upper and bottom surfaces of the floating gate as well as the SiO_2/charge-sheet interfaces is expressed by the equation below.[23)]

$$\mathbf{F}_{es} = \iint_S \mathbf{T} \cdot \mathbf{n} dS \quad T_{ij} = -\frac{1}{2}(\mathbf{E} \cdot \mathbf{D})\delta_{ij} + E_i D_j \quad (i, j = x, y, z). \tag{2}$$

E, **D**, and **n** represent the electric field, electric displacement, and normal vector, respectively. Under these conditions, we monitored the vertical shift of the beam center relative to its flat position Z by sweeping gate voltage and calculated the beam displacement–gate voltage Z-V_g characteristic. The obtained results are shown using a broken line with solid circles in Fig. 3(a). The figure shows that the floating gate has two stable states, which are upward- and downward-bent states at zero bias, and the floating gate can be switched between the two states by applying gate voltage. A switching voltage of approximately −13 V was found for the downward- to upward-bent state switching, and that of approximately 38 V for the reverse switching.

In our past analysis,[20)] we found that the mechanical switching force was proportional to the cube of zero-bias displacement, which is the beam displacement without any applied force or field. Smaller zero-bias displacements should therefore lower switching voltage. We calculated the relationship between beam displacement and gate voltage at various initial zero-bias displacements. In order to vary zero-bias displacement, we changed the internal stress of the floating gate to 670, 650, and 645 MPa. Zero-bias displacement decreases with decreasing stress. In the actual fabrication process, we can control the stress by changing the oxidation and annealing conditions of the thermally oxidized SiO_2 film. As a result, switching voltage decreases with decreasing zero-bias displacement [Fig. 3(a)]. However, the hysteresis loops also shrink, and the downward

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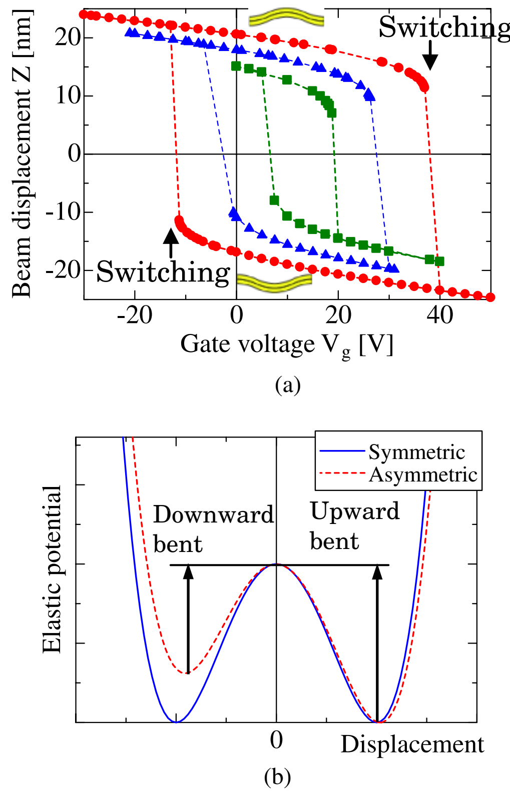

Fig. 3. (Color online) (a) Beam displacement–gate voltage relationship at various initial zero-bias displacements (20.6, 18, and 15 nm). (b) Elastic potential shape for symmetric and asymmetric structures.

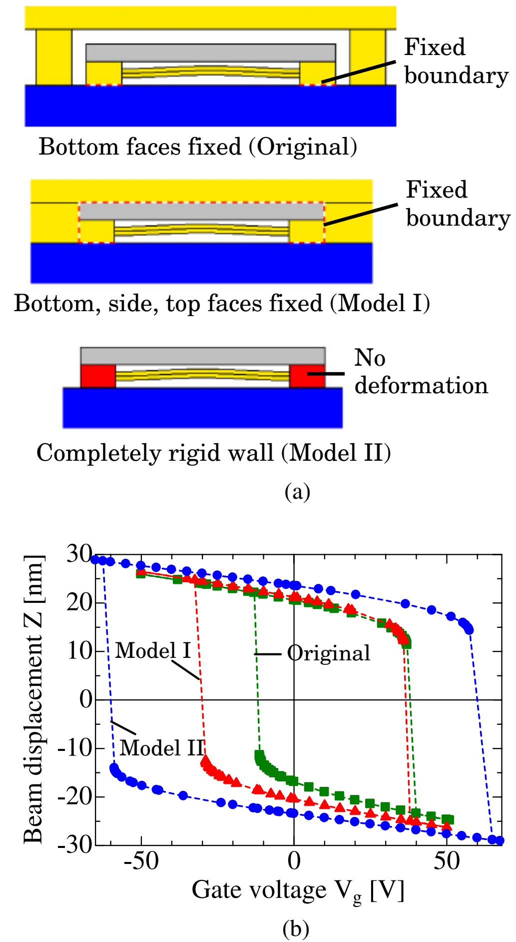

Fig. 4. (Color online) (a) Surrounding conditions and fixed boundaries. (b) Beam displacement–gate voltage relationship for three structures that have different fixing conditions.

bent state is no longer stable at zero gate bias for the case of a zero-bias displacement of about 15 nm, as shown by a broken line with solid squares. Switching voltage cannot therefore be reduced to less than 20 V by simply decreasing zero-bias displacement.

In order to reduce switching voltage further, we need to shift and/or expand the entire hysteresis curve in the direction of negative gate voltage. We analyzed the physical mechanism behind the asymmetric hysteresis loop in terms of the deformation of the sidewalls and structural asymmetry. In the present structure, both ends of the floating gate are clamped at the sidewalls with finite elasticity and therefore not fixed completely. Thus, the elastic potential energy of the floating gate is affected by the surrounding cavity structure. The cavity structure is obviously symmetric in the horizontal direction, but not in the vertical direction. The asymmetry of the hysteresis loop largely depends on the mechanical symmetry of the cavity structure as well as the details of clamping conditions on the floating gate. Therefore, the elastic potential curve does not show symmetric double minima for the upward- and downward-bent states [Fig. 3(b)]. To investigate this issue, we studied the effects of the beam fixing conditions by changing the surrounding structures. Figure 4(a) show three structures used for the analysis. The top structure is the one used for the above simulation (Original). The entire beam cavity structure is physically fixed only at the interface between the bottom planes of the sidewalls and the substrate. In contrast, the middle structure shown in Fig. 4(a) is covered with a rigid surrounding structure, and all the bottom, side and top planes of the cavity are fixed physically (Model I). For comparison, we also introduce a structure shown at the bottom of Fig. 4(a) where the sidewalls of the cavity are completely solid and the both ends of the beam are fixed (Model II). This is an unrealistic assumption, but Model II is useful to discriminate the effects of the deformation of the sidewalls and to clarify the intrinsic mechanical properties of the floating gate. The beam displacement–gate voltage characteristics obtained for the three structures are shown in Fig. 4(b). The internal stress is 670 MPa. For Model II, the hysteresis loop is found to be nearly symmetric with respect to the zero-bias axis although the switching voltages are extremely high. This proves that the deformation of the sidewalls and the gate is the major origin of the asymmetry of the hysteresis loop. Comparing Original with Model I, the hysteresis loop expanded to the left, and the symmetry is improved greatly by fixing the outer planes of the cavity. We therefore employ this structure for the following analysis.

Next, we study the effects of the clamping point of the floating gate in the cavity in order to improve the hysteresis symmetry further. Varying the beam clamping point relative to the MOSFET surface may induce changes not only in mechanical symmetry but also in electrostatic potential symmetry. In Fig. 5(a), the upper and lower air gaps of Original are both 40 nm. Model U has a higher clamping point, and the upper and lower air gaps are 30 and 50 nm, respectively. Model L has a lower clamping point, and the

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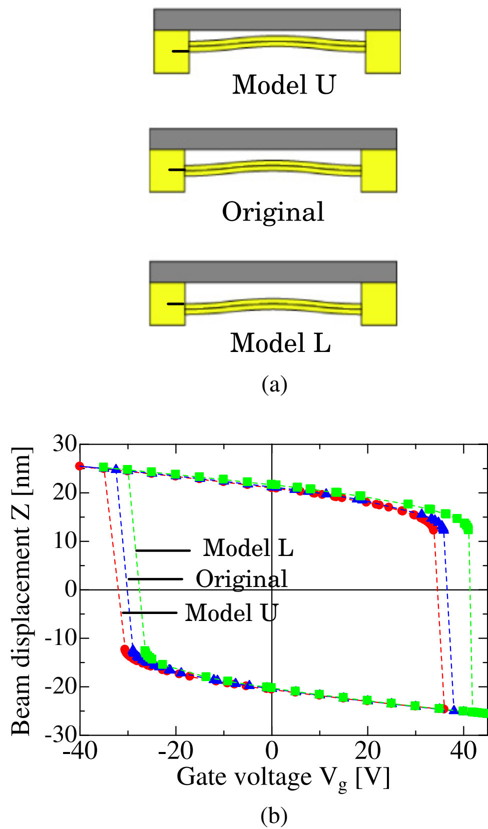

Fig. 5. (Color online) Beam displacement–gate voltage relationships for various positions of attachment of the floating gate.

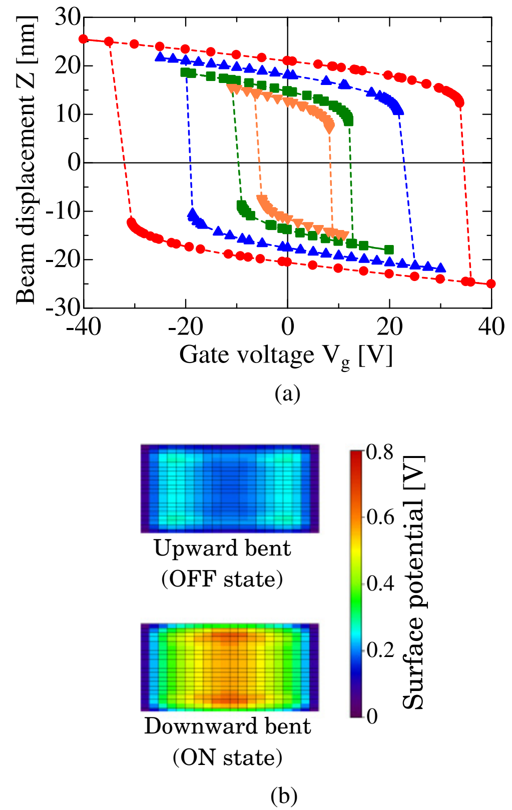

Fig. 6. (Color online) (a) Beam displacement–gate voltage relationships at various zero-bias displacements for the improved structure. (b) Substrate surface potential distribution at zero bias.

upper and lower air gaps are 50 and 30 nm, respectively. The total cavity height between substrate and the top gate is kept constant. The internal stress is 670 MPa. The results in Fig. 5(b) show that the hysteresis loop can be shifted to the left by moving up the clamping point in the cavity. As we discussed above, we adopted the mechanical boundary condition that fixes the top outer surface of the gate electrode and the surface of the silicon substrate physically. Therefore, our cavity structure, in principle, holds the mechanical mirror symmetry in the vertical direction around the midpoint of cavity height. Since the gate electrode has a finite thickness, however, the mechanical mirror symmetry plane locates not just right at the midpoint of the cavity air gap but slightly above it. This is presumably the reason why Model U results in a highly symmetric hysteresis among the three structures. Therefore, we choose it as the best optimized floating gate structure.

Using the optimized structure, we then calculated the gate voltage-beam displacement characteristics again at various zero-bias displacements, as shown in Fig. 6(a). The internal stresses are 670, 650, 630, and 620 MPa, for zero-bias displacements of 20.8, 17.8, 14.3, and 12.1 nm, respectively. The optimized structure enables us to decrease the zero-bias displacement to a much smaller value than that used for the original structure without losing the zero bias bistability. The switching voltage was found to be reduced to less than 10 V. There is an obvious tradeoff between the reduction in switching voltage and the increase in the ON/OFF ratio of MOSFET current. An excessive decrease in the initial zero-bias displacements therefore may degrade the readout capability. However, we confirmed that the substrate surface potential distribution shows an obvious change for the bistable floating gate states at zero bias for the smallest zero-bias displacement, as shown in Fig. 6(b). The simulation results show the surface potential changes of between 0.2 and 0.6 V around the center of the floating gate, which is sufficient to induce a current change in the MOSFET, as shown in the next section.

3. Electrical Readout Property Analysis

In order to investigate the electrical readout properties of our NEMS memory, we finally conducted hybrid simulation by solving the semiconductor carrier transport equations as well as the electromechanical equations above. In the present simulation, three-dimensional Navier's equation, Poisson's equation, and carrier continuity equation were solved simultaneously. Figure 7(a) shows the simulated structure of the NEMS memory cell; the optimized floating gate in the cavity structure is integrated into the MOSFET. The substrate region is p-type silicon with an impurity density of 5×10^{15} cm^{-3}, and the source and the drain region are n-type silicon with an impurity density of 5×10^{17} cm^{-3}. The electron and hole mobilities have low impurity concentrations of 1000 and 400 cm^2/(V·s), respectively. The source, drain, and substrate voltages were kept constant to be 1, 0, and 0 V, respectively. We conducted a steady-state analysis and monitored beam displacement and drain current with gate voltage sweeping. As shown in Fig. 7(b), the drain current–gate voltage characteristic showed a hysteresis associated with the bistable states of the floating

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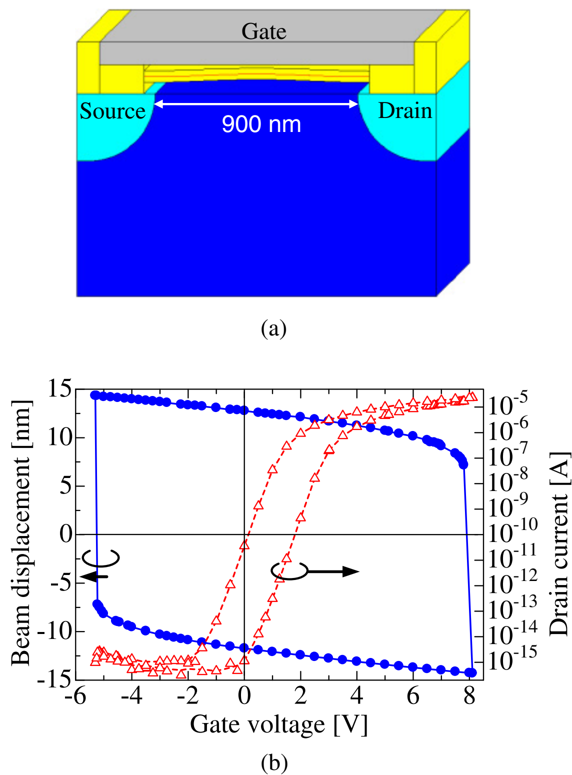

Fig. 7. (Color online) (a) Simulated three-dimensional structure with added substrate structure. (b) Beam displacement, drain current–gate voltage relationships. Circle plot shows beam displacement and triangle plot shows drain current.

gate. The threshold voltage shift and ON/OFF current ratio were found to be approximately 1.6 V and 3×10^4 at $V_g = 0$ V, respectively. These results demonstrate that the bistable states of our NEMS memory can indeed be read via drain current. Further improvement of ON/OFF current ratio is certainly needed to make our NEMS memory competitive with other emerging nonvolatile memories, but there still remains much room for optimizing device parameters such as zero-bias displacement, air gaps, and impurity density. The density of nc-Si dots can still be increased to about twice that of the structure used in this study. We expect that the higher density of the stored charge improves the threshold voltage shift and the ON/OFF current ratio increases to about 10^5–10^6.

4. Conclusions

The static switching properties and readout characteristics of the NEMS memory were investigated by three-dimensional hybrid FEM simulation in which structural analysis, electrostatic analysis, and carrier transport analysis were performed simultaneously. We showed that the memory states could be switched by applying gate voltage and that switching voltage was reduced by decreasing zero-bias displacement and improving structural symmetry; the switching voltage may be reduced to less than 10 V by optimizing the overall structures. While maintaining the switching voltage low, we demonstrated that the memory states could be detected via the difference in drain current with an ON/OFF current ratio of about 3×10^4.

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