Impact of NBTI on the Performance of 35nm CMOS Digital Circuits

Yangang Wang and M. Zwolinski
School of Electronics and Computer Science, University of Southampton, Southampton, SO17 1BJ, UK,
E-mails:yw2@ecs.soton.ac.uk, mz@ecs.soton.ac.uk

ABSTRACT

The negative bias temperature instability (NBTI) of p-MOSFET has the greatest impact on the long term reliability of nano-scale devices and circuits. For several decades, NBTI research has been focused at the device physics level or on the characterization methodology, with little attention paid to the impact of NBTI on the performance of basic digital circuits. This paper discusses the effects of NBTI on 35nm technology CMOS inverters and SRAM. The delay degradation and power dissipation of the inverters, as well as the static noise margin degradation of the SRAM are analysed. Moreover, the effects of power supply voltage on inverters and the cell ratio on SRAM under NBTI are also discussed.

Keywords: Degradation, inverters, negative bias temperature instability (NBTI), SRAM, static noise margin.

1. INTRODUCTION

For state-of-the-art p-MOSFETs, two main factors cause the negative bias temperature instability (NBTI) to restrict device lifetime. One of these is the continuous increase of the effective oxide electric field [1], the other is the adverse effect of introducing more nitrogen into the oxide [2-5]. Furthermore, NBTI was also reported as a critical reliability issue in the high-κ dielectric [6]. Therefore, much effort has been devoted to this important reliability issue in the last 10 years. Researchers are usually concerned with the topics such as the physical mechanism of degradation and recovery, as well as the characterization methodology [1-5]. The degradation is generally ascribed to the formation of Si/SiO_2 interface states (N_{it}) and the oxide positive charges (N_{ot}). The N_{it} is related to Si dangling bonds because of the breaking of the Si–H bonds, and the reaction as well as the H diffusion was regarded as the mechanism of NBTI kinetics [7]. The N_{ot} is linked either with hole trapping by Oxygen/Nitrogen atoms and/or vacancies [2,3], or with the generation process such as the breaking of Si–O and Si–N bonds [8]. On the other hand, the recovery of NBTI after removing the high stress voltage is firstly thought of as the re-passivation of the Si– by the returning of H [9], and then the fast recovery was taken to be the detrapping of trapped holes [10]. Moreover, the traditional measurement technique was thought too slow to monitor the real degradation for losing the fast recovery part. Therefore, some fast techniques were developed which characterize the NBTI by the linear drain current without removing the stress bias, and the degradation can be one order of magnitude higher than that measured by the traditional technique [5,11].

Although NBTI has been considered as one of the design parameters for long term circuit reliability concerns, compared to the research on the above aspects, little work has been reported on the impact of NBTI on nano-scale digital and analog circuits [12-16]. NBTI induces increasing of threshold voltage (V_{th}) and degradation of transconductance, which results in a decrease of the transistor switching speed and the driving capacity. Therefore, the lifetime performance of digital circuit can be affected significantly by NBTI. For analog circuits, problems exist in the NBTI induced mismatch on matched devices pairs [13-15].

In this paper, the effects of p-MOSFET NBTI on the performance of basic nano-scale digital cells, which are the building blocks of most digital circuits, such as CMOS inverters and SRAM are investigated, and a method for mitigating NBTI effects is proposed.

2. SIMULATION METHODOLOGY

The performance of the digital cells such as the delays, the power/energy dissipations and the voltage transfer characteristics are simulated by transient and DC analysis using SPICE. The BSIM4 model cards are used with the parameters extracted from 35nm technology MOSFETs [17]. The device channel width may change to study the circuit performance variations.

It is reported that the ΔV_{th} of NBTI follows a power law with respect to stress time and the typical ΔV_{th} varies from several tens of millivolts to more than one volt [1-5]. This work does not address the physical origins of NBTI, and the degradations of V_{th} are set in the SPICE input files by changing the V_{th0} of the p-MOSFET BSIM4 model cards. A series of V_{th} are swept one by one during the

simulation. Unless otherwise specified, the supply voltages (V_{dd}) are 1.0V, and the circuit temperature is set at 100°C which is the typical value for device operational temperature.

3. RESULTS AND DISCUSSIONS

3.1 THE CHAIN OF CMOS INVERTERS

The performance of a single inverter and a chain of inverters are affected significantly by the V_{th} of both n and p-MOSFETs (V_{thn} and V_{thp}). The voltage transfer characteristics (VTC) can drift in parallel under NBTI, which induces variations in the delays, switching characteristics and power dissipations. For nano-scale MOSFETs, the increase in the subthreshold drain current because of short-channel effects also has adverse effects on the performance of inverters.

The inverter delay (t_d), which consists of the high-to-low (t_{df}) and low-to-high (t_{dr}) delays, is related to the switch speed and power dissipation. Therefore, the improvement of t_d is always taken into account by designers. In physical terms, t_d is determined by the on-state resistance of device as well as by the loading capacitance. For the chain of inverters, the switching delay is characterized by the propagation delay (τ), which is half of the sum of the pull-down τ (τ_n: time from $V_1=V_{dd}/2$ to $V_2=V_{dd}/2$) and pull-up τ (τ_p: time from $V_2=V_{dd}/2$ to $V_3=V_{dd}/2$) [18]. For ideal cases, the steady state power dissipation (P) is negligible, and P is controlled by the switching process. However, as the steady state current increases in the nano devices, P also increases compared to long channel cases.

Fig.1(a) and (b) are the relative delays and power dissipation variations of inverters induced by NBTI. The increase in V_{thp} slows the switching speed of the devices, which prolongs the delays. In Fig.1(b), the 5-stage inverters are simulated with all the p-MOSFETs having the same ΔV_{thp}.

It is reported that the delay of inverters has a power law relationship with stress time, which means the delays increase linearly with ΔV_{thp} [12]. In Fig.1, both t_d and τ have an approximate linear relationship with ΔV_{thp}, which can be explained by the gate delay models [12]. It is noticed that the delay degradation is smaller than the degradation in V_{th}. When a 100mV in V_{thp} degradation is taken as the failure criteria, the variation ratios of V_{th}, t_d and τ are 37.1, 5.5 and 16%, respectively, the difference ratios are related to V_g-V_{th} in theory [12].

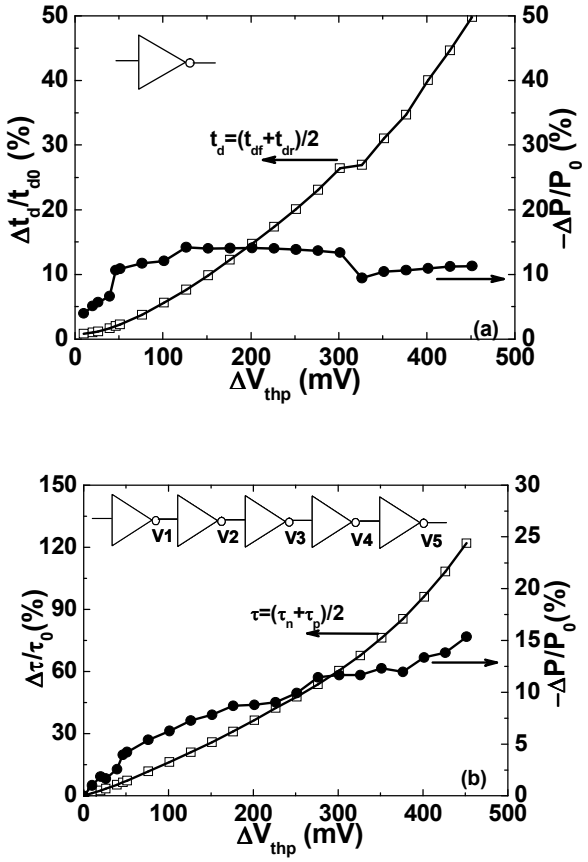

Fig.1 The delays and power dissipations of the inverter (a) and the chain of inverters (b) under NBTI

The power dissipation is another limiting factor for designing nano-scale circuits. The increase of delays because of NBTI does not cause an increase in the power/energy dissipations. On the contrary, as shown in the Fig.1, P decreases significantly under NBTI. The reason is that both the subthreshold drain current (steady state current) and the switching current decrease significantly with V_{thp} increasing.

With the scaling down of the device dimensions, the power-supply voltage decreases, which induces an increase in the delays but a decrease of P. Fig.2 shows the relative variations of τ and P with V_{dd} decreasing under NBTI. The delay degradations are enhanced by lower V_{dd}, while the P improvements are insensitive to V_{dd} to some extent. According to Fig.2, it is suggested the trade-off V_{dd} for the 35nm CMOS inverters subjected to NBTI is 0.9-1.0V.

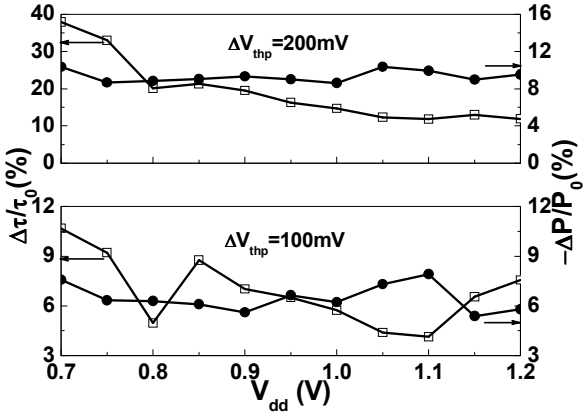

Fig.2 The τ and P variations of the chain of inverters under NBTI versus the power-supply voltage

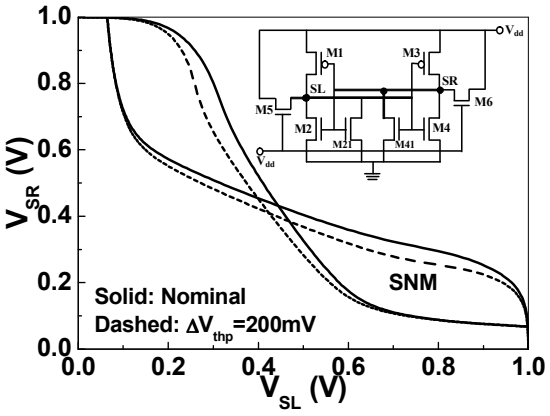

Fig.3 The static transfer characteristics and the static noise margin of the SRAM, inset is the circuit schematics

3.2 THE CMOS SRAM

As one of the most important parts of modern microprocessors and SOCs, the SRAM cell is often considered as the benchmark for the development of CMOS technology [17,19]. V_{th} mismatch will result in stability problems for SRAM using minimum geometry transistors. The stability of an SRAM cell is always characterized by the static noise margin (SNM), which is defined as the minimum DC noise voltage needed to flip the cell state [17,19]. SNM is a limiting factor for trading off the performance of a technology against the cost. The SNM can be calculated by the smaller area formed by the two static transfer characteristic (STC) curves. For the symmetric SRAM cell structure illustrated in Fig.3, the STCs are almost the same by either sweeping the V_{SL} or the V_{SR}.

Therefore, it is crucial to investigate the NBTI of SRAM for the moment [20]. The STC and SNM definition for a SRAM cell at initial state and at ΔV_{thp}=200mV are shown in Fig.3, the inset has the circuit schematics of a traditional SRAM cell. The two p-MOSFETs (M1, M3) have the same ΔV_{thp} during the simulation. The ΔV_{th} can affect the shapes of the STCs and then the SNM.

Fig.4 shows the relative degradation of SNM as a function of ΔV_{thp}. The SNM degrades linearly with ΔV_{thp} (i.e. the stress time power law), which will in return limit the lifetime of the circuits. It is reported that the SNM degradation increases with decreasing supply voltage [21], so the importance of NBTI on SRAM will be more significant with the scaling of the device dimensions.

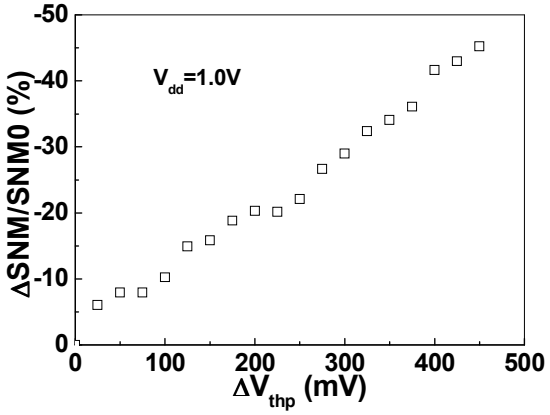

Fig.4 The relative degradation of SNM under NBTI

It is believed that the stability of SRAM can be improved by increasing the cell ratio (CR), which is the ratio of the driver transistor's (M2, M4) width/length (W/L) to the access transistor's (M1, M3) W/L [17,22]. During the above simulation, the CR is set to 2. When the CR increase to 5, Fig.5(a) shows the improvement of SNM is about 22% compared to CR equals to 2 for a nominal SRAM cell. Moreover, as shown in Fig.5(b), the SNM degradation ratios always reduce because of CR increasing at different levels of NBTI. However, the improvement of relative SNM degradation is not significant when CR become more than 3. As a large CR results in the increasing of cost and high power/energy dissipations, designers should take the above into account to find the optimal designs.

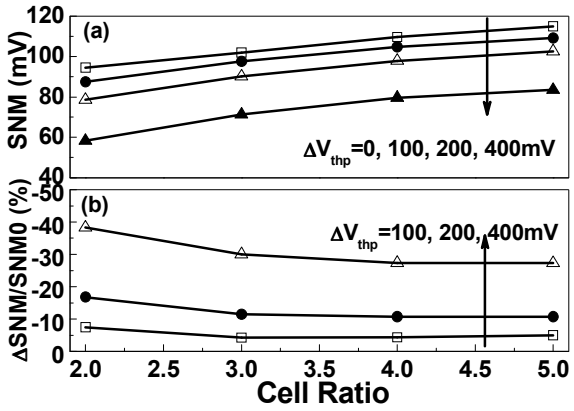

Fig.5 Both the SNM (a) and the relative degradation of SNM (b) are improved by the increasing of the cell ratio

4. CONCLUSIONS

The effects of NBTI on the performance of the 35nm CMOS inverters and SRAM are simulated in this paper. Although the delay degradation of the inverters increases significantly with NBTI, the power dissipation also decreases to some extent. The increasing of delays is induced by gate delays, and the decreasing of power dissipation results from the reduction of the subthreshold drain current and switching current. When taking the effects of NBTI on the delays and power dissipations into account, the trade-off V_{dd} for the 35nm CMOS inverters is 0.9-1.0V. On the other hand, for the traditional SRAM cells, the static noise margin degrades linearly with the NBTI. However, the SNM and the relative SNM degradation can be improved by increasing the cell ratio with a relatively higher cost. It is suggested the optimal cell ratio for the 35nm CMOS SRAM is about 3.

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