Series Resistance in Vertical MOSFETs with Reduced Drain/Source Overlap Capacitance

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Abstract

In this work we investigate the series resistances in vertical MOSFETs incorporating the fillet local oxidation (FILOX) structure that serves to reduce the gate to drain/source overlap capacitances. The series resistances are modeled analytically and the important influencing factors, namely gate bias dependence and the asymmetric nature of the device, are identified. We extract by simulation, R_d and R_s from devices with different FILOX thicknesses, employing an impedance method often used in RF characterisation. We identify the trade-off whereby thickening the FILOX first causes an increase of the cut-off frequency f_T, until the on-current I_{on} becomes limited by increasing series resistances and f_T therefore reduces. The results indicate a thickness of 40nm FILOX for maximum f_T. We also investigate the influence of process conditions on low series resistances, namely time of rapid thermal annealing RTA and angle of implantation.

1. Introduction

In our previous research into the feasibility of submicron Vertical MOSFETs (VMOST) for RF applications, a number of innovations have been proposed and their potential demonstrated in addressing device issues such as the overlap parasitic capacitance [1], short-channel effect [2] and parasitic bipolar effects [3]. As RF MOSFET scaling enters the deep micron regime, more attention is required on the effects of the drain and source series resistances on the overall device performance. It is already known that R_s and R_d exhibit gate bias dependence in MOSFETs [4]. It is also known that the device electrical performance and reliability, including the key performance indicators saturated drain current I_{on}, transconductance, noise figure, cut-off frequency and degradation due to hot carriers, depend more on source resistance R_s than the drain resistance R_d [5]. Therefore, in this work it is of interest to investigate series resistances in each junction of previously proposed vMOST concept with a fillet local oxidation (FILOX) structure [1]. Due to the asymmetrical characteristics of drain (top) and source (bottom) junction regions and the unique FILOX structure, it is important to obtain physical insight by first analytically modeling the gate bias dependence and asymmetric characteristics of the series resistance in relation to key metrics for further performance optimisation. The series resistances are extracted from a device generated from process simulation, using a small signal impedance method based on a practical RF measurement methodology. Next, series resistances for devices with different FILOX thicknesses are studied and an optimal value is identified based on a maximized gain-bandwidth product, f_T. Finally, some other key process parameters are identified in order to maintain low series resistances.

2. Simulation setup

2D computer simulations were carried out using the process simulator *Athena Silvaco* in accordance with the fabrication process as described in earlier work [1]. A sample device structure is shown in Fig.1 where FILOX is grown between the gate and the drain/source to reduce the overlap capacitances. Throughout this 'virtual experiment', the device channel length has been maintained at 100 nm with a gate oxide thickness of 4nm and a body doping level of $1x10^{18}cm^{-3}$. The FILOX thickness is varied from 20nm to 60nm while the RTA time and donor implant angle also vary in different experiments. The device simulations were conducted using the *Silvaco Atlas* simulation platform.

3. Analytical model

The series resistances in vMOST-FILOX can be modeled by the equivalent circuit shown in Fig.1a. The resistance components of concern occur along the current conduction path from the source to drain. In each junction, the series resistance is formed of three components: overlap region resistance R_{ov}, sheet resistance R_{sh} and contact resistance R_{co}. The scope of our work focuses on the overlap region resistance which constitutes a significant component of the total series resistance and also determines the asymmetric and gate bias dependencies. The overlap region resistance at the source junction is first analyzed from the schematic as shown in Fig.1b, where R_{acc} represents the accumulation layer resistance and R_{sp} represents the spreading resistance.

The derivation of accumulation resistances follows a surface potential based approach for modeling the

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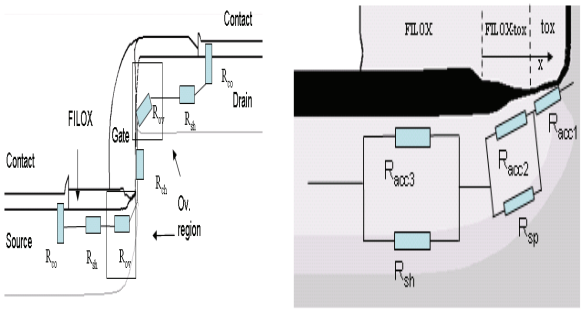

Fig1. a) A vMOST-FILOX structure (L=100nm) with an equivalent circuit of the series resistance; b) Series resistance in the overlap region of the source junction.

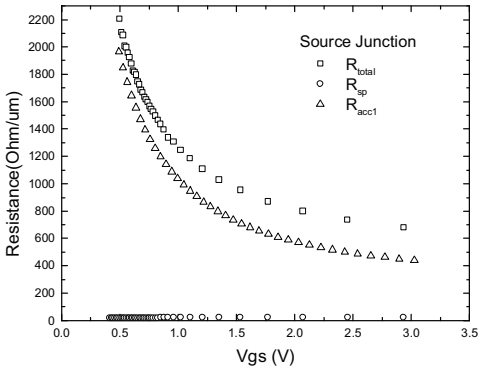

Fig.2 R_{acc1}, R_{sp}, R_{total} vs. V_{gs} of source junction

gate bias dependence of carrier charge density. This is unlike the work described in [6] where the surface potential in junctions was neglected and thus derivation of the gate bias dependence of accumulation layer charges was oversimplified. R_{acc1} under the uniform gate oxide is evaluated by integration of the local resistivity along the lateral junction depletion region. It can be expressed as below.

$$R_{acc1}(\phi_s) = \int_{l_{ext}-W_{dep}}^{l_{ext}} \frac{dx}{w \cdot u_{eff}(\phi_s) \cdot Q_{sov}(\phi_s, x)} \quad (1)$$

Where ϕ_s is the surface potential; l_{ext} is the total roll-off distance for a Gaussian doping profile that decreases from a level at two third of the maximum N_{dmax} to N_{sub}; W_{dep} is the lateral depletion region width obtained from the Poisson equation and Gauss Law from the maximum electrical field, E_{max}, which is in turn, is obtained from a numerical simulation; the effective mobility in the accumulation layer is modeled by a universal accumulation layer carrier mobility model [7].

The spreading resistance R_{sp} is evaluated by integrating the local resistivity over a region where the carriers spread into the junction bulk as the surface conduction reduces. The spreading angle is determined by the junction geometry and inversion layer thickness [8]. The results in Fig.2 show that R_{sp} is much less compared to R_{acc2} which therefore dominates the FILOX-t_{ox} region. In the FILOX region, the sheet resistance dominates. At the contact, the majority of the carriers flow into the metal at its edge rather than through the entire contact area [9]. Fig.2 also shows that the total series resistance is dominated by R_{acc1} and consequently shows the same gate bias dependence. This means that the device exhibits a smaller series resistance at high gate bias. *

In order to significantly reduce R_{acc1}, we identify three key process parameters namely average junction doping density, FILOX thickness encroachment and junction abruptness. Significantly, these parameters are different at the top and bottom of the vertical pillar as are the respective influences of the gate bias dependence and other asymmetric effects. FILOX tends to encroach more towards the junction boundary position at the pillar bottom for this case. The doping profile at the junction border also differs for the drain and the source due to differing dopant diffusion for vertical and lateral directions. Additionally, the distance between the drain contact edge and the vertical pillar surface also influences the drain resistance, R_d by affecting the current spreading position that in turn influences the R_{acc1} and R_{sp}.

4. Series Resistance Extraction

Many methods of extracting the combined series resistance (R_d=R_s) from DC measurements have been reported and summarized in [10]. In these methods, an array of differing channel lengths, L are required and significant errors can be introduced for small values of L. A few DC methods [11, 12] have extracted R_d/R_s separately taking account of its gate bias dependence using a single transistor, which is suitable for the case of vertical MOSTs with a small range of Ls. However, these methods require accurate determination of L_{eff} and complex calculations. In order to avoid all the aforementioned disadvantages, in this work we extract the series resistances from impedances of a MOSFET two port system [13]. During the extraction, the device is biased in the strong inversion region with V_{ds}=0V where the transadmittances and intrinsic gate-substrate capacitance, C_{gbi} can be neglected. Additionally, the series resistances are extracted in the small signal test regime over a frequency range from 0.1GHz to 3GHz such that the impedances of junction-bulk capacitances can be neglected. The suitability of this frequency range for extraction is shown by the plot of resistances versus frequency in Fig.3. The extracted results of R_s against V_{gs} are illustrated in Fig.4 where the values are compared to the analytical model. The device fabrication process included a 0^o tilt source/drain arsenic implant and a 40s RTA at

* The detailed analytical model will be described in the presentation

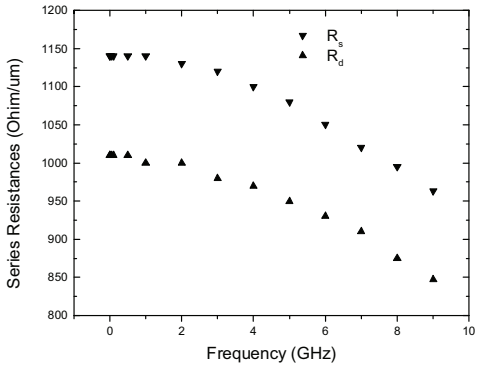

Fig.3 R_d & R_s vs. frequency, FILOX=40nm, 0^o S/D implant, 40s RTA, V_{gs}=1V, V_{ds}=0V

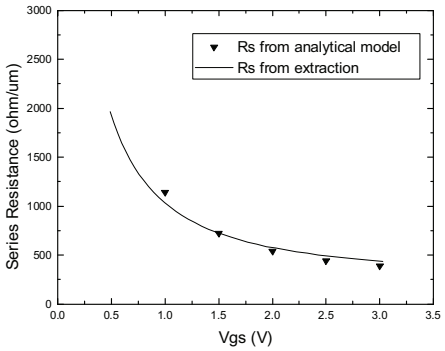

Fig.4 R_s vs. V_{gs}, FILOX=40nm, 0^o S/D implant, 40s RTA, V_{ds}=0V

1100°C.

To clarify the influence of FILOX thickness on the series resistance, we carried out extraction of R_d and R_s from simulation for the devices with FILOX thicknesses from 20nm to 60nm. The results are illustrated and compared in Fig.5 which shows that series resistances experience a dramatic increase when FILOX thickness increases from 50nm to 60nm. For a 60nm FILOX, the analytical model indicates that the dramatic increase of R_s is due to reduction of the junction doping level by thicker FILOX and its encroachment that has thickened the oxide above R_{acc1}. Simulation has confirmed that the thickness of this oxide varies between 6nm to 20nm along the for the bottom junction. For the top junction with thicker FILOX, the resistance is increased due to junction doping level reduction only. Relatively less increase of R_d compared to R_s is because of much reduced FILOX encroachment into the oxide above R_{acc1}.

The devices with thinner FILOX show much less variation in series resistances. The variation is mainly caused by varying junction doping level and junction abruptness for devices with different FILOX thicknesses. The small differences also indicate that for these devices, less asymmetry between R_s and R_d is due to significantly less FILOX encroachment into the sidewall near the bottom and top junction boundary, resulting in less variation of R_{acc1}. Reducing the distance between the top contact edge and the sidewall by 50nm in the top junction, causes

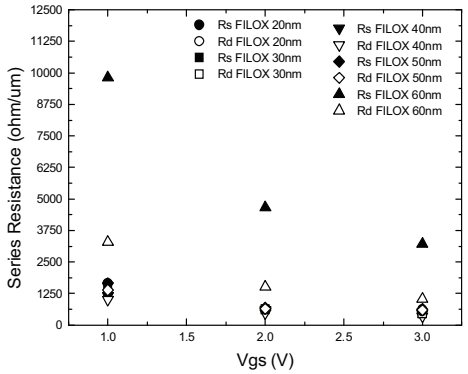

Fig.5 R_d, R_s vs. V_{gs}, 0^o S/D implant, 40s RTA, V_{ds}=0V

an 11%increase in R_d.

The f_T and I_{on} for all the devices at V_{ds}=V_{gs}=1.0V are shown in Fig.6. It can be seen that f_T increases with increase of FILOX thickness up to 40nm and f_T starts to fall thereafter. The increase of f_T is due to the effect of decreasing overlap capacitance; the extracted total overlap capacitance values are listed in table.1 where a reduction with FILOX thickness can be seen. The decrease of f_T beyond 40nm of FILOX is a result of the dominance of series resistance which limits I_{on} and hence the transonductance, g_m. Therefore an optimal FILOX thickness of 40nm is proposed for vMOSTs for a maximized f_T performance.

A comparison among the series resistances from varied tilt angle of source/drain implantation and RTA process conditions is made and shown in Fig.6 where the RTA temperature remains at 1100°C for all the cases. The results for V_{gs}=2V are listed in table 2. We observe that for a 40nm FILOX either 40 second RTA or 15 degree implantation is a necessary process step to extend the junction around the bottom corner and further into the pillar to avoid compromise of series resistance by FILOX encroachment. This is further assisted by using higher implantation energy that additionally increases the overall junction doping

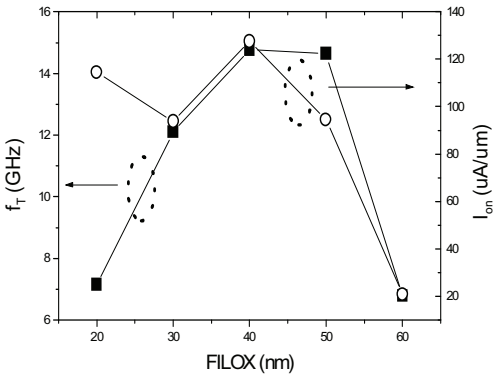

Fig.6 I_{on}, f_T vs. FILOX thickness; V_{ds}=V_{gs}=1.0 V

Table.1 Overlap Capacitance vs. FILOX thickness

t_{FILOX} (nm)	20	30	40	50	60
$C_{overlap}$ (fF/um^2)	3.96	3.76	3.15	2.94	1.88

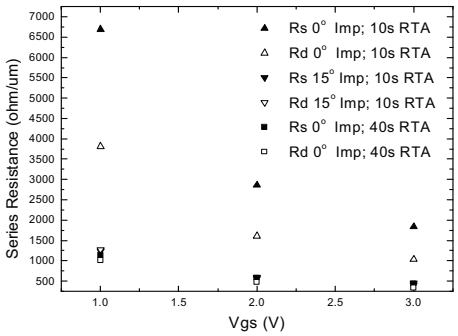

Fig.6 R_d, R_s vs. V_{gs} for cases of a) 0 degree s/d implant, RTA=10s; b) 15 degree s/d implant, RTA=10s; c) 0 degree s/d implant, RTA=40s; all with FILOX=40nm, V_{ds}=0V

Table.2 R_d, R_s vs tilt angle, RTA time with V_{gs}=2V

Tilt Angle (°)	RTA time (s)	R_s (Ω/μm)	R_d(Ω/μm)
0	10	2860	1610
15	10	589	562
0	40	581	479

level. However, this is not true when the energy becomes too high that the peak of doping moves away from the surface of the bottom junction. Consequently R_s deteriorates due to a reduced surface doping and less junction extension. In this case the short channel effect also becomes more severe due to a shortened channel length.

5. Conclusions

In this paper, an analytical and simulation study of series resistance components in vMOST-FILOX was presented. The key parameters that influence the R_d and R_s gate bias dependence and asymmetric device aspects were indentified. An impedance-RF method was used to extract R_d and R_s from devices with different FILOX thicknesses. The analytical model allowed insight into the dominant resistance components whereby apart from lowered junction doping level, the FILOX encroachment additionally increases the R_s. An optimal f_T was seen for FILOX thickness of 40nm which represented a trade-off between the dominance of series-R limited I_{on} and the overlap capacitance. Finally the work also suggested that by using longer RTA time and angled tilt arsenic implantation for source/drain, the junction can be extended further away from the FILOX encroachment and the series resistance is efficiently reduced.

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