Scaling Analysis of Nanoelectromechanical Memory Devices

Tasuku Nagami[1]*, Yoshishige Tsuchiya[2,4], Ken Uchida[1,3,4], Hiroshi Mizuta[2,3,4], and Shunri Oda[1,3,4]

[1]*Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, Meguro, Tokyo 152-8552, Japan*
[2]*School of Electronics and Computer Science, University of Southampton, SO17 1BJ Southampton, U.K.*
[3]*Department of Physical Electronics, Tokyo Institute of Technology, Meguro, Tokyo 152-8552, Japan*
[4]*Solution Oriented Research for Science and Technology Program, Japan Science and Technology Agency, Kawaguchi, Saitama 332-0012, Japan*

Received November 30, 2009; revised January 18, 2010; accepted January 24, 2010; published online April 20, 2010

Numerical simulation of electromechanical switching for bistable bridges in non-volatile nanoelectromechanical (NEM) memory devices suggests that performance of memory characteristics enhanced by decreasing suspended floating gate length. By conducting a two-dimensional finite element electromechanical simulation combined with a drift-diffusion analysis, we analyze the electromechanical switching operation of miniaturized structures. By shrinking the NEM floating gate length from 1000 to 100 nm, the switching (set/reset) voltage reduces from 7.2 to 2.8 V, switching time from 63 to 4.6 ns, power consumption from 16.9 to 0.13 fJ. This indicates the advantage of fast and low-power memory characteristics.

DOI: 10.1143/JJAP.49.044304

1. Introduction

Over the past few decades, silicon nanofabrication techniques for very large scale integrated circuit (VLSI) have been developed, and the performance of a complementary metal–oxide–semiconductor (CMOS) circuit has drastically been improved. The development of microfabrication technologies have also enabled the fabrication of micro-electro-mechanical systems (MEMSs) such as cantilever beams and membranes, and their applications to sensors, resonators, and so on.[1,2] In addition, MEMSs have recently been miniaturized to sub-micron/nanoscale, which are called nanoelectromechanical systems (NEMS), whose mechanical and electrical properties have extensively been investigated.[3–6] For example, an oscillation frequency of over 1 GHz has already been reported for a 1.1-μm-long SiC-based beam.[6] Since the operation speed of NEMS increases square inversely proportional to their characteristic lengths, extremely fast NEMS with a switching time close to that of electronic devices may be realized by reducing their dimensions into the 100-nm regime. It may therefore be worthwhile to consider integrating NEMS components into conventional Si devices in order to add new functionality.[7,8]

We have proposed a novel nonvolatile memory device[9] based on the bistable operation[10,11] of a sub-μm-long NEMS structure, combined with nanocrystalline (nc-) Si quantum dots.[12] A basic concept of nonvolatile memory based on the mechanical bistability of a micromachined bridge has been reported.[13] Our NEMS memory features a suspended SiO_2 beam formed in the cavity as a floating gate, which incorporates nc-Si dots for charge storage (Fig. 1). Once an electron is stored in such a small Si nanodot, another electron transfer probability into the dot is strongly reduced owing to the Coulomb blockade effect even at room temperature.[14] The amount of charge in the beam can therefore be determined by the number of nc-Si dots. We use a very high frequency digital plasma process for nc-Si deposition that facilitates the deposition of nc-Si dots of 8 ± 1 nm in diameter.[15,16] The density of the 8 nm nc-Si dots is typically about 10^{11}–10^{12} cm^{-2} in a monolayer. We can control the amount of the nc-Si dots precisely by adjusting the deposition condition. In order to inject electrons into the nc-Si dots, we apply a high voltage to the gate electrode for initialization. Then, the electrons are injected into the nc-Si dots through the sidewalls, or the gate electrode contacts the floating gate and the electrons are injected through the SiO_2 of the floating gate. The beam is buckled either upward or downward, and its both ends are clamped at the cavity sidewalls. When the gate voltage is applied, the charged beam moves in the cavity via electrostatic interactions between electric field in the cavity and the charge stored in the beam. Write/Erase addressing scheme is realized by combination of gate voltage and substrate voltage (Fig. 2). In write/erase operation gate voltage is positive and negative, respectively. Substrate voltage is negative because of n type transistor. So, in write operation, the memory cell applied both gate and substrate voltage switches the state. In erase operation, the memory cell applied only gate voltage switches the state. A positional displacement of the beam changes the surface potential of the metal–oxide–semiconductor field-effect transistor (MOSFET) placed underneath and is therefore sensed as a shift of its threshold voltage. Readout addressing scheme is realized by combination of gate voltage and drain voltage (Fig. 2). The FET is normally off since the stored charge is

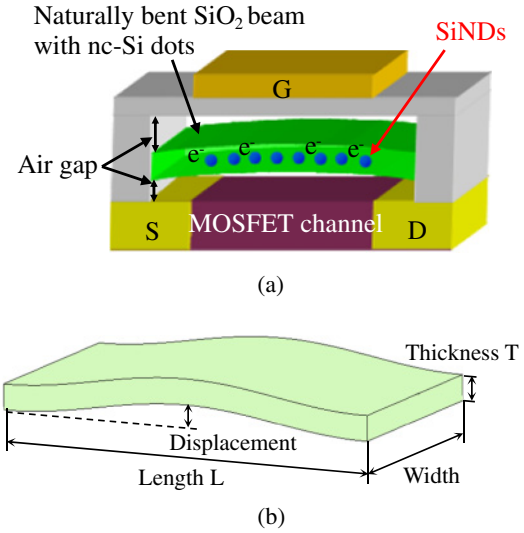

Fig. 1. (Color online) (a) Schematic illustration of a NEMS memory device featuring a buckled floating gate suspended in the cavity above the sense MOSFET. (b) Geometrical parameters of the floating gate.

*E-mail address: nagami@neo.pe.titech.ac.jp

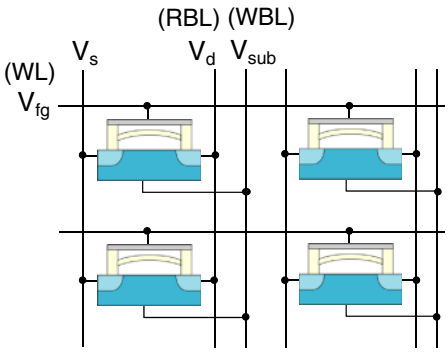

Fig. 2. (Color online) Cell array of the NEMS memory. WL (gate) and RBL (drain) are used for readout selection. WL (gate) and WBL (substrate) are used for write/erase selection.

negative. So, the readout current mainly flows through the memory cell applied both gate and drain voltage. We can obtain the memory state from drain current value. Write and erase operations of the NEMS memory are not associated with charge tunneling via the gate oxide and therefore do not cause any gate oxide deterioration, which limits the endurance cycles of a conventional flash memory. On the other hand we obviously need to quantify the impact of mechanical fatigue of the beam on the endurance cycle for our NEMS memory. However, amorphous SiO_2 that we use to fabricate the beam is supposed to be mechanically robust as demonstrated by a recent experimental study of high-frequency mechanical vibration characteristics of a SiO_2 wire.[17)]

In a past experiment[18)] we fabricated a 3-μm-long free-standing SiO_2 single beam using a Si undercut etching technique. The mechanical bistability of the beam was successfully demonstrated using the nanoindentor loading system.[19)] We also performed a three-dimensional finite element method (FEM) simulation and obtained the switching and readout operations for NEMS memory.[20,21)] However, the length of the floating gate used in ref. 21 was 1 μm. Miniaturization is important for NEMS memory performance and integration. In this study, therefore, we conduct two-dimensional finite element steady-state analysis and transient analysis for miniaturized structures by combining electromechanical simulation and drift-diffusion analysis. We investigate the variations of the switching voltage, on/off current ratio, switching time, and power consumption.

2. Switching Voltage and On/Off Current Ratio

First, we analyzed the electrical readout characteristics for miniaturized structures from theoretical equations before performing a numerical simulation. In past analysis,[21)] we obtained the electric property of the NEMS memory as shown "Original" in Fig. 3(a). We calculated variations of threshold voltage V_t, threshold voltage shift ΔV_t, and switching voltage V_S by using equations below,[20,22)] and predicted the change of the electric characteristic.

$$V_t \sim V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si} q N_A \psi_B}}{C_{g\text{–}sub}} - \frac{\sigma_{fg}}{C_{g\text{–}fg}}, \quad (1)$$

$$\Delta V_t \sim \frac{2\sigma_{fg} Z_0}{\varepsilon_{air}}, \quad (2)$$

$$V_S \propto L^{-4} T Z_0^3 d_{gap} {\sigma_{fg}}^{-1}, \quad (3)$$

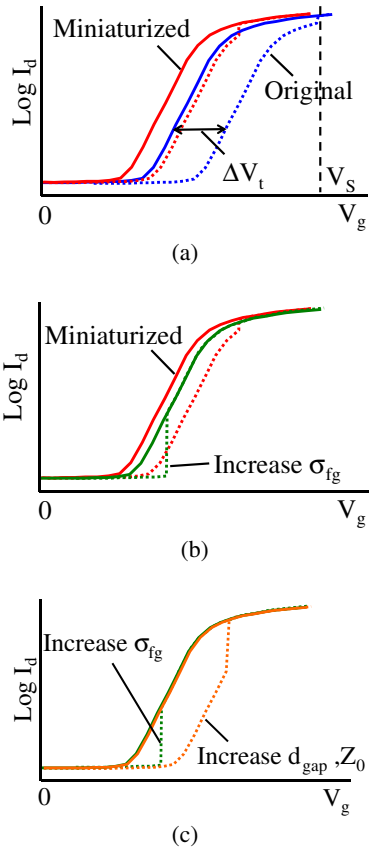

Fig. 3. (Color online) Log I_d vs V_g characteristics for various parameters of floating gate. Dotted line and solid line show off state and on state respectively.

where L is the floating gate length, T the thickness, Z_0 the zero-bias displacement, which is the vertical shift of the beam center relative to its flat position at zero gate bias, and σ_{fg} the stored charge density of the floating gate, ψ_B the Fermi potential (with respect to the intrinsic Fermi potential), N_A the substrate impurity concentration, $C_{g\text{–}sub}$ the capacitance between the gate and the substrate, $C_{g\text{–}fg}$ the capacitance between the gate and the floating gate, and d_{gap} the gap between the gate and the substrate. Shrinking the size by the factor n means the length, the width and the thickness of the floating gate become $1/n$, the doping concentration of the substrate becomes n. From eqs. (1)–(3), if the stored charge density is constant, V_t, ΔV_t, and V_S decrease with miniaturization as shown "Miniaturized" in Fig. 3(a). The reduction of ΔV_t and hence the on/off current ratio by scaling is problematic. In order to recover ΔV_t, σ_{fg} should be increased, which, however, results in the reduction of V_S [Fig. 3(b)]. Then, we adjust d_{gap} and Z_0 so that we obtain sufficient ΔV_t and high on/off current ratio [Fig. 3(c)]. In this way, we varied the floating gate length L between 50 ($n = 20$) and 1500 nm ($n = 0.67$).

In order to analyze NEMS memory characteristics, we should consider the deformation of structures, the electrostatic potential distribution and the carrier transport. So, we solved the Navier's equation, the Poisson's equation and the carrier continuity equation simultaneously. We used the finite element method simulator COMSOL Multiphysics[23)] to solve these equations. Figure 4 shows a schematic model of 1 μm length of the floating gate used for the present

Table I. Scaling factor and structural parameters used for simulation.

Scaling factor n	Floating gate length L (nm)	Air gap d_{air} (nm)	Zero-bias displacement Z_0 (nm)	Internal stress σ_{ox} (MPa)	Stored charge σ_{fg} (C/cm^2)
0.67	1500	35	16.6	350	-4.86×10^{-8}
1	1000	23	13.0	361	-6.40×10^{-8}
2	500	12.5	8.1	382	-1.02×10^{-7}
4	250	7	5.0	411	-1.64×10^{-7}
10	100	4	3.0	512	-3.38×10^{-7}
20	50	3	1.9	557	-4.25×10^{-7}

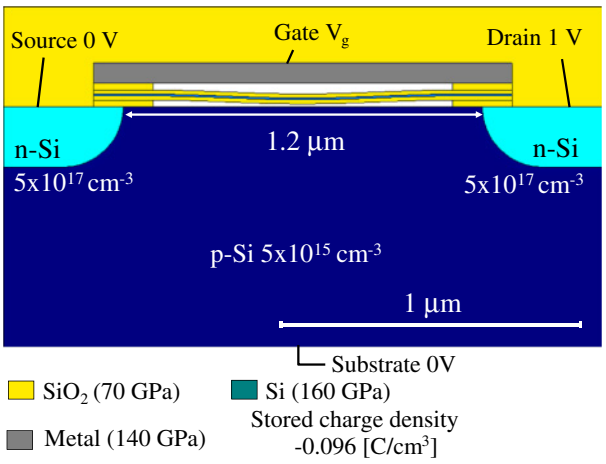

Fig. 4. (Color online) A schematic of model which has 1 µm length of the floating gate.

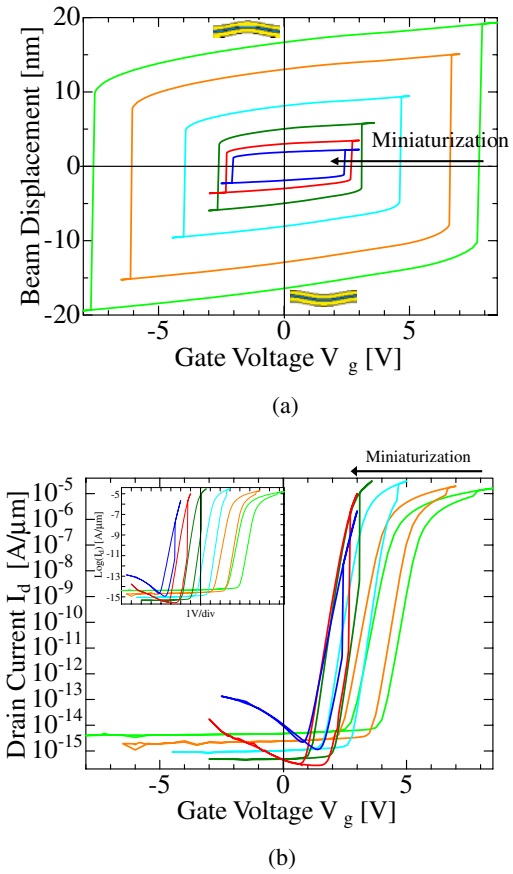

Fig. 5. (Color online) (a) Beam displacement–V_g characteristics and (b) I_d–V_g characteristics for various L between 50–1500 nm. Inset shows I_d–V_g characteristics shifted to negative bias direction. Shift amount increases 1 V per each curve.

simulation. We assumed that the structure is uniform to the direction of the channel width. The floating gate consists of three layers, thermally-oxidized SiO_2, Si, and SiO_2. For simplicity, we used a Si layer instead of the nc-Si dot array layer. The Si layer is harder than the nc-Si dot array layer, so the switching voltage should be observed a bit higher value. Sidewalls and surrounding structure are formed using SiO_2. The electrode was assumed to be chromium. Young's modulus values and Poisson's ratios are 70 GPa and 0.17 for SiO_2, 160 GPa and 0.22 for Si, and 140 GPa and 0.21 for Cr, respectively. The dielectric constants are 4.2 and 11.7 for SiO_2 and Si, respectively. The length and thickness of the floating gate are 1 µm and 33.3 nm, and become $1/n$ with shrinking the size by the factor n. In mechanical simulation, the surrounding area of the structure was assumed to be physically fixed. The internal compressive stress was introduced into the floating gate to take account of the residual stress caused during the thermal oxidization process. In the electrical simulation, the source, drain, and substrate voltage were kept constant to be 1, 0, and 0 V, respectively. The gate voltage was swept. The charge density of the floating gate assumed to be $-0.096\,C/cm^3$ for 1 µm. The substrate region is p-type silicon with the impurity concentration of $5 \times 10^{15}\,cm^{-3}$, and the source and the drain region are n-type silicon with the impurity concentration of $5 \times 10^{17}\,cm^{-3}$. Impurity concentration becomes n with shrinking the size by the factor n. The dependency of electron and hole mobilities on impurity concentration and electric field was taken into account using the Yamaguchi model.[24] The air gap, zero-bias displacement, internal stress value and stored charge density for each miniaturized structure are summarized in Table I. The air gap and zero bias displacement become several nanometers for $L < 250$ nm. These parameters will be difficult to control finely. We should estimate the variability of these parameters and characteristics in future. In this analysis, we investigated the influence of miniaturization for memory characteristics. Under these conditions, we conducted a steady-state analysis and monitored the beam displacement Z and drain current I_d with gate voltage V_g sweeping. As shown in Fig. 5(a), the beam displacement–gate voltage characteristics became smaller hysteresis loops with reducing size. Figure 5(b) shows the drain current–gate voltage

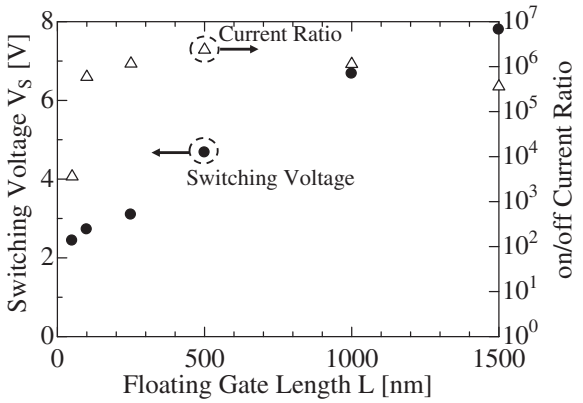

Fig. 6. Dependence of the switching voltage and on/off current ratio on L derived by the steady state calculation.

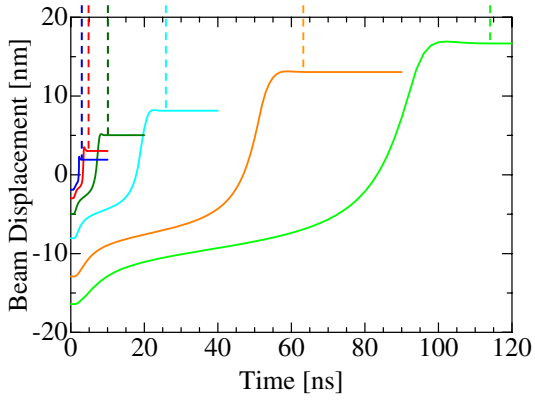

Fig. 7. (Color online) Time evolution of the beam displacement calculated with various floating gate length L between 50–1500 nm.

characteristics for each structure. The hysteresis loops shifted to the left side of the gate voltage axis and changed the shape by shrinking structure. From these results, we summarized the switching voltages and the on/off current ratios in Fig. 6. The switching voltage scales with the floating gate length L from 6.7 V at $L = 1\,\mu$m to 2.7 V at $L = 100$ nm. On the other hand, the on/off current ratio is maintained about 10^5–10^6 until $L = 100$ nm. However, the on/off current ratio reduced to 10^3 for $L = 50$ nm, which suggests the scaling limit in the present device structure.

3. Switching Time and Power Consumption

Next we investigated the transient characteristics of the switching operation. For evaluating the switching speed of our NEMS memory, we need two/three-dimensional (2D/3D) transient analysis which takes account of damping phenomena after the bridge switched to its ON/OFF states.[25] We performed transient analysis by solving the equation of motion including the damping parameter in the context of 2D FEM calculation. Then, time evolution of the beam displacement after stepwise loading pulsed voltage on the beam was calculated. Mechanical damping factor is essential parameter for transient response analysis. However, we did not have information about the damping parameter for NEMS memory. So, we calculated the transient responses with applying step voltage by varying the damping parameter to find the critical damping. In this way, we obtained the switching time in ideal damping condition. Figure 7 shows time evolution of the beam displacement for each structure. Here, we defined the switching time as the transient response time for beam displacement to reach steady state value. We summarized the switching times and applied voltages in Fig. 8. The variation of the switching voltage is the same trend but a bit higher than that of Fig. 6, because we used a bit higher voltage pulse to optimize the transient characteristics. The switching time scales with the length and became about 4.6 ns at $L = 100$ nm with the switching voltage of 2.8 V.

In order to estimate the power consumption of the NEMS memory switching, we also calculated energy required for the switching by summing elastic energy E_m, kinetic energy E_k, damping loss E_d, electrostatic energy E_e, and charging loss E_R. Each energy value is calculated by

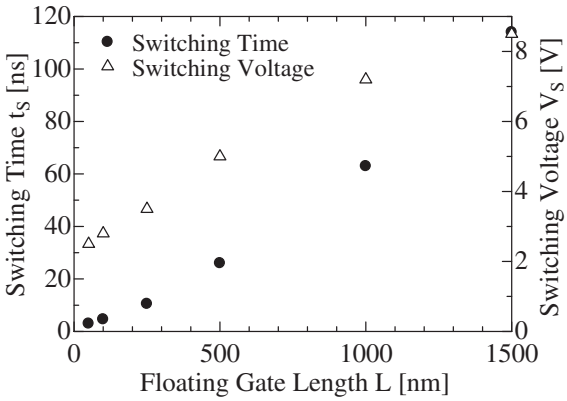

Fig. 8. Dependence of the switching voltage and the switching time on L derived by dynamic calculation.

$$
\begin{aligned}
E_m &= \int_V \frac{1}{2}\,\boldsymbol{\varepsilon}\cdot\boldsymbol{\sigma}\,dV,\\
E_k &= \int_V \frac{1}{2}\,\rho\mathbf{v}^2\,dV,\\
E_e &= \int_V \frac{1}{2}\,\mathbf{E}\cdot\mathbf{D}\,dV,\\
E_d &= \int_V \int_0^t \mathbf{F}_d\cdot\mathbf{v}\,dt'\,dV,\\
E_R &= \int_0^t |dE_e(t')|\,dt',
\end{aligned}
\tag{4}
$$

where $\boldsymbol{\varepsilon}$ is the strain, $\boldsymbol{\sigma}$ the stress, ρ the mass density, $\mathbf{v}$ the velocity, $\mathbf{E}$ the electric field, $\mathbf{D}$ the electric displacement, and $\mathbf{F}_d$ the mechanical damping force. Figure 9 shows transient response of energy variation as each energy is zero at $t = 0$. Variations of E_e and E_R were dominant in total energy variation. Here, we defined the switching energy as difference of energy between before and after switching. The switching energy is 16.9 fJ for $L = 1\,\mu$m. We also calculated the switching energy for other miniaturized structures (Fig. 10). The switching energy scales as the square of the scaling factor, and is 0.13 fJ for $L = 100$ nm.

4. Conclusions

The switching voltage, on/off current ratio, switching time, and power consumption for miniaturized NEMS memory

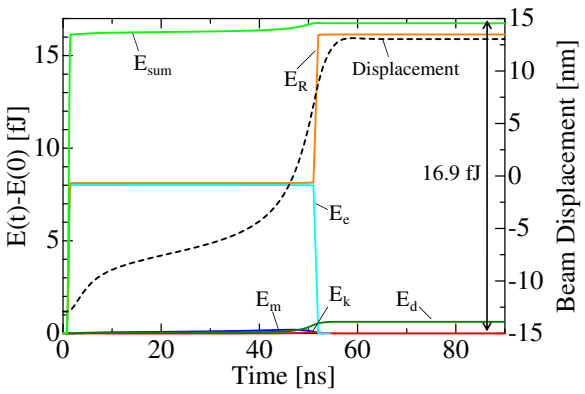

Fig. 9. (Color online) Time evolution of the energy variation for the floating gate length of 1 μm. E_{sum} represent sum of E_m, E_k, E_d, E_e, and E_R.

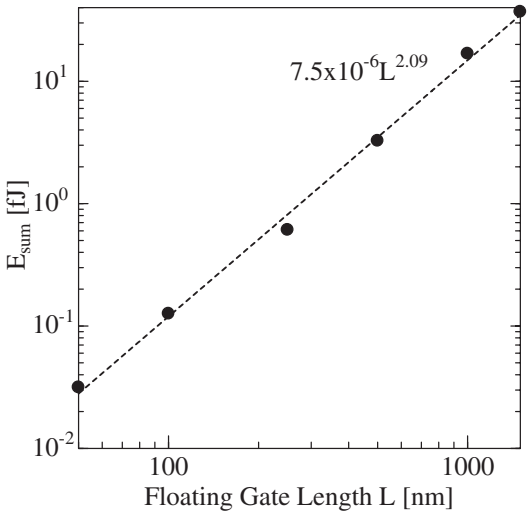

Fig. 10. Dependence of the total energy variation on L derived by dynamic calculation.

structures were investigated by 2D hybrid FEM simulation in which structural analysis, electrostatic analysis, and carrier transport analysis were performed simultaneously. Memory performances enhance with decreasing suspended floating gate length L from 1 μm to 100 nm, where switching voltage of 2.8 V, switching speed of 4.6 ns, and switching energy of 0.13 fJ are projected. However, at 50 nm, memory window collapses in this device structure. Although not suitable for ultralarge scale integration, the fast and ultra low power NEMS memory may find suitable application in mobile terminals.

Acknowledgement

This work was partly supported by Global COE Program, "Photonics Integration-Core Electronics", the Ministry of Education, Culture, Sports, Science and Technology, Japan.

1) A. N. Cleland and M. L. Roukes: Appl. Phys. Lett. **69** (1996) 2653.
2) J. B. Sampsell: J. Vac. Sci. Technol. B **12** (1994) 3242.
3) H. Fujii, S. Kanemaru, T. Matsukawa, and J. Itoh: Appl. Phys. Lett. **75** (1999) 3986.
4) A. Tilke, L. Pescini, A. Erbe, H. Lorenz, and R. H. Blick: Nanotechnology **13** (2002) 491.
5) R. H. Blick, A. Erbe, L. Pescini, A. Kraus, D. V. Scheible, F. W. Beil, E. Hoehberger, A. Hoerner, J. Kirschbaum, H. Lorenz, and J. P. Kotthaus: J. Phys.: Condens. Matter **14** (2002) R905.
6) X. M. H. Huang, C. A. Zorman, M. Mehrengany, and M. L. Roukes: Nature **421** (2003) 496.
7) N. Abelé, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu: IEDM Tech. Dig., 2005, p. 479.
8) N. Abelé, V. Pott, K. Boucart, F. Casset, K. Séguéni, P. Ancey, and A. M. Ionescu: Electron. Lett. **41** (2005) 242.
9) Y. Tsuchiya, K. Takai, N. Momo, S. Yamaguchi, T. Shimada, S. Koyama, K. Takashima, Y. Higo, H. Mizuta, and S. Oda: Proc. IEEE Silicon Nanoelectronics Workshop, 2004, p. 101.
10) M. T. A. Saif: J. Microelectromech. Syst. **9** (2000) 157.
11) M. Sulfridge, T. Saif, N. Miller, and M. Meinhart: J. Microelectromech. Syst. **13** (2004) 725.
12) S. Oda and M. Otobe: Mater. Res. Soc. Symp. Proc. **358** (1995) 721.
13) B. Hälg: IEEE Trans. Electron Devices **37** (1990) 2230.
14) K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, T. Hashimoto, T. Kobayashi, T. Kure, and K. Seki: Proc. IEEE **87** (1999) 633.
15) T. Ifuku, M. Otobe, A. Itoh, and S. Oda: Jpn. J. Appl. Phys. **36** (1997) L4031.
16) K. Nishiguchi, X. Zhao, and S. Oda: J. Appl. Phys. **92** (2002) 2748.
17) D. A. Dikin, X. Chen, W. Ding, G. Wagner, and R. S. Ruoff: J. Appl. Phys. **93** (2003) 226.
18) Y. Tsuchiya, K. Takai, N. Momo, T. Nagami, S. Yamaguchi, T. Shimada, H. Mizuta, and S. Oda: J. Appl. Phys. **100** (2006) 094306.
19) K. Takashima, Y. Higo, S. Sugiura, and M. Shimojo: Mater. Trans. **42** (2001) 68.
20) T. Nagami, H. Mizuta, N. Momo, Y. Tsuchiya, S. Saito, T. Arai, T. Shimada, and S. Oda: IEEE Trans. Electron Devices **54** (2007) 1132.
21) T. Nagami, Y. Tsuchiya, S. Saito, T. Arai, T. Shimada, H. Mizuta, and S. Oda: Jpn. J. Appl. Phys. **48** (2009) 114502.
22) Y. Taur and T. H. Ning: *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 1998) pp. 88, 119.
23) COMSOL: Multiphysics Modeling and Simulation [http://www.comsol.com/].
24) K. Yamaguchi: IEEE Trans. Electron Devices **30** (1983) 658.
25) M. Sulfridge, T. Saif, N. Miller, and M. Meinhart: J. Microelectromech. Syst. **13** (2004) 725.