

Hybrid Silicon Nanoelectromechanical Devices: Physics and Applications

Hiroshi Mizuta¹, Yoshishige Tsuchiya¹ and Shunri Oda²

¹NANO Group, School of Electronics and Computer Science, University of Southampton,
Southampton SO17 1BJ, U.K., hm2@ecs.soton.ac.uk

²Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, Tokyo, Japan

Silicon VLSI technology developed and matured over the past decades has been fully exploited to build the vast technology area of micro-electromechanical systems (MEMS). Along with a rapid expansion of the MEMS market, there have also been continuous efforts at making the MEMS smaller in order to boost the operating frequency to GHz and beyond. The MEMS technology has already entered a sub- μm regime and proceeds rapidly towards a nanometer-scale regime. The appearance of high-speed nano-electromechanical systems (NEMS) is tempting enough for us to consider the hybridization of the NEMS and conventional silicon electronic devices (*'More than Moore'*) because we expect such hybrid systems enhance scaling of functional density & performance while simultaneously reducing the power dissipation beyond the conventional CMOS-based systems.

A number of new hybrid NEM-CMOS devices have recently been studied for logic, memory and sensing applications. A typical NEM hybrid device is a suspended-gate field-effect transistor (SGFET) which features a movable gate suspended over the MOS channel with an air gap. The SGFETs have attracted an increasing interest thanks to the extremely-abrupt switching with the subthreshold slope much smaller than the theoretical limitation of 60 mV/dec for MOSFETs. As for the memory applications, we proposed two types of novel high-speed and nonvolatile NEM memory devices to go beyond conventional Flash memory. The bistable floating gate (FG) NEM memory features a buckled SiO_2 FG with embedded Si nanodots as single-electron storage. The other one is a suspended gate (SG) Si nanodot memory (SGSNM) (Fig. 1) in which the SG is pulled in to the FG only when we programme and erase the information. As for the sensing applications, a new in-plane resonant NEM sensor has recently been studied based on a mass-detection principle. This nanosensing device features a silicon resonant-suspended-gate and an in-plane MOSFET co-integrated on an ultrathin SOI platform and enables sub-attogram-level mass detection.

By downscaling the NEMS towards a 100-nm-regime and even smaller, we may explore a novel hybrid system of NEMS and single-electron transistors (SETs). A suspended-gate SET is an apparent extension of the SGFETs which is expected to achieve a dramatic modulation of the Coulomb oscillation period. There are, however, lots more new phenomena associated with strong coupling of single-electron tunnelling and low-dimensional phonons, such as phonon blockade and single-electron quantum shuttle, which may be exploited to develop novel *'Beyond CMOS'* information devices. A suspended quantum dot (QD) SET (Fig. 2) is particularly attractive to investigate the interaction between single electrons and phonons confined in suspended QDs. Recent study of the single-electron tunneling current for the double QDs suspended SET reveals the existence of multiple current peaks associated with inelastic tunneling mediated by confined phonons. These results allow envisaging the future possibility of tailoring the electron-phonon interaction in such suspended QDs systems.

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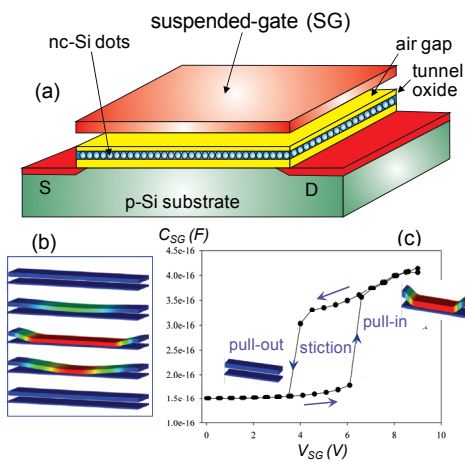


Fig. 1 A schematic SGSNM, SG pull-in/pull-out and hysteresis in the SG - substrate capacitance.

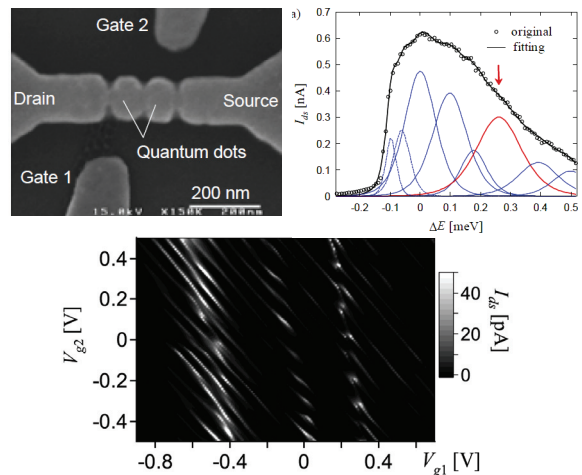


Fig. 2 A suspended DQD-SET, I_{ds} - V_{g1} - V_{g2} curves at 120 mK and current peaks around the charge triple point.