Modeling the Impact of Process Variation on Resistive Bridge Defects

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***Abstract*—Recent research has shown that tests generated without taking process variation into account may lead to loss of test quality. At present there is no efficient device-level modeling technique that models the effect of process variation on resistive bridges. This paper presents a fast and accurate technique to model the effect of process variation on resistive bridge defects. The proposed model is implemented in two stages: firstly, it employs an accurate transistor model (BSIM4) to calculate the critical resistance of a bridge; secondly, the effect of process variation is incorporated in this model by using three transistor parameters: gate length (L), threshold voltage (V_{th}) and effective mobility (μ_{eff}), where each follow Gaussian distribution. Experiments are conducted on a 65-nm gate library (for illustration purposes), and results show that on average the proposed modeling technique is more than 7 times faster and in the worst case, error in bridge critical resistance is 0.8% when compared with HSPICE.**

***Index Terms*—Resistive bridge fault, process variation, fault model, deep-submicron defect.**

I. Introduction

The impact of process variation on integrated circuit performance cannot be ignored due to continuous scaling of CMOS [1]–[3]. Fabrication process variation is mainly due to sub-wavelength lithography, random dopant distribution, line edge roughness and stress engineering [4]–[6]. There is a general consensus in research community that transistor gate length and threshold voltage are the two leading sources of process variation; recently mobility (μ_{eff}) has also emerged as a source of variation due to variation in effective strain in a strained silicon process and should be included in the analysis together with the other two parameters, i.e., L and V_{th} [6]. In a recent study, it has been shown that more than 30% error in the drive current of a transistor is observed on a 65-nm device due to process variation, when compared to a transistor nominal operating conditions [6]. Process variation also has negative effect on the quality of manufacturing test, leading to test escapes as in the case of bridge defects [7].

Resistive bridge fault (RBF) (Fig. 1) represents a major class of defects in deep-submicron CMOS and have received increased attention on modeling, simulation and test generation [8]–[12]. Manufacturing test employs fault models for testing digital circuits, which are meant to emulate the physical behaviour of a defect at device level. Accurate fault models

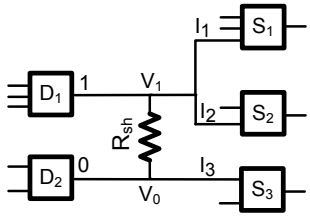

Fig. 1. Resistive Bridge forming potential circuit fault.

are important for fault simulation, test generation and fault diagnosis [13], [14]. Using ISCAS 85, 89 benchmarks and a 45-nm gate library, a recent study has shown that tests generated for nominal scenario without considering process variation can lead to as much as 10% loss of test quality due to additional faults [7].

In nominal operating conditions (without modeling the effect of process variation) available bridge fault modeling techniques can be categorized into two main classes: SPICE-based [12] and Fitted Models [15]. These two models offer a trade-off between speed and accuracy as described in Section III. In this paper, we propose a variation-aware fault modeling technique, which is fast and accurate, when compared with HSPICE. This is achieved by employing a two stage modeling technique. Firstly, the most recent transistor model from Berkeley Short-Channel IGFET Model (BSIM4) is used to determine the critical resistance of a bridge using the I-V_{ds} model of BSIM4 [16]. The BSIM4 transistor model is valid across all operating modes of the transistor and uses accurate models that relate different electrical parameters with device structure and takes into account various inter-dependencies between different transistor parameters, which allows accurate variation-aware modeling. Secondly, the effect of process variation on the critical resistance (of a bridge) is modeled by incorporating fluctuations in three transistor parameters: gate length (L), threshold voltage (V_{th}) and mobility (μ_{eff}) [6]. Temperature and supply voltage is assumed to be fixed, i.e., no variation. The proposed modeling technique can be extended to take into account the effect of supply voltage and temperature variations, as described at the end of Section IV-B. We have analyzed both un-correlated and correlated parameter fluctuations. The un-correlated parameter fluctuations are modeled by considering

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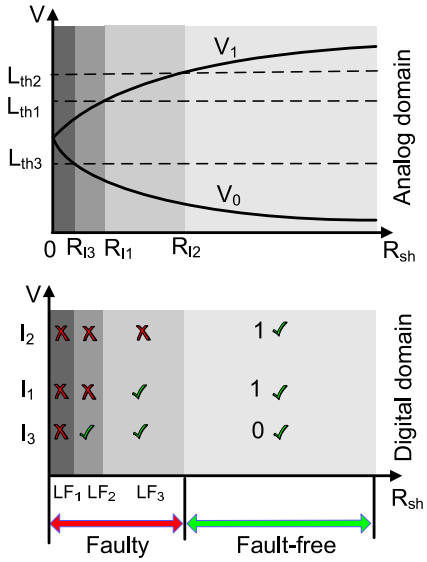

Fig. 2. Bridge fault example and its behaviour in analog and digital domain

these three parameters with Gaussian distribution [6]. The effect of (within-die) spatially correlated parameter fluctuations are modeled by using a correlation co-efficient on transistor gate length (L), which is identified as the major contributor of such variations [17]. Note the parameter fluctuations (correlated or otherwise) do not imply that these parameters are independent, for example as L decreases, V_{th} also decreases, this effect is also known as V_{th} roll-off [16]. Experimental results verify that the proposed technique is efficient when compared to HSPICE results in terms of accuracy and speed.

The paper is organized as follows: Section II gives an overview of resistive bridge defects and describes the change in their behaviour due to process variation leading to test escapes. The available fault modeling techniques and their limitations are discussed in Section III. The proposed variation aware bridge modeling technique is discussed in Section IV. Experimental setup and results are reported in Section V, and finally Section VI concludes the paper.

II. Preliminaries

Due to process variation, the behaviour of a resistive bridge deviates from the one in nominal operating conditions, leading to test escapes. This change in behaviour and its effect on test is briefly described in this section.

A typical bridge fault behavior in nominal scenario is illustrated in Fig. 1 and Fig. 2. Fig. 1 shows a resistive bridge R_{sh}, D_1 and D_2 are the gates driving the bridged nets, while S_1, S_2 and S_3 are the successor gates. Let us assume that the output of D_1 is driven high and the output of D_2 is driven low. The dependence of the voltage levels on the outputs of D_1 (V_1) and D_2 (V_0) on the equivalent resistance of the physical bridge is shown in Fig. 2 (based on SPICE simulation using 65-nm library). To translate this analog behavior into the digital domain, the input threshold voltage levels L_{th1}, L_{th2} and L_{th3} of the successor gates S_1, S_2 and S_3 have been added to the plot shown in Fig. 2. The logic threshold of a gate input is defined as the input voltage at which the output reaches half of the supply voltage, while other inputs of the gate are at non-controlling value(s) [18]. For each value of the bridge resistance $R_{sh} \in [0, \infty)$, the logic values read by inputs I_1, I_2 and I_3 can be determined by comparing V_1 and V_0 with the input threshold voltage of the corresponding input. These values are shown in the second part of Fig. 2 (marked as "digital domain"). Crosses are used to mark the faulty logic values and ticks to mark the correct ones. It can be seen that, for bridges with $R_{sh} > R_{I2}$, the logic behavior at the fault site is fault-free (all inputs read the correct value), while for bridges with R_{sh} between 0 and R_{I2}, one or more of the successor inputs are reading a faulty logic value. A number of bridge resistance intervals can be identified based on the corresponding logic behavior. For example, bridges with $R_{sh} \in [0, R_{I3}]$ exhibit the same faulty behavior in the digital domain (all successor inputs read the faulty logic value), similarly, for bridges with $R_{sh} \in [R_{I3}, R_{I1}]$, successor gates S_1 and S_2 reads the faulty value, while S_3 reads the correct value. For the resistance range $R_{sh} \in [R_{I1}, R_{I2}]$, all successor gates other than S_2 read the correct logic value, and finally for $R_{sh} > R_{I2}$ all the successor gates read the correct logic value. Consequently, each interval $[R_a, R_{a+1}]$ corresponds to a distinct logic behavior occurring at the bridge fault site. The R_{sh} value corresponding to R_{I2} is normally referred to as "critical resistance" (R_{crit}), as it represents the crossing point between faulty and correct logic behavior. Methods for determining the critical resistance have been presented in several publications [19], [11]. The value of critical resistance of a bridge has time-dependency, i.e., it is different for static test and dynamic test; the proposed model is developed for static test. These distinct logic behaviors at the bridge fault site are referred to as *Logic Faults*, where each individual logic fault comprises of the following variables: boolean input to the driving gates, boolean values interpreted by the driven inputs of the successor gates (I_1, I_2 and I_3, as in Fig. 1) and the covered resistance range of the bridge R_{sh}. Fig. 2 shows three logic faults (marked as "LF_1", "LF_2" and "LF_3") corresponding to distinct logic behaviours occurring at the bridge fault-site. The

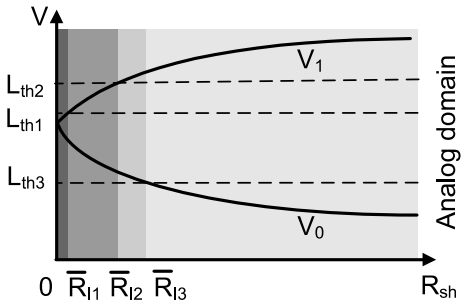

Fig. 3. Change in drive current (due to process variation) from the behaviour shown in Fig. 2 leading to test escapes.

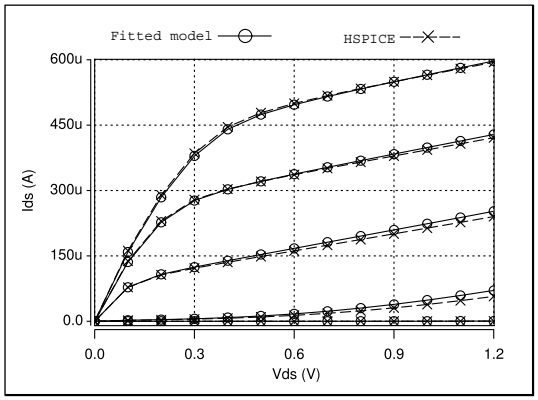

Fig. 4. Nominal operating conditions: HSPICE and Fitted Model.

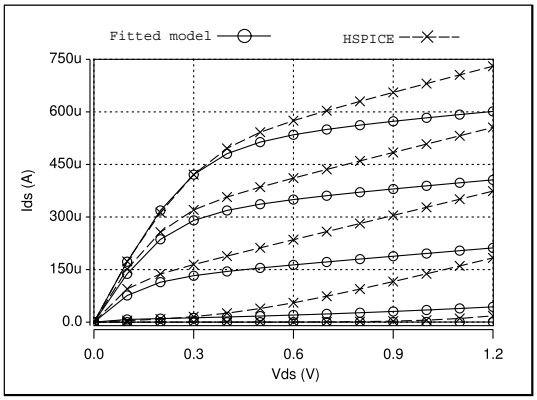

Fig. 5. Effect of gate length variation: HSPICE and Fitted Model.

fault domain of a bridge fault-site comprises of the union of individual logic faults.

Due to process variation, the behaviour of the resistive bridge deviates from the nominal scenario (Fig. 2). It affects two important parameters, i.e., drive current of driving gates (D_1 and D_2) and and logic threshold voltages of the driven gates (S_1, S_2 and S_3) [7]. The change in these two parameters may introduce additional logic faults resulting in expanding the fault domain of a bridge fault-site.

These two parameters are examined individually to clearly illustrate the impact of their change, however in practice (and in all the experiments reported in this paper) these two parameters vary together and exhibit commulative effect. First, we illustrate the effect of drive current variation of the driving gates, while keeping the original logic threshold voltages of the driven gates. This is shown in Fig. 3, which shows an increase in the voltages on the two nets (V_1 and V_0 for the same value of R_{sh}) and change in the covered resistance range. It can be seen that in comparison to the nominal scenario shown in Fig. 2, the critical resistance has changed as $R_{sh} \in [\bar{R}_{I2}, \bar{R}_{I3}]$ now covers the maximum resistance range. From test generation point of view, a test generated to propagate the fault effect through I_2 (gate S_2 as in the case of nominal scenario) will lead to a test escape, as $R_{sh} \in [\bar{R}_{I2}, \bar{R}_{I3}]$ will be missed. Therefore in this case, an additional test is needed to propagate the fault effect through I_3 (gate S_3) to cover the new logic fault, added to the fault domain. Similarly, the change in logic threshold voltage of the driven gates also leads to test escapes as demonstrated in [20].

III. Analysis of available modeling techniques

This section examines the available device-level fault models for resistive bridge defects and their limitations in modeling the effect of process variation. In general, the available fault models (in nominal operating conditions) can be categorized into two: SPICE-based [7] and Fitted Models [15]. These two models offer a trade-off between speed and accuracy. SPICE-based Models offer high accuracy at the expense of long simulation time and the Fitted Models offer very fast computation time but are less accurate than SPICE-based Models.

The only investigation, we are aware of, that integrates the effect of process variation in a resistive bridge model is reported in [7], [20]. It uses a SPICE-based Model, and to integrate the effect of process variation, it uses the following four transistor parameters: threshold voltage (V_{th}), width (W), length (L) and oxide thickness (T_{ox}). These parameters are assumed to be statistically independent and are varied by Gaussian distribution with a standard deviation of approximately 10% of mean value. The experiments are conducted on a 45-nm gate library with Predictive Technology Model (PTM) transistor models [21]. For each bridge fault-site, it uses SPICE simulation to determine the voltages (V_1 and V_0 as in Fig. 1) at discrete bridge resistance intervals and stores the outcome in a database for subsequent use. The nominal values of V_1 and V_0 are then used to generate new set of variation-induced logic faults by Monte-Carlo simulation and for this purpose the four parameters are varied through 500 permutations to generate a new set of variation-induced logic faults (Fig. 3). This method has two limitations: Firstly, when scaling from one technology node to another, the database (with SPICE information) needs to be re-generated, as that is technology-specific; Secondly, the database generation (per technology node) requires long computation time. A recent study has reported that it took nearly a week with 8 computers working in parallel to generate a database for ISCAS 85, 89 benchmarks [20].

The database generation can be avoided by calculating the critical resistance of a bridge by using I-V_{ds} based electrical equation of a Shockley transistor model [9]. Since Shockley model is a simple transistor model [22], [23], curve fitting is used to match the results with SPICE data, leading to what is called a "Fitted Model", which uses additional co-efficients to achieve higher accuracy than Shockley model [15], [24]. The Fitted Model is intended for nominal operating conditions and only 0.4% worst-case error is reported when compared with SPICE results on a 0.35μm gate library [15]. When considering the effect of process variation, the problem with the Fitted Model is that of accuracy, i.e., the percentage of

error increases as process variation is introduced. To study the effect of process variation on the Fitted Model, we also used the I-V$_{ds}$ equation of the Shockley model and a 65-nm PTM transistor model card [21]. We first fitted the I-V$_{ds}$ model using HSPICE simulation results in nominal operating conditions, and the results are shown in Fig. 4, these plots are generated by increasing V$_{gs}$ from 0-V to 1.2-V with a step size of 0.3-V. It can be seen that the Fitted Model matches well with that of HSPICE in nominal operating conditions. Next, we introduced the effect of process variation by varying the transistor gate length by 5-nm (for illustration purposes) and re-generated the plots using HSPICE and the Fitted Model. The result is shown in Fig. 5, as can be seen the Fitted Model deviates from HSPICE simulated results. This is because, the Fitted Model uses a simple Shockley transistor model, which does not take the effect of process variation into account, leading to inaccurate results. To improve its accuracy, additional models that relate the inter-dependencies between different transistor parameters are needed [25]. For example, scaling of the gate length results in reducing V$_{th}$, while increasing subthreshold swing and Drain Induced Barrier Lowering (DIBL). Therefore to accurately model the impact of process variation, more accurate transistor models should be used to relate different electrical parameters with the device structure. This means that curve fitting at nominal operating conditions using a simple (Shockley) transistor model and SPICE simulation data can not be extended to accurately model the effect of process variation in deep-submicron devices.

IV. Variation-aware Modeling Technique

From the discussion in the previous section, it is observed that the available modeling techniques for resistive bridges are either time consuming or can not be used (as such) to model the effect of process variation on resistive bridges. It gives motivation to develop a process variation-aware modeling technique that is fast and accurate. This is achieved by employing a two stage modeling technique. Firstly, the most recent transistor model (BSIM4) is used to determine the critical resistance of a bridge using the I-V$_{ds}$ model of BSIM4. This I-V$_{ds}$ model requires approximating the V$_{ds}$ voltage across the transistors driving the bridge. The BSIM4 model and the approximation method to determine the critical resistance of a bridge is described in Section IV-A. Secondly, the effect of process variation on the critical resistance (of a bridge) is modeled by integrating fluctuations in three parameters (L, V$_{th}$ and μ_{eff}) [6], [17], as described in Section IV-B.

A. Bridge Critical Resistance Calculation using BSIM4

The critical resistance of a bridge is calculated by using the BSIM4 (BSIM4.6.4) transistor model, which is valid across all operating (active and saturation) regions. It accurately relates different electrical parameters with device structure and takes into account various inter-dependencies between different transistor parameters, it is therefore well-suited to model the effect of process variations [16]. The following equation models the I-V$_{ds}$ characteristics of an NMOS transistor:

$$I_{ds} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} \cdot I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm}} ln\left(\frac{V_A}{V_{Asat}}\right)\right] \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \quad (1)$$

where, I_{ds} is the drain current equation for both linear and saturation regions, I_{ds0} is the drain current valid from the subthreshold to the strong inversion regime and is given by Eq. (2), NF is the number of device fingers, R_{ds} is the source/drain resistance, V_{ds} is the source/drain voltage, V_{dseff} is the effective V$_{ds}$, C_{clm} is the channel length modulation, V_A is the Early voltage, V_{Asat} is the Early voltage at $V_{ds} = V_{dsat}$, V_{ADIBL} is the Early voltage due to Drain Induced Barrier Lowering (DIBL), V_{ADITS} is the Early voltage due to Drain Induced Threshold Shift (DITS), V_{ASCBE} is the Early voltage due to substrate current induced body effect (SCBE).

$$I_{ds0} = \frac{W \mu_{eff} Q_{ch0} V_{ds} \left(1 - \frac{V_{ds}}{2V_b}\right)}{L \left(1 + \frac{V_{ds}}{E_{sat} L}\right)} \quad (2)$$

where, μ_{eff} is the effective mobility of the carriers, Q_{ch0} is the channel charge density, V_b is given by $\frac{(V_{gsteff} + 2v_t)}{A_{bulk}}$, V_{gsteff} is the effective $(V_{gs} - V_{th})$, v_t is the thermal voltage, A_{bulk} models the bulk charge effect, E_{sat} is the critical electric field at saturated carrier velocity.

The above two equations can be solved using the device parameters (per transistor) through a transistor model card (for example, PTM [21]) and the variables (for example, C_{clm}, V_{ADIBL}, V_{ADITS} etc) of Eq. (1) and Eq. (2) are obtained from the BSIM4 transistor model equations [16]. These equations are used to calculate the critical resistance of a bridge defect and have been validated by comparing the results with HSPICE using 65-nm PTM model card [21].

Next, we explain the V$_{ds}$ approximation method for critical resistance calculation by using the algorithm shown in Fig. 7 for both NMOS and PMOS transistors. The fault-site shown in Fig. 6-(a) is used as an example, where two inverters are driving the bridge (R$_{sh}$), I$_0$ is the current through the resistor. The value of R_{sh} can be calculated by the following expression:

$$R_{sh} = \frac{(V_1 - V_0)}{I_0} \quad (3)$$

Using the logic threshold voltage (L$_{thA}$, obtained through HSPICE simulation) of the driven gate "A" (Fig. 6), V_1 is L_{thA}, which can be used to calculate I$_0$ through the I-V$_{ds}$ relationship shown in Eq. (1), i.e., $I_0 = I_p(V_{ds,p})$, where $V_{ds,p} = L_{thA} - V_{dd}$. The only unknown variable left in

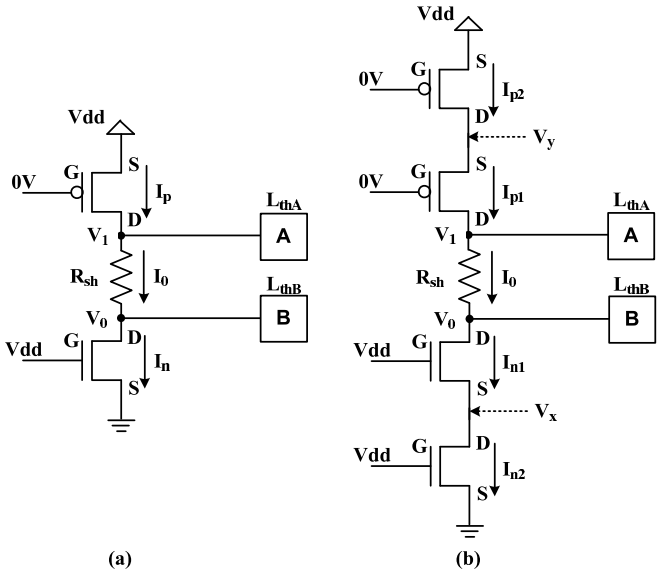

Fig. 6. Bridge resistance examples: (a) A fault-site driven by two inverters; (b) A fault-site driven by 2-input NOR and 2-input NAND.

Eq. (3) is V_0, which can be approximated by using the algorithm shown in Fig. 7 (since $I_0 = I_n(V_0)$, which implies $V_0 = I_n^{-1}(I_0)$). In Fig. 7 the value of V_0 is gradually incremented (step-6) until the relative difference of I_0 and I_n (I_n is represented by I_{tmp}) is smaller than the specified limit, as determined by step-8 of the algorithm. The value of V_0 is then used together with the other two variables (V_1 and I_0) to calculate R_{sh} using Eq. (3). The same procedure can be repeated for PMOS transistor, starting with the value of V_0 as the logic threshold of gate "B", i.e., L_{thB}. In case of transistors in parallel, the effective $\frac{W}{L}$ is calculated before starting the algorithm.

Next, we show how to approximate the value of I_0 in the case where two transistors are in series (Fig. 6-(b)). In this case, R_{sh} (Eq. (3)) is calculated starting with the logic threshold voltage of gate "B", i.e., $V_0 = L_{thB}$. V_0 is used to calculate I_0 using the algorithm shown in Fig. 8 for (NMOS or PMOS) transistors in series. It can be seen that the currents through the two NMOS transistors (I_{n1} and I_{n2}) are calculated by approximating the value of V_x, starting with $\frac{V_0}{2}$ as shown in step-3. This is used to generate the intermediate values of I_0, which further improve the approximation of V_x (step-8). This process is repeated until the difference in I_{n1} and I_{n2} is smaller than 1μA, which usually requires very small (5 or less) number of iterations. The difference of less than 1μA provides a close approximation of I-V_{ds} when compared with the HSPICE results. The value of I_0 is then used to calculate V_1 using the algorithm (Fig. 7). Finally, all three variables (V_0, V_1 and I_0) are used to calculate R_{sh} using Eq. (3). A similar algorithm is used for PMOS transistors (in series, by step-11 to step-17). It can be extended to calculate I_0 for more than 2 transistors in series, for example in case of 3 transistors, step-3 is changed with $\frac{V_0}{3}$ and approximating

Input: I_0
Output: V_0 or V_1
1: Read the PTM model card.
// Model card is needed for parameters in Eq. (1)
2: V_{tmp} = 0, STEP = 0.0005
3: I_{tmp} = 0, LIMIT = 0.005
// The values of LIMIT and STEP are chosen after
// detailed analysis.
4: **if** NMOS **then**
5: **repeat**
6: V_{tmp} = V_{tmp} + STEP
7: I_{tmp} = $I_n(V_{tmp})$; with $V_{bs} = 0$ and $V_{gs} = V_{dd}$
// I_{tmp} is calculated by using Eq. (1)
8: **until** $\left[\frac{|I_0 - I_{tmp}|}{I_0} \geq LIMIT\right]$
9: **return** (V_{tmp})
// $V_0 = V_{tmp}$
10: **else**
11: **repeat**
12: V_{tmp} = V_{tmp} - STEP
13: I_{tmp} = $I_p(V_{tmp})$; with $V_{bs} = 0$ and $V_{gs} = -V_{dd}$
// I_{tmp} is calculated by using Eq. (1)
14: **until** $\left[\frac{|I_0 - I_{tmp}|}{I_0} \geq LIMIT\right]$
15: **return** $(V_{dd} + V_{tmp})$
// $V_1 = V_{dd} + V_{tmp}$
16: **end if**

Fig. 7. V_{ds} approximation algorithm for N/P transistor.

currents through each transistor i.e., I_{n1}, I_{n2} and I_{n3} using their respective V_{ds} voltages to calculate the value of I_0. Note that previously [15] has used Eq. (2) and a V_{ds} approximation method to calculate the critical resistance of a bridge in normal operating conditions, but that work does not include the effect of process variation, which is described next.

B. Incorporation of Process Parameter Variation

We first explain process variation modeling by using mutually independent parameter fluctuations (without spatial correlation) followed by a description of modeling within-die spatial correlation effects. A recent study describes the parameter extraction technique (for process variation) using a 65-nm CMOS library with a PTM model [6], [21]. Three transistor parameters are recognized as the leading sources of process variation, which include: gate length (L), threshold voltage (V_{th}), and mobility[1] (μ_{eff}). These parameters follow Gaussian distribution with standard deviations of 4% for L, 5% for V_{th} and 21% for μ_{eff}. Negligible spatial correlation is found in between these parameters, i.e., they can be treated as independent random variables following Gaussian distribution.

[1]Mobility varies due to variation in effective strain in a strained silicon process [6].

Input: V_0 or V_1
Output: I_0

Read the PTM model card.
// Model card is needed for parameters in Eq. (1)
if NMOS **then**
  V_x = $\frac{V_0}{2}$
  // Fig. 6-(b) shows V_x
  repeat
    $I_{n1} = I_n(V_0 - V_x)$;
    with $V_{bs} = -V_x$ and $V_{gs} = V_{dd} - V_x$
    $I_{n2} = I_n(V_x)$; with $V_{bs} = 0V$ and $V_{gs} = V_{dd}$
    // I_{n1} and I_{n2} are calculated by using Eq. (1)
    I_0 = $\frac{(I_{n1}+I_{n2})}{2}$
    V_x = $I_n^{-1}(I_0)$; with $V_{bs} = 0V$ and $V_{gs} = V_{dd}$
    // Using Algorithm shown in Fig. 7
  until $(|I_{n1} - I_{n2}| \geq 1\mu A)$
else
  V_y = $\frac{(V_1+V_{dd})}{2}$
  // Fig. 6-(b) shows V_y
  repeat
    $I_{p1} = I_p(V_1 - V_y)$;
    with $V_{bs} = V_{dd} - V_y$ and $V_{gs} = -V_y$
    $I_{p2} = I_p(V_y - V_{dd})$; with $V_{bs} = 0V$ and $V_{gs} = -V_{dd}$
    // I_{p1} and I_{p2} are calculated by using Eq. (1)
    I_0 = $\frac{(I_{p1}+I_{p2})}{2}$
    V_y = $I_p^{-1}(I_0)$; with $V_{bs} = 0V$ and $V_{gs} = -V_{dd}$
    // Using Algorithm shown in Fig. 7
  until $(|I_{p1} - I_{p2}| \geq 1\mu A)$
end if
return (I_0)

Fig. 8. I_0 approximation algorithm for two transistor in series.

TABLE I
VARIED PROCESS PARAMETERS

Parameter	Mean (μ)	Std. Deviation (σ)
L	60-nm	±4% (2.4-nm)
V_{thn}	0.423-V	±5% (21.15-mV)
V_{thp}	-0.365-V	±5% (18.25-mV)
μ_{effn}	491 cm^2/V.s	±21% (103.1 cm^2/V.s)
μ_{effp}	57.4 cm^2/V.s	±21% (12.05 cm^2/V.s)

These results are validated by comparing with the measured data using a fabricated device.

Our experiments are based on a ST Microelectronics 65-nm gate library using the same PTM model cards that are used in [6], which is why we have also assumed the same parameter fluctuations. The mean and standard deviation for both NMOS/PMOS transistors are shown in Table I. The calculated standard deviation of V_{th} is also compared with the σV_{th} value using the relationship presented in an earlier publication [26], and only a small difference (around 5-mV) is found for both the NMOS and PMOS transistors.

$$\sigma V_{th} = 3.19 \times 10^{-8} \frac{\left(t_{ox} \cdot N_A^{0.4}\right)}{\sqrt{L_{eff} \cdot W_{eff}}} [V] \quad (4)$$

where, N_A, L_{eff} and W_{eff} are the average channel doping, effective channel length and width respectively.

The effect of within die variations are analysed, by varying only the gate length of different transistors using a spatial correlation model [17]. As pointed out by several publications, gate length is a leading source of process variation and it has shown correlated variation effects due to lithography [27]–[29]. The spatial correlation model that correlates the gate length of different transistors within the same die is given by the following relationship:

$$\rho = \begin{cases} 1 - \frac{x}{X_L}(1 - \rho_B), & x \leq X_L \quad (5) \\ \rho_B, & x \geq X_L \quad (6) \end{cases}$$

where, ρ is the correlation co-efficient that relates the gate length of different transistors, X_L is the correlation length, ρ_B is the correlation baseline and x is the separation between transistors.

Variations in supply voltage and temperature are not considered in this paper. This model can be extended to take into account such variations as well. Eq. (1) can be used to take into account supply voltage variation in a straight forward manner, for example the parameter V_{ds} changes with supply voltage. Temperature variation can be incorporated in Eq. (1) by using temperature dependent transistor models of saturation velocity, mobility and source/drain resistance, as described in BSIM4 transistor model [16].

V. EXPERIMENTAL RESULTS

All experiments are conducted using a 65-nm ST Microelectronics gate library using the PTM transistor models [21]. The gate library consists of a variety of gates including simple (NAND, NOR, INV) and compound gates (AO22, OA22 etc.), each with different drive strengths. For illustration purposes 1.2-V is used as the nominal operating voltage in all experiments. The flow of the proposed modeling technique is shown in Fig. 9. The flow inputs are the required gate library and the transistor models and the output is the critical resistance of the bridge defect, which gives indication of the defect behaviour due to process variation. The flow has four main blocks as marked in Fig. 9. The bridge fault-site is generated by randomly selecting (driving and driven) gates from the gate library, using n driven gates per fanout, where $n \in [1, 5]$ and only non-feedback bridges are generated by the bridge fault-site generator. Each of the driving gate is assigned a random input, while ensuring that the two nets are driven at opposite logic values to activate the bridge fault. This setup uses 350 fault-sites for each experiment because it was shown in [7] that the average number of fault-sites per

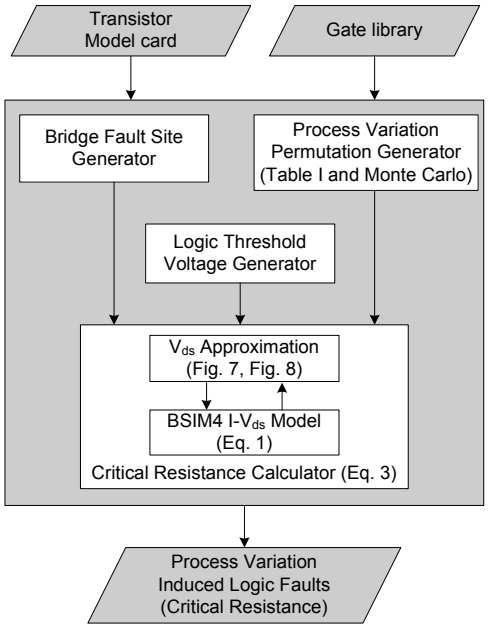

Fig. 9. Flow for Process Variation-aware Bridge Defect Modeling.

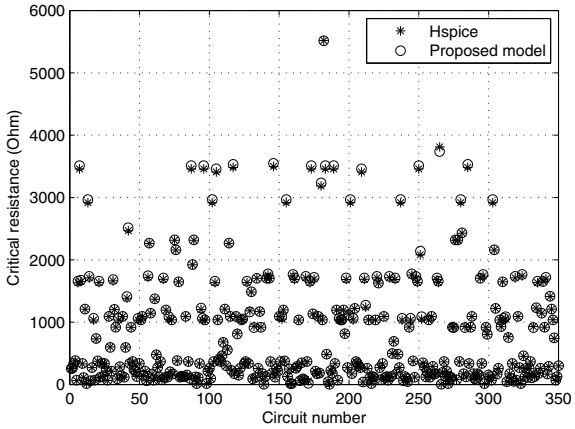

Fig. 10. Nominal operating conditions: proposed technique and HSPICE.

design is less than 300 with coupling capacitance based layout extraction of bridges using ISCAS 85, 89 benchmarks. For a given fault-site, the logic threshold voltages of the driven gate inputs' are simulated by HSPICE to achieve higher accuracy, by the logic threshold generator (Fig. 9). The effect of process variation is incorporated by the process variation permutation generator. It varies three parameters (L, V_{th} and μ_{eff}) using Gaussian distribution with mean and standard deviation as shown in Table I. In total 600 permutations per fault-site are generated through Monte-Carlo simulation. The number of permutations are based on a recent study, which shows that the probability of generating a unique logic fault follows the law of diminishing returns, as it reduces significantly after 500 permutations [20]. The outputs of these three blocks are fed to the critical resistance calculator (Fig. 9), that uses BSIM4 I-V_{ds} transistor model (Eq. (1)) and the V_{ds} approximation method (Fig. 7 and Fig. 8) to generate all process-variation induced logic faults along with their critical resistances. All experiments are conducted on Intel Xeon Quad Core 2.7 GHz processor with 12 GB RAM.

This setup is used to conduct two experiments. The first experiment (Section V-A) validates the proposed modeling technique by comparing the results with HSPICE in nominal operating conditions and under the influence of process variation. The second experiment (Section V-B) shows the effect of spatially correlated process parameter fluctuations on the behaviour of resistive bridge, and compares the outcome with the findings of the first experiment.

A. Validations of the Proposed Modeling Technique

The proposed modeling technique is validated by comparing the results with HSPICE in nominal operating conditions and then under the influence of process variation by using un-correlated parameter fluctuations of three parameters (L, V_{th} and μ_{eff}).

1) Nominal Operating Conditions: For the nominal operating conditions, the proposed model is used to calculate the critical resistance and the results are compared with HSPICE for 350 different fault-sites. The outcome is shown in Fig. 10. It can be seen that the proposed model performs very well and high accuracy is achieved in comparison to HSPICE for all 350 fault-sites. These results are further elaborated in Table II, which shows the calculated critical resistance for 6 fault-sites. These fault-sites include a number of cases where high approximation error is expected due to transistors in series. From Table II, it can be seen that the difference in calculated critical resistance varies from 4Ω to 12Ω, when compared with HSPICE, leading to calculation error of 0.1% to 0.8% respectively. The maximum difference is in case of a bridge driven by a 3-Input NOR gate and a 3-Input NAND gate (0.8%). This is because 3 transistors are in series in the pull-up and pull-down networks of the gates driving high and low respectively, and each transistor requires V_{ds} approximation using the method shown in Fig. 8, to calculate the critical resistance of the bridge. This particular case also shows the maximum difference in critical resistance calculation, out of all the fault-sites considered in nominal operating conditions. This shows that the proposed technique is accurate in nominal operating conditions with maximum difference of 0.8% in critical resistance calculation when compared with HSPICE.

2) Operating Conditions under Process Variation: The proposed technique is validated under the influence of process variation by considering variations of the three un-correlated parameters (L, V_{th}, μ_{eff}) by using the process variation integrator as shown in Fig. 9. Recent research has shown that it is sufficient to consider 3σ variation of process parameters, when modeling process variation for logical part of the design [7], [30], and higher variation effects (6σ or more) are considered for (SRAM and Flash) memories [4]. This work also deals

TABLE II
NOMINAL OPERATING CONDITIONS: HSPICE RESULTS IN COMPARISON TO THE PROPOSED MODEL.

Driving Gates (D_1, D_2)	Boolean Input(s)		R_{crit}, Ω		Error %
			HSPICE	Proposed Model	
INV, INV	0	1	1661	1657	0.24
INV, 2-Input NAND	0	1, 1	1232	1224	0.65
2-Input NAND, 2-Input NAND	0, 0	1, 1	3752	3748	0.1
2-Input NOR, 2-Input NAND	0, 0	1, 1	2104	2093	0.52
2-Input NOR, 3-Input NAND	0, 0	1, 1, 1	1655	1647	0.48
3-Input NOR, 3-Input NAND	0, 0, 0	1, 1, 1	1500	1512	**0.8**

TABLE III
HSPICE RESULTS IN COMPARISON TO THE PROPOSED TECHNIQUE USING 3σ VARIATIONS OF UN-CORRELATED PARAMETERS (L, V_{th}, μ_{eff}).

Driving Gates		3σ Variation R_{crit} (Ω)		
(D_1, D_2)	Mechanism	Low	High	Time (s)
INV, INV	PM	95	7557	15.7
	HSPICE	99	7574	292.4
INV, 2-Input NAND	PM	410	9757	21.2
	HSPICE	406	9762	311.2
2-Input NAND, 2-Input NAND	PM	2548	14004	73
	HSPICE	2569	13900	315.2
2-Input NOR, 2-Input NAND	PM	61.6	11998	33.3
	HSPICE	56	12080	309.1
2-Input NOR, 3-Input NAND	PM	60	13544	33.4
	HSPICE	67	13440	296
3-Input NOR, 3-Input NAND	PM	75	13159	38.8
	HSPICE	73.6	13090	329.4

* PM → Proposed Modeling Technique

with the logical part of the design, which is why we have also considered 3σ variation effects. The results are shown in Table III for the same set of fault-sites as in Table II. It shows the calculated critical resistance under the influence of process variation for the two techniques (PM (Proposed Modeling Technique) and HSPICE). The low and high values of R_{crit} represent the minimum and maximum values of critical resistance, as a result of variations. It can be seen that the minimum and maximum differences are 1.4 Ω and 104 Ω respectively, which is also the maximum difference observed for all 350 fault-sites. It should be noted that bridge fault is detected over a range of resistance values and a test is not for a specific (discrete) resistance, as shown in [12]. For example, all bridges with resistance values $R_{sh} \in [0, R_{I3}]$ (Fig. 2) are detectable with the same test. This means that the difference in resistance values (Table II, Table III) in between the proposed model and HSPICE does not necessarily mean loss of test coverage. Next, to observe the effect of process variation on critical resistance of a bridge, we used a fault-site with two inverters as driving gates and only one gate is used as a driven gate. The change in critical resistance is shown in Fig. 11, as can be seen the proposed model achieves very high accuracy when compared with HSPICE.

The last column of Table III shows the simulation time of the two techniques. To demonstrate the relative speedup in critical resistance calculation using the proposed technique, the simulation time of logic threshold generation is excluded as it is the same for both, either by using pre-computed database or HSPICE at runtime. It can be seen that the proposed technique is approximately 9 times faster than HSPICE and in general, 7 times faster for 350 fault-sites. However, when the logic threshold generation time is included using HSPICE at runtime, the relative speed up is more than 10% for all 350 fault-sites, when considering upto 5 driven gates per bridged net. We are currently investigating more efficient ways for

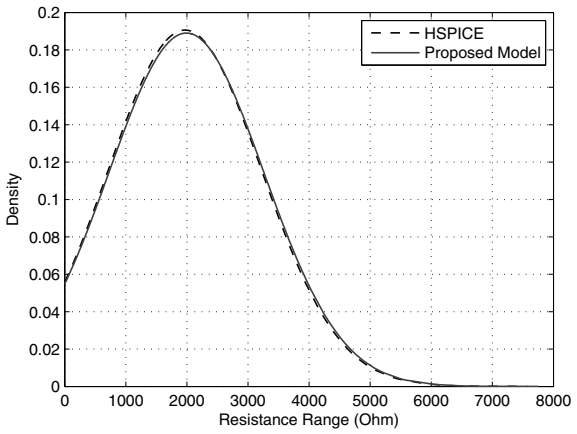

Fig. 11. The effect of process variation on the critical resistance of a bridge driven by two inverters.

logic threshold generation than pre-computed databases or runtime HSPICE. These results clearly show that the proposed technique is sufficiently accurate and significantly faster than HSPICE.

As described in Section II, the newly generated logic faults (leading to test escapes) are due to change in gate output voltages (V_0 and V_1 as in Fig. 1) of the driving gates and logic threshold voltages of the driven gates. We analyzed the effect of process variation on these two parameters and the results are shown in Table IV for 1σ variation around mean. The change in gate output voltage is simulated by using the proposed model with $R_{sh} = 0\Omega$ (V_0=V_1) on 350 fault-sites. The effect of logic threshold variation is simulated by HSPICE for each gate input of all the gates in the gate library. On average, the logic threshold voltage varies in the range of [-4%, 3.7%] around the mean, and it is lower than the gate output voltage variation, which on average varies in the range of [-17.6%, 18%]. The experimental results discussed in this

TABLE IV
EFFECT ON GATE OUTPUT VOLTAGE (V_0) AND LOGIC THRESHOLD VOLTAGE (L_{th}) DUE TO 1σ UN-CORRELATED PARAMETER FLUCTUATIONS.

Parameter	Range	V_{th}, L and μ_{eff}	
		Low	High
V_0 (R_{sh} = 0 Ω)	Min.	-3%	2.8%
	Max.	-24.8%	30%
	Avg.	-17.6%	18.0%
Logic Threshold	Min.	-0.5%	0.2%
	Max.	-13.3%	13.2%
	Avg.	-4%	3.7%

section clearly demonstrate the efficiency (speed and accuracy) of the proposed modeling technique in comparison to HSPICE.

B. Effect of Spatially Correlated Parameter Fluctuations

Gate length is a leading source of variation that shows correlated variation effects due to lithography [17] and its effect is examined in this experiment. We investigated the effect of within die spatial correlation using the proposed model[2] to compare its effect with un-correlated parameter fluctuations on resistive bridges. This is analyzed by varying (3σ) the gate length "L" using a spatial correlation model described in Section IV-B, with 600 permutations per fault-site. The correlation coefficient ρ is calculated using Eq. (5) and Eq. (6) respectively, with $\rho \leq 0.8$ and the baseline correlation ρ_B is 0.2. This is compared with un-correlated 3σ variation of "L". Table V shows the results for the same set of fault-sites as in Table II. As can be seen the un-correlated variation of "L" results in wider spread than spatially correlated variations. This is further shown in Fig. 12, which shows the distribution spread of a bridge critical resistance. Two inverters are driving this bridge with only one driven gate, and three different types of variations are used for this purpose: "L" with spatial correlation ($\rho \leq 0.8$ and $\rho_B = 0.2$), "L" without spatial correlation and by using three un-correlated parameters (L, V_{th} and μ_{eff}). As expected, the 3σ variation of L, V_{th} and μ_{eff} results in a much wider spread of critical resistance than the other two types of variations. From this experiment it can be observed that the effect of spatial correlation is covered by considering variations due to three un-correlated parameter (L, V_{th} and μ_{eff}). From test generation point of view, it means that considering the three un-correlated parameter variations is likely to cover the complete logic fault domain due to spatially correlated parameter variation.

In this paper, the effect of uncorrelated and correlated parameter variation is modeled by using [6] and [17] respectively. The proposed technique (Fig. 9) is independent of any specific variation model and can be used to incorporate the effect of other parameters using their respective distribution models, for example as used in [7] and [30].

[2]Section V-A confirmed the accuracy of the proposed model, which is why HSPICE is not used in this experiment.

TABLE V
SPATIAL CORRELATION OF "L" USING 3σ VARIATION.

Driving Gate (D1, D2)	R_{crit} (Ω)	L with SC ρ_B = 0.2, $\rho \leq 0.8$	Un-correlated L
INV, INV	Low	251	237
	High	3724	4020
INV, 2-Input NAND	Low	674	537
	High	4396	5009
2-Input NAND, 2-Input NAND	Low	2855	2808
	High	5841	6311
2-Input NOR, 2-Input NAND	Low	331	216
	High	4760	5210
2-Input NOR, 3-Input NAND	Low	270	146
	High	5697	6006
3-Input NOR, 3-Input NAND	Low	243	122
	High	5639	5954

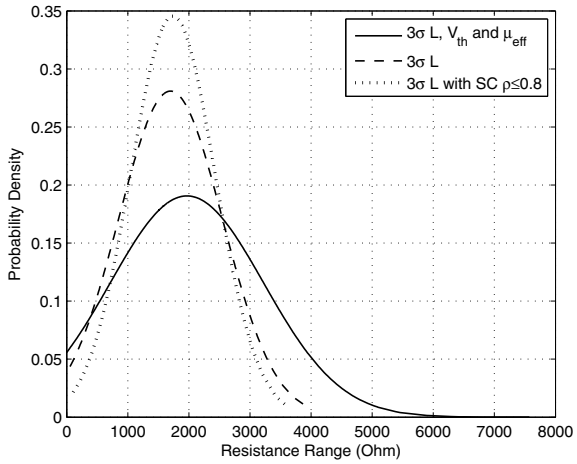

Fig. 12. Comparison of spatially correlated and un-correlated parameter fluctuations on the critical resistance of a bridge driven by two inverters.

VI. CONCLUSION

This paper has presented a modeling technique that takes into account the effect of process variation on resistive bridge defects. The modeling technique employs an accurate BSIM4 (I-V_{ds}) transistor model that is applicable in all operating regions and accurately relates the inter-dependencies between different transistor parameters by integrating advanced models that relate different electrical parameters with device structure. The effect of process variation is modeled by using three transistor parameters: L, V_{th} and μ_{eff}, using Gaussian distribution. The experiments conducted on a 65-nm gate library show that it is fast (average is 7 times faster) and accurate (worst case is 0.8% error in critical resistance calculation) when compared with HSPICE simulation results in identical operating conditions. The effect of spatial correlation between the gate length of different transistors on the same die is found to be covered by the variation effects of the three (L, V_{th} and

μ_{eff}) mutually independent parameters. Therefore a test for these three parameters is likely to cover all the logic faults due to within die spatial correlation.

The proposed modeling technique has been demonstrated on a 65-nm gate library, and it can be used for evaluating the impact of process variation on bridge defect using other technology nodes. The flow (Fig. 9) will require a gate library with respective transistor model card and appropriate values of mean and standard deviation for the three transistor parameters (Table I). Our continuing work includes developing a fault simulator and test generation methods for static and dynamic test that incorporates the proposed modeling technique to maintain the quality of manufacturing test in the presence of process variation.

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