2010 Asia Pacific Conference on Circuits and Systems (APCCAS 2010)
6 – 9 December 2010, Kuala Lumpur, Malaysia

Effects of CNT Diameter Variability on a CNFET-Based SRAM

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***Abstract*—In this paper we study the effects of Single Walled Carbon Nanotube (SWCNT) diameter variations on performance and stability of 6-T SRAM cells. Parametric and Monte Carlo simulations are performed for SRAM designs based on different SWCNT mean diameters. Parameters such as read/write delays, Static Noise Margin (SNM) and Write Margin (WM) are studied together with the effects of diameter variations on them. Our results show that minimum variation of timing characteristics and noise margins can be achieved at a CNT mean diameter of 1.2nm.**

I. INTRODUCTION

With the scaling of conventional CMOS reaching its physical limits, researchers are concentrating on alternative devices. The Carbon NanoTube (CNT) is one of the most promising of these devices [1]. CNT Field Effect Transistors (CNFETs) could become ideal choices for future of nano-electronics due to their high drive currents, low leakage power and good gate controllability. However lack of process control over CNT fabrication processes incurs a wide range of variations in I-V characteristics of CNFETs due to CNT diameter (*D*) variations, causing unreliable electrical behavior of logic circuits and memories made from them. This paper aims to quantify the effects of imperfections in the fabrication process of CNTs on the performance of CNT-based SRAMs. For this purpose we have used the CNFET model proposed in [9] which has been shown to be more accurate in comparison with other available models [9].

Recent growth techniques can achieve as high as 96% semi-conducting CNTs [2]. Here we assume only semiconducting CNTs are used in the design of a CNFET. The most commonly used statistical CNT diameter models adopt Gaussian distribution [3]. Several studies of the performance of CNFET SRAMs in comparison with CMOS SRAMs have been made [13, 14 and 18]. None of these however, take into account the limited control over *D*, thereby ignoring effects of *D* variation in providing comparative figures for CNT- and CMOS-based SRAM stability and performance. We attempt to address this issue and provide detailed analysis of *D* variability effects on performance metrics of a CNFET-based SRAM.

The rest of this paper is structured as follows. Section II provides an overview of the CNFET structure. Our proposed SRAM design is presented in Section III. The Simulation procedure of the SRAM is explained in Section IV. Section V provides analysis of the results and section VI concludes the paper.

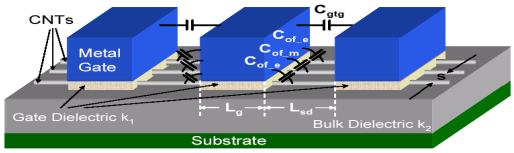

Figure 1. CNFET with multiple CNTs [9]

II. CNFET STRUCTURE

Two alternative CNFET structures are prominent: Schottky Barrier (SB) FET [5] and MOSFET-like FET [6, 7]. SBCNFETs show ambipolar behavior [8] which is undesirable as far as complementary logic design goes [8]. MOSFET-like CNFETs exhibit unipolar behavior and as far as fabrication is concerned they are easier to make. We have used a CNFET model developed by Stanford [9] which implements a circuit-compatible compact model for CMOS-like Single Walled (SW)-CNFETs and is implemented in HSPICE. It is superior to previous models in that it accounts for scattering in the channel region, the resistive source/drain, the SB resistance and the parasitic gate capacitance. By adding a full trans-capacitance network the model produces better predictions of the dynamic performance and transient response. Previous models used one or more lumped static gate capacitances and an ideal ballistic transport model [6, 10]. The model has been calibrated against experimental CNFET data to within 90% accuracy [12]. The CNFET structure used in this work is shown in Fig. 1. The section of the SWCNT under the gate is intrinsic. For doped source/drain extension regions doping level is taken as 1% which is above the first conduction band of the SWCNT. The model assumes equal electron and hole mobility in CNTs. One or more devices can be fabricated along the same CNT. Multiple CNTs may be placed under the same gate.

III. 6-CNFET SRAM

We have designed and simulated a 6 CNFET SRAM cell (Fig. 2). The 6T SRAM is commonly used and is superior to other SRAM structures due to its superior robustness, low power operation and short access time [11].

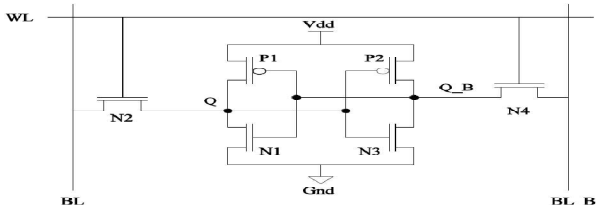

Figure 2. Schematic of 6T SRAM

For read stability N1 must be stronger than N2 [15]. Also, to satisfy writeability P2 must be weaker than N4 [15]. To have higher drive current and hence "stronger" transistors in CNFETs more CNTs are put under the gate of the transistor. Hence, N1 & N3 employ 3 CNTs under the gate; N2 & N4 have 2 CNTs and P1 & P2 employ 1 CNT under the gate. Centre to centre CNT spacing (S) is 20 nanometers (nm) since at this S the charge screening effect of CNTs on each other and its effect on drive current and SRAM performance is negligible [9].

IV. Simulation Conditions

To be consistent with the work of [4], various values for mean D in the range 1.01nm to 1.71nm are taken into account. Considering the inaccuracy of fabrication techniques, a standard deviation (STD) from the mean (μ) in the range of 0.04nm to 0.2nm was introduced for each mean diameter (D_μ) value. D distribution is assumed as Gaussian; a reasonable assumption for large numbers of fabricated CNTs [3]. A positive distribution is also considered as CNT diameter always has a positive value.

Monte Carlo (MC) simulations were performed to analyze how random variations of D_μ and diameter STD (D_δ) affect the mean and STD of the various performance parameters. In addition, parametric simulations were performed to study how D affects the performance parameters of the SRAM such as Static Noise Margin (SNM) and Write Margin (WM). For the MC simulations, five different samples of D_μ within the abovementioned range were considered. For each D_μ sample, five categories of D_δ in the range 0.04nm to 0.2nm were taken into account. As long as D < 3nm (typical for CNT devices) and the CNFET is taken to be a short-channel device (where CNT length under the gate is < 100nm) only the first conduction/valence bands have a significant effect on current with a power supply of less than 1V [9]. A physical channel length of 32nm and an oxide thickness of 4nm are assumed. This channel length is short enough for the device to be assumed short channel and long enough for the model to correctly simulate the device (CNFETs with channel lengths <10nm cannot be simulated correctly by the model). The physical metal gate width of a CNFET is assumed to be 48nm. This width affects the parasitic capacitance but the on-current depends on the actual "effective" gate width which is determined by the number of CNTs under the gate and the spacing between them. A power supply voltage of 0.9V is used in accordance with the ITRS roadmap for 32nm technology [16]. 10,000 samples were taken and MC iterations were run for each D_μ and D_δ considered. All simulations are run for the 32nm technology node.

Write delay is defined as the time from the 50% activation of WL to the time the internal nodes Q and Q_B (Fig. 2) reach 50% of their final value [17]. Read delay is defined as the time required for developing a 100mV differential voltage between BL and BL_B after WL reaches 50% of its final swing [18]. As the worst-case stability condition for our SRAM configuration occurs when the cell is accessed for read operation, read SNM is the focus in this work.

V. Results

A. Read/Write Delay

Figs. 3 and 6 show the relationship between read and write delays with different values of D respectively. Both delays decrease as D increases. As band gap (E_g) of a CNT is inversely proportional to D [3], increasing D will cause a decrease in E_g which allows for larger on-currents of CNFETs; thus reducing delay. It can be observed from Figs. 3 and 6 that the delay increases rapidly below D of around 0.85nm. It is interesting to note that in [4] we also observed that for various logic gates the D at which variations in timing delays greatly increased was the same value of 0.85nm. Figs. 4 and 7 depict the dispersion of mean read/write delay values with D_μ and various D_δ. It is observed that mean read/write delay increases with D_μ and fixed D_δ. As equal D_δ values translate into different percentage change in different D_μ, we have taken the Coefficient of Variation (CV) into account. CV is the ratio of STD over μ and is a normalized measure of dispersion which is comparable among different mean distributions. Results reveal that both read and write delays show the least amount of variation at maximum D_μ of 1.71nm as this is where the smallest value for CV is obtained. In Figs. 5 and 8 STDs of read and write delays are plotted against D_δ respectively. It can be observed that at smaller D_μ, D_δ variations cause far greater deviations in delay values. For instance at D_μ of 1.01nm, a D_δ of 0.2nm causes a read delay STD of 1ns, but the same D_δ for a D_μ of 1.71nm, only gives a 0.05ns STD in read delay. This result suggests higher reliability in terms of read/write delay variations with larger D.

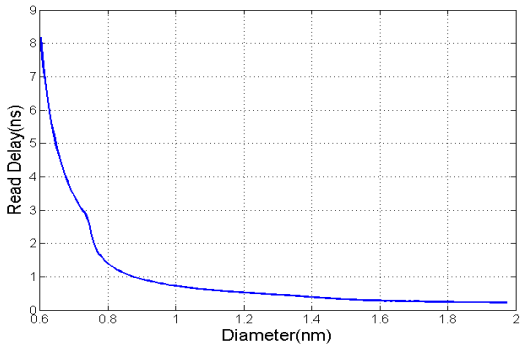

Figure 3. Dependence of Read Delay on CNT diameter

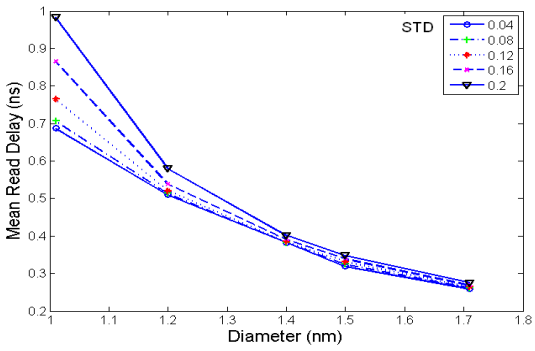

Figure 4. Variation of Mean Read Delay with diameter Mean and STD

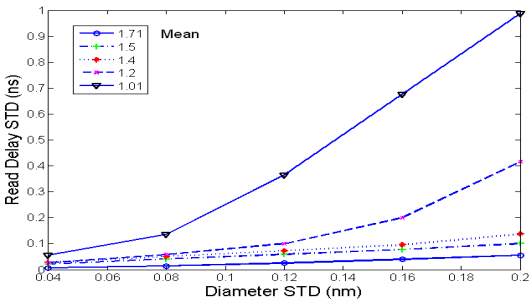

Figure 5. Read Delay STD vs. CNT diameter Mean and STD

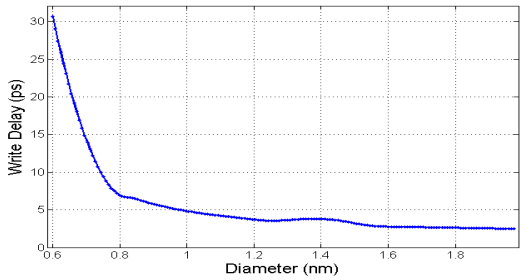

Figure 6. Dependence of Write Delay on CNT diameter

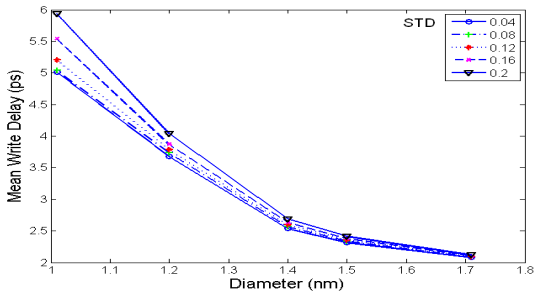

Figure 7. Variation of Mean Write Delay with diameter Mean and STD

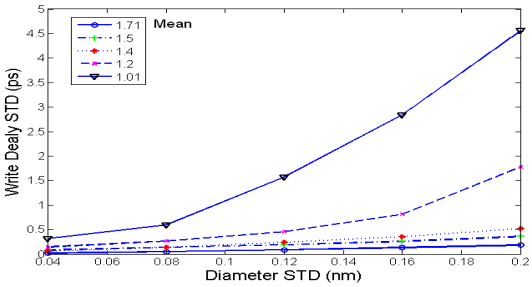

Figure 8. Write Delay STD vs. CNT diameter Mean and STD

B. *Static Noise Margin*

An important measure of the stability of SRAM cells is SNM; defined as the maximum value of DC noise voltage tolerated without changing the stored bit [19]. A large SNM is desired to ensure stability of SRAM. Fig. 9 shows that SNM remains almost constant at the high value of ~270mV for $D \leq 0.85$nm. Above 0.85nm SNM worsens almost linearly with D increasing; although even for larger CNT diameters, SNM of CNFET-based SRAMs is superior to that of CMOS implementations [15]. SNM depends on three factors [19]: threshold voltage (V_{th}), power supply and Cell Ratio (CR). With the CNFET-based SRAM, CR can be considered as the ratio of the number of CNTs in the drive transistors to that of access transistors; 3/2 in this case. Power supply is fixed in our simulations; V_{th} is the only remaining factor which could cause variation in SNM. V_{th} is given by:

$$V_{th} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD} \quad (1)$$

Where a = 2.49Å, the carbon to carbon atom distance, V_{π} = 3.033eV, the carbon π-π bond energy in the tight binding model, e is the unit electron charge and D is CNT diameter.

It can be seen from (1) that V_{th} is inversely proportional to D, meaning D can be the only cause of SNM variations here. Thus, the decrease of SNM with increasing D in Fig. 9 is explained through the dependence of V_{th} on the inverse of D. SNM is proportional to V_{th} [19]; as D increases, V_{th} decreases, causing SNM to decline. Fig. 9 shows that below D of ~0.85nm, there is little change in SNM. There is even a slight decrease in SNM with decreasing D. We have run simulations and found that there is a slight variation in CR at these small diameters (CR increases from ~1.48 at $D \approx 0.6$nm to ~ 1.49 at $D \approx 0.8$nm and stabilizes at this value for larger D). This slight change in CR can be accredited to minute current changes due to charge screening effects; hence, the slight rise in SNM can be explained by the fact that SNM rises with increasing CR [19]. There is little change in mean SNM with D_{δ} especially when D is large. For a D_{μ} of 1.01nm and in the range of D_{δ} considered, SNM only varies by ~10mV throughout. This change for $D > 1.5$nm is ~ zero (Fig. 10). STD change in SNM with various D_{μ} and D_{δ} is shown in Fig. 11. It is clear that the change in STD of SNM with D_{δ} is roughly constant for all D_{μ}.

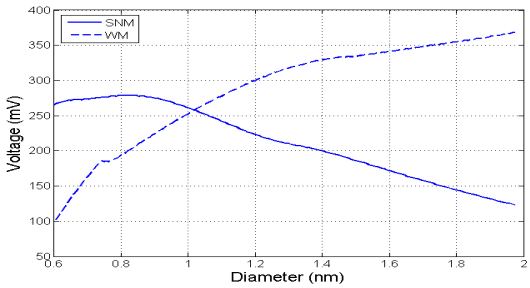

Figure 9. Effect of diameter change on SRAM SNM and WM

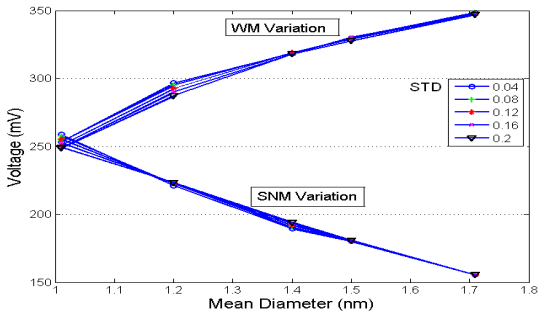

Figure 10. Variation of mean SNM and WM vs. diameter Mean & STD

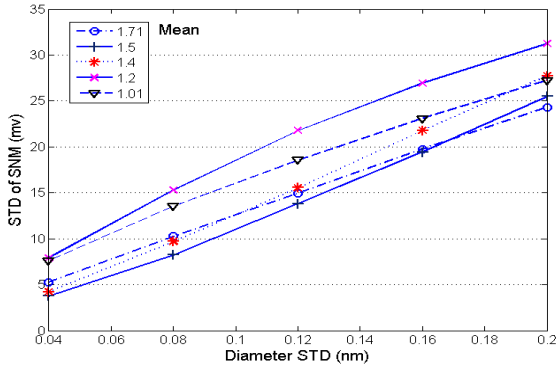

Figure 11. STD of SNM vs. diameter Mean & STD

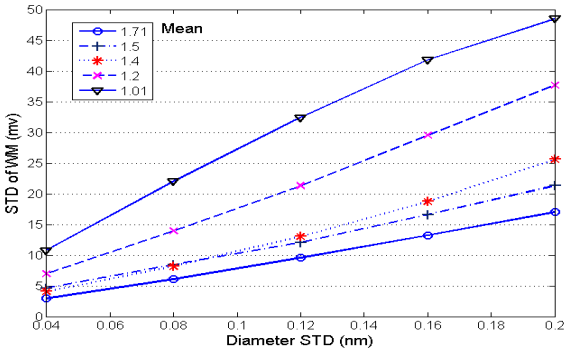

Figure 12. STD of WM vs. diameter Mean & STD

C. *Write Margin*

WM and SNM are often tradeoff parameters in SRAM design. The higher the SNM, the more difficult it is to write data into the cell (lower WM). A high WM is desired as it can improve write delay and ensure correct data is being written. WM is inversely proportional to the pull-up ratio (PR) of the SRAM cell and V_{th}. PR is defined as the drive current ratio of pull-up transistors over that of access transistors. Our simulation results have shown that PR is almost constant; hence WM variation is dominated by V_{th}. As D increases, V_{th} is lowered, causing WM to rise as seen in Figs. 10 and 12. STD of WM rises as D_δ increases with a fixed D_μ, Fig. 12. The minimum variation in WM is observed with the largest D_μ of 1.71nm.

VI. CONCLUSION

We have analyzed the performance of a CNFET-based SRAM in the presence of D variations due to manufacturing inaccuracy. In terms of read and write delays, results suggest that larger D_μ and smaller D_δ are optimal as they result in the least read/write delays and also less variation in mean and STD of delays, meaning more reliable circuit operation in terms of timing characteristics.

Improved SNM is provided with smaller D but smaller D also means lower WM; hence, there's a tradeoff involving circuit speed and WM on one side and SNM on the other. As a general rule, considering D_δ which is always present during CNT synthesis, it can be suggested that D_μ should be kept above 1nm but not larger than 1.5nm. Of course to be able to suggest a certain D_μ for CNFET-based electronics, power consumption should also be taken into account. This is the direction of our future work.

ACKNOWLEDGMENT

We thank Professor Peter Ashburn for his valuable guidance.

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