Genetic-Based High-Level Synthesis of ΣΔ Modulator in SystemC-A

Chenxu Zhao and Tom J. Kazmierski
School of Electronics and Computer Science
University of Southampton, UK
Email: cz05r,tjk@ecs.soton.ac.uk

***Abstract*—This paper proposes a novel genetic-based high-level synthesis methodology for ΣΔ modulators. This approach is based on simulation-based optimisation where optimal topology of the ΣΔ modulator is automated explored using a genetic algorithm(GA) under various design constraints, such as SNR(Signal-to-Noise Ratio) and hardware complexity. The proposed synthesis technique has been implemented in SystemC-A due to its advantages in terms of high simulation speed, flexibility and data manipulation. Experimental results validates the effectiveness of the synthesis approach.**

I. Introduction

As an important interface block, ΣΔ modulators are widely used in various applications such as audio and telecommunication devices [1], [2]. However, high-level design of ΣΔ modulators remains mostly manually and it is critical to exploring the feasible topologies because of the large number of connections between components in ΣΔ modulator (integrators, DAC, quantizer). Typically, a library of traditional topologies is available for designers to select according to designers' experience while structure design is accessible only to a small number of expert designers [3].

In order to decrease the complexity of the design procedure, several tools for automated ΣΔ modulator design have been developed recently [3], [4], [5], [6], [7], [8]. Most of the methodologies are based-on the optimisation of the coefficients of signal paths for preset popular ΣΔ modulator topologies [4], [5], [6]. Ruiz-Amaya et al. [6] develop a toolbox in MATLAB/Simulink environment to optimize the coefficients of the selected ΣΔ modulator structures using an adaptive statical optimization algorithm based on simulated annealing. A behaviour simulation-based synthesis tool(DAISY) is programmed in C language by Francken et al [7]. A set of selected topologies are stored in a library. The synthesis tool automated test all the topologies in the library and choose the one with the smallest power consumption according to design specifications (SNR and signal bandwidth). The major limitation of these techniques is that the design space for topology exploration is restricted. Thus, only local optimality is achieved for predefined design objectives.

To overcome the limitation, some methodologies are presented to realize the topology synthesis for ΣΔ modulator [3], [8]. Tang [3] proposes an MINLP-based synthesis flow. In this approach, a generic representation, which describes all possible topologies for a certain order single-bit single-loop ΣΔ modulator, is defined to derive the symbolic TF(Transfer Function). The MINLP description contains nonlinear equations that express the generic TF and a cost function describing signal-path complexity, sensitivity, and power consumption. Finally, the MINLP description is embedded into a design flow to obtain the optimal topology satisfies design specifications. However, the TF is difficult to be built as the complexity of the symbolic terms grows roughly with the modulator order [3]. In [8], Yetik creates a tool in MATLAB to automated generate the transfer functions of ΣΔ modulators which are used as inputs of the synthesis algorithm to find all the possible topologies to achieve the desired frequency response. However, the coefficients of the synthesized topology are not optimized in this approach.

This paper presented an novel synthesis method for automated synthesis architecture of ΣΔ modulator and optimizing the topology parameters to satisfy the design constraints. This approach, which integrates an ΣΔ modulator primitive component library, an efficient evaluation engine and an evolutionary computation method (GA), is implemented in SystemC-A [9]. SystemC-A is an extended version of SystemC [10] which allows modelling of mixed-signal and mixed-energy domain systems at arbitrary levels of abstraction. Most powerful features of existing HDLs (e.g. VHDL-AMS [11] and Verilog-AMS [12]) and a number of extra advantages in terms of simulation speed, data manipulation and flexibility are provided by SystemC-A [13].

Single-loop ΣΔ modulators are used as case studies to validate the proposed synthesis technique. However, this approach is general, it can be extended to multi-loop modulators. Experimental results show that the synthesized topologies are superior to traditional topology.

II. Genetic-Based Synthesis Flow

The genetic-based optimal synthesis flow is shown in Fig. 1. After specifying the design objectives and constraints such as the signal bandwidth, peak SNR and the order of ΣΔ modulators, available components in primitive cell library are combined automatically to form an initial design set as the input of synthesis module. In the synthesis module, Genetic Algorithm(GA) is used to explore the feasible topologies and optimize the objective functions.

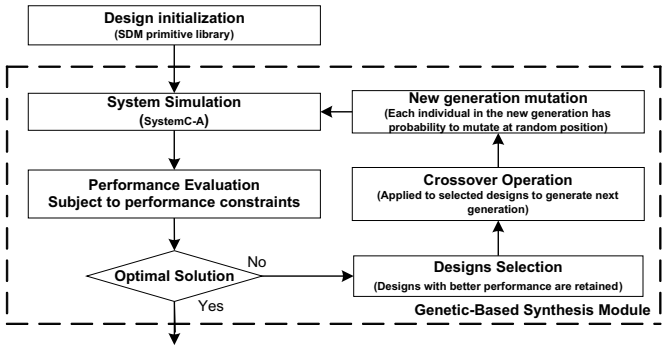


Fig. 1. Genetic-based automated synthesis flow

A. Design Initialization

The components in the ΣΔ modulator primitive library are shown in Fig.2. For simplicity, non-idealities of components are not considered in this work. Drawing from the library, a set

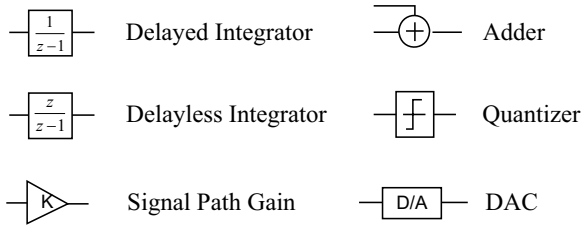
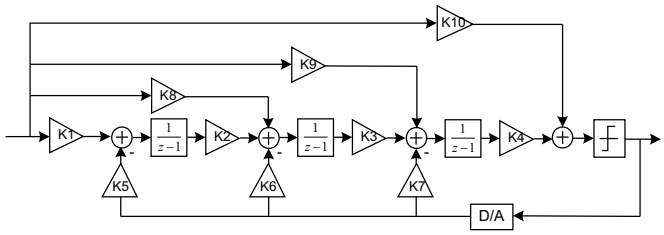


Fig. 2. ΣΔ modulator primitive library

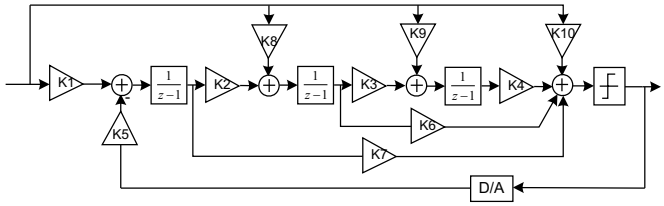
of topologies is automatically generated (parents of the first generation in GA) in the design initialization phase and loaded into the synthesis module. Each topology in the initial set is generated in 3 steps. Firstly, The number of integrators are determined by predefined order of ΣΔ modulators. The type of each integrator (delayed or delayless type) in the modulator is randomly defined by the system. Secondly, components in the modulators can be randomly connected by feedforward and feedback paths. Finally, all the coefficients in the generated topology get random initial values. Subsequently, SystemC-A model is automated generated according to this topology. Fig.3 shows some well-known 3rd order single-loop ΣΔ modulator topologies [1] which can be generated in the design initialization phase.

B. Genetic approach to synthesis

Genetic Algorithm (GA) is selected in this work because it is a popular and well tested optimization algorithm which has demonstrated good performance in a wide variety of complex global optimization problems. In the proposed genetic-based synthesis approach, performance figures of the candidate designs are evaluated by a fitness function that rates the solutions according to their performance parameters. The performance parameters such as SNR are obtained from behavior simulation results of the SystemC-A models. The fitness function is constructed in a weighted scalar error form which will be illustrated in the next section.



(a) Integrators with distributed feedback and input coupling(CIFB structure)



(b) Chain of integrators with feedforward signal paths(CIFF structure)

Fig. 3. Well-known single-loop ΣΔ modulator topologies

After evaluating the initial designs, classical genetic operations (selection, crossover, mutation) are applied to current generation parents to breed the new generation. In the selection operation, a proportion of designs with better performance (higher fitness) are retained. After the selection, if the crossover operation is triggered (crossover probability exceeds a fixed threshold), new off-springs are generated by exchanging elements of selected parents such as the signal paths and type of integrators. An example of crossover operation are illustrated in the Fig. 4. As shown in the figure, the crossover probabilities of the type of 1st integrator and the feedforward signal path from the input to 2st integrator are higher than the trigger probability in this example. Thus, these two components of parents A and B exchange leaving the other components constant to get the new offsprings. Finally, a new generation is obtained after applying crossover operation to the selected designs.

For each of the individuals in the new generation, the genes on their chromosomes have fixed probability to mutate. Mutation operation contains two phase: topology mutation and component's coefficient mutation. In the first phase, if topology mutation probability is higher than the fixed trigger, new topology is automated generated from the ΣΔ modulator primitive library and each parameter in the generated topology get random value within range as illustrated in design initialization phase. If there is no mutation in the first phase, mutation probability of each component in the ΣΔ modulator topology will be compared with the trigger to decide whether component's parameter will mutate.

This evolution process finishes when the generation size exceeds the specified number. The optimal solution in the given generation is that with the highest fitness.

III. Synthesis Experiments

In this section, automated synthesis of a third order single-loop ΣΔ modulator is used as a case study to demonstrate the

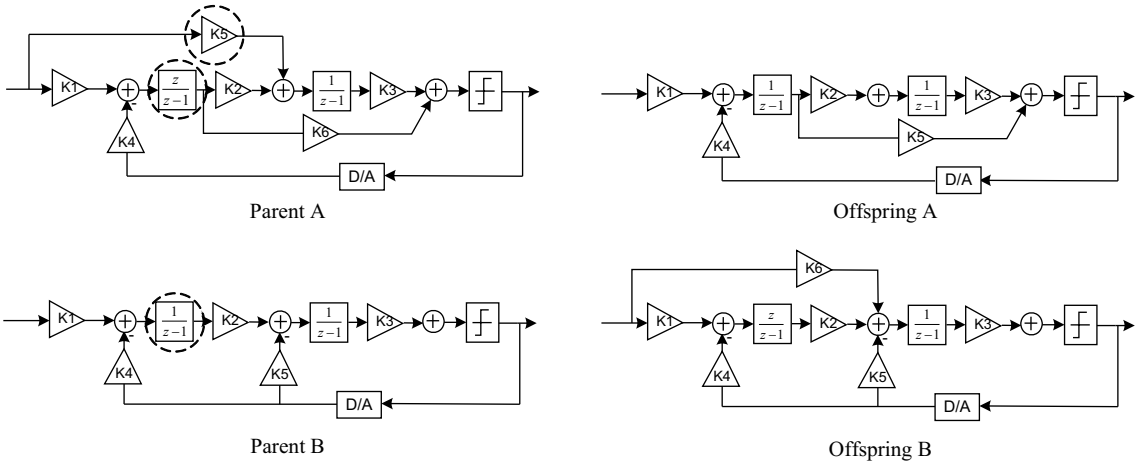


Fig. 4. An example of crossover operation in synthesis module

	Design objective	*Performance constraints*	*Objective Reference*
1	Maximum SNR	SNR≥110dB No.of signal path≤15	SNR=110dB
2	Minimum signal path	SNR≥110dB No.of signal path≤12	No.of signal path=12

TABLE I
SYNTHESIS EXPERIMENTS

practical operation of the proposed approach. The synthesized results are compared with traditional modulator [2], [14].

The synthesis of a 3rd order SDM is demonstrated by two experiments as shown in Table 1. In experiment 1, the topology is synthesized for maximum SNR and in experiment 2 - for minimum complexity(minimum signal-path).

The search for a solution is guided by the synthesis objective(Fitness function). The objective fitness function is in the following format:

$$Fitness = K\frac{Objective}{Objective'} \tag{1}$$

Where K is the weight coefficient, $Objective$ is the system performance measure obtained from each simulation while $Objective'$ is the designer specified objective reference value.

Experiment 1:

$$Fitness = K\frac{SNR}{SNR'} \tag{2}$$

SNR' is the objective reference value($SNR' = 110dB$). K is set to 1 if all user defined performance constraints are met, otherwise K is set to 0.0001. For example, if a synthesized topology can achieve 110dB SNR with less than 15 signal paths, K will equal to 1 that means the algorithm finds a feasible solution. In the proposed synthesis approach, a performance evaluation engine is embedded in SystemC-A to enable measurements of the power spectrum density (PSD) and SNR through FFT of the output bitstream.

Experiment 2:

$$Fitness = K\frac{NPath}{NPath'} \tag{3}$$

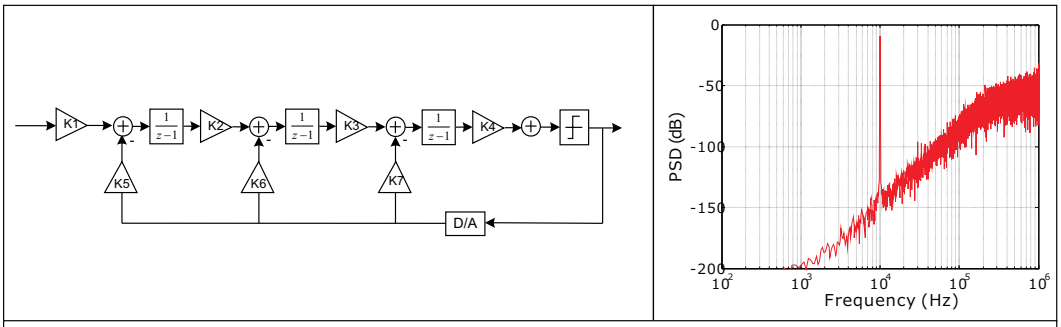
$NPath$ is the number of signal paths in the synthesized structure. In order to minimize the fitness parameter, K is set to -1 if performance constraints are met or -10 otherwise.

The synthesis process was carried out using the following design parameters:

1) Oversampling ratio: OSR=128
2) Bandwidth: 20KHz
3) Oversampling frequency: fs=5.12MHz
4) Input frequency: $10KHz$
5) Reference voltage: 1V
6) Order of Sigma-Delta modulator: 3

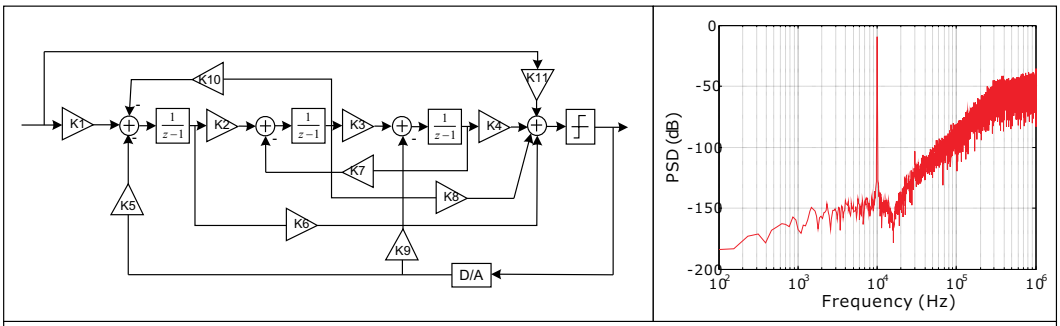
The fitness improvement during the synthesis flow is shown in Fig.5. It is clear that the synthesis approach finds a feasible solution and then further explores the design space to approach the optimal solution.

The synthesized topologies and associated PSD, which is measured by output bitstream, are shown in Fig. 6. The traditional 3rd order topology [2], [14] is also plotted for comparison. It is obvious that the noise floor in synthesized topology of experiment 1 can be reduced further leading to about 12dB improvement of the SNR comparing with the typical structure. In experiment 2, the synthesis approach is used to explore design space to find the topology which has minimum number of signal paths while SNR maintained above 110dB. As shown in the synthesized result, the topology with 8 signal paths achieves the design specifications. Although this topology contains 1 more signal path comparing with the typical one, it achieves around 9dB improvement of SNR. Fig. 7. plots the SNR curves of the synthesized and traditional topologies. As shown in the figure, the synthesized solutions also achieve better performance in terms of dynamic range(the input amplitude achieves zero-crossing SNR). As illustrated in the experimental results, the proposed approach realized automated topology synthesis of $\Sigma\Delta$ modulator according



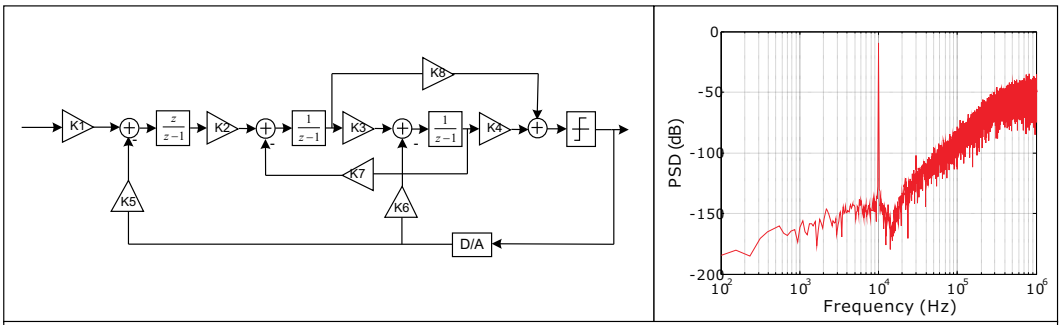
K1=1 K2=0.5 K3=0.3 K4=0.4 K5=1 K6=1 K7=1
System Performance
SNR=103.5dB DR=120dB Number of Signal paths=7

(a) Traditional 3rd order ΣΔ modulator



K1= 0.45 K2= 0.84 K3=0.32 K4=0.3 K5=0.45 K6=0.24 K7=1.06e-3 K8=0.42 K9=1.1 K10=5.6e-5 K11=1.8
System Performance
SNR=115.3dB DR=136dB Number of Signal paths=11

(b) Synthesized result of experiment 1 (Maximum SNR)



K1= 0.54 K2=0.714 K3=0.348 K4=0.352 K5=0.545 K6=1.173 K7=9.38e-4 K8=0.539
System Performance
SNR=112.1dB DR=126dB Number of Signal paths=8

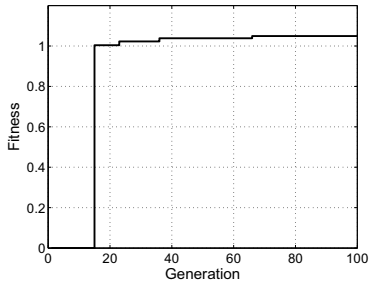
(c) Synthesized result of experiment 2(Minimum signal paths)

Fig. 6. Synthesized and traditional 3rd order ΣΔ modulator topologies

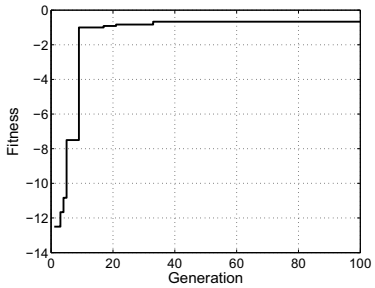
to user defined design specifications and constraints. The coefficients of the topology are also optimized simultaneously.

IV. Conclusion

This paper presents an effective genetic-based synthesis approach for automated design of ΣΔ modulator according to user defined performance specifications and constraints. Due to the complex nature of the optimization process, the algorithm has been implemented in SystemC-A which is extremely well suited for complex modeling, implementation of post-processing of simulation results and optimization algorithms. Synthesized results validate the effectiveness of the proposed methodology. In the future work, we will include the non-ideality effects of the components in the primitive library and extend the approach to support multi-loop structures synthesis.



(a) Experiment 1:Maximum SNR



(b) Experiment 2: Minimum Signal Paths

Fig. 5. Fitness improvement between generations

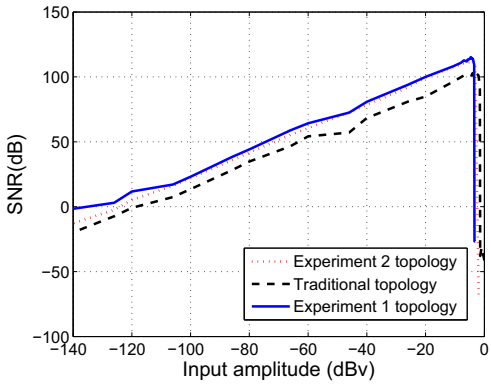


Fig. 7. SNR curves for the synthesized and traditional structures

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