

Metal-Catalyst-Free Growth of Carbon Nanotubes and Their Application in Field-Effect Transistors

T. Uchino,^{a, z} G. Ayre,^b D. C. Smith,^b J. L. Hutchison,^c C. H. de Groot,^a and
P. Ashburn^a

^a*School of Electronics and Computer Science, University of Southampton, Southampton,
SO17 1BJ, UK*

^b*School of Physics and Astronomy, University of Southampton, Southampton, SO17 1BJ, UK*

^c*Department of Materials, University of Oxford, Parks Road, Oxford, OX1 3PH, UK*

Abstract:

The metal-catalyst-free growth of carbon nanotubes (CNTs) using chemical vapor deposition and the application in field-effect transistors (FETs) is demonstrated. The CNT growth process used a 3-nm-thick Ge layer on SiO₂ that was subsequently annealed to produce Ge nanoparticles. Raman measurements show the presence of radial breathing mode peaks and the absence of the disorder induced D-band, indicating single walled CNTs with a low defect density. The synthesized CNTs are used to fabricate CNTFETs and the best device has a state-of-the-art on/off current ratio of 3×10^8 and a steep sub-threshold slope of 110 mV/dec.

^z E-mail: tu@ecs.soton.ac.uk

The excellent electrical, optical, thermal, and mechanical properties of carbon nanotubes (CNTs) have spurred research into many practical applications including nanoelectronic devices,¹ biosensors,² and via interconnects.³ For applications such as CNT sensors, integration of the sensors with Si complementary metal-oxide-semiconductor (CMOS) circuits is highly desirable. One approach to smart sensors is to fabricate the CMOS circuits before the CNT sensor fabrication.⁴ However, metal catalyzed CNT growth is typically carried out around 800°C,⁵ which is not compatible with the requirement to keep the CNT growth temperature below 500°C to avoid degradation of CMOS performance. An alternative approach is to grow the CNTs before the CMOS circuit fabrication. However, in this case, the integration of metal catalyzed CNT growth with a CMOS manufacturing process is problematic due to the metal contamination. CNT growth traditionally involves the use of metal nanoparticles as a catalyst. Transition metals such as Fe and Ni create deep levels in the Si bandgap which act as recombination centers just like Au. In this paper, the metal-catalyst-free growth of CNTs is investigated and applied to the fabrication of CNT field-effect transistors (FETs).

Several different metal-catalyst-free growth methods of CNTs have been reported,⁶⁻¹² including our earlier work on CNT growth from Ge nanoparticles.^{8,10} However to date, no device results have been reported for CNTFETs produced by any of the metal-catalyst-free CNT growth methods, mainly because it has not been possible to grow CNTs on a suitable insulator without a metal catalyst.

In this paper, the first electrical characteristics are presented on CNTFETs produced using metal-catalyst-free CNTs. The CNT growth process uses non-metallic nanoparticles produced by annealing a thin Ge film on a SiO₂ layer. Raman measurements show that radial breathing mode (RBM) peaks are present and the disorder induced D-band is absent in our samples, indicating single walled CNTs (SWNTs) with a low defect density. Electrical measurements

on completed CNTFETs show p-FET behavior and the best devices show a state-of-the-art on/off current (I_{on}/I_{off}) ratio of 3×10^8 and a steep sub-threshold slope of 110 mV/dec.

Experimental

A p^+ Si substrate ($0.005 \Omega\cdot\text{cm}$) was employed as a back gate and a 45-nm-thick thermally grown SiO_2 layer was employed as a gate dielectric. A 3-nm-thick Ge layer was deposited by either sputtering or evaporation on the SiO_2 layer. The nanoparticles on the insulator were formed at 850°C for 10 min in a mixture of Ar (1000 sccm) and H_2 (300 sccm) after a pre-anneal in H_2 (1000 sccm) at 950°C . The samples were reloaded to a hot-wall reactor and then CNT growth was performed using chemical vapor deposition (CVD) at atmospheric pressure. CNTs were grown at 850°C for 10 min using a mixture of methane (1000 sccm) and H_2 (300 sccm) immediately after a pre-anneal in H_2 (1000 sccm) at 900°C . Back gate CNTFETs were fabricated with Pd source/drain contacts. Pd was deposited by sputtering and the source/drain electrodes were formed using direct write laser lithography and lift-off. The gap between Pd source/drain electrodes was $2.0 \mu\text{m}$ and the width was $8.0 \mu\text{m}$. Typically only one or two CNTs crossed over the $2.0 \mu\text{m}$ gap between the source and drain. Electrical characteristics of CNTFETs were measured in ambient air. Raman spectra were obtained using He-Ne (632.8 nm) laser excitation.

Results and Discussion

Figure 1a shows the particle height distribution after nanoparticle formation obtained from atomic force microscopy (AFM) measurements. Line analysis shows that the peak particle count occurs at a particle height of $1.4 \pm 0.8 \text{ nm}$ and area analysis gives a mean particle density of $450 \pm 20 \text{ particles}/\mu\text{m}^2$. Figure 1b shows a typical field emission scanning electron microscope (FE-SEM) image after CNT growth. CNTs can clearly be seen, together with shorter and thicker nanowires, which have been shown to be silica nanowires in our

earlier work.^{8,10} The area density of CNTs was analyzed using several FE-SEM images from different parts of the wafer and evaluated as $3.0 \text{ CNTs}/\mu\text{m}^2$.

Energy dispersive X-ray spectroscopy analysis indicates that the nanoparticles contain a mixture of Ge, Si, and O.¹³ In order to investigate the origins of the oxygen, CNTs were grown without air exposure after the Ar/H₂ anneal. The observed area density of CNT was 3.4 CNTs/ μm^2 , compared with $3.0 \text{ CNTs}/\mu\text{m}^2$ after air exposure, which indicates that air exposure has no significant effect. This result suggests that the oxygen in the nanoparticles comes from the SiO₂ substrate in this case. These and earlier results^{11,12} suggest the following mechanism for CNT growth. As GeO₂ has a melting point of 400°C, it is likely that the nanoparticles melt during the pre-anneal at 900°C, so that CNTs are synthesized from the oxide droplets in which the carbon feedstock is dissolved. In our previous work,⁸ CNTs were grown on SiGe substrates after a carbon implantation and a chemical oxidation in H₂O₂ solution. Pre-anneal in Ar/H₂ at 1000°C was required to form the seeds for CNT growth. In this work, the process for producing the seeds is better controlled, as can be seen from the nanoparticle height distribution in Fig. 1a, and hence the process window for CNT growth is wider. The yield of CNTs obtained in this work is higher than our previous work using SiGe substrates.⁸

Figure 2a shows Raman spectra and the inset clearly shows the presence of RBM peaks, indicating that SWNTs are present. A total of 36 Raman spectra were measured and no D-band peak around 1350 cm^{-1} was observed in any of the spectra. This indicates that the CNTs have a low defect density, as was also observed in our previous work.⁸ Figure 2b shows the diameter distribution of SWNTs which is estimated from the wave number of the RBM peaks. RBM peaks have been observed with different Raman shifts from 190 cm^{-1} to the lower limit around 120 cm^{-1} . Assuming a standard formula for converting RBM peaks to diameter,¹⁴ the SWNTs have diameters in the range 1.3 - 2.0 nm. The thicker CNTs may exist but the Raman notch filter prevents the measurement for lower wave numbers.

Electrical measurements have been made on more than 150 functional back gate CNTFETs. I-V measurements showed that 77% of the devices had a high I_{on}/I_{off} ratio of more than 10^5 . Figure 3a shows sub-threshold characteristics at $V_D = -1$ V for twelve typical CNTFETs. The drain current at $V_G = -5$ V ranges from 1 to 10 μ A, the I_{on}/I_{off} ratio ranges from 2.0×10^5 to 3.0×10^8 and the sub-threshold slope (SS) ranges from 80 to 280 mV/dec. The best of our devices shows an I_{on}/I_{off} ratio of 3.0×10^8 , which compares with the best reported value in the literature of 2.5×10^7 for Pd contacted devices,¹⁵ as shown in Table I.¹⁵⁻¹⁸ Table I indicates that our metal-catalyst-free CNTFETs are able to deliver state-of-the-art values of I_{on}/I_{off} ratio and sub-threshold slope. Although many other process issues remain to be resolved with CNTFETs, such as diameter control and localization, our results nevertheless demonstrate a practical method of growing CNTs without a metal catalyst.

As the Pd source/drain electrodes deliver a good ohmic contact and p-FET behavior, the drain current at $V_G < 0$ is mainly determined by the work function of the contact metal which determines the Schottky barrier height. The drain current at $V_G = 5$ V varies widely from 10^{-12} to 10^{-8} A. This variation of drain current at $V_G > 0$ cannot be attributed to a gate leakage, because the gate of all devices is common due to the back gate transistor. Tunneling current from the Pd contact into the CNT channel is a more likely explanation for the drain current variability at $V_G > 0$. The injection of electrons from the drain electrode to the CNT channel depends on the bandgap of CNT.¹⁹ Simulations reported in the literature²⁰ predict an increase in leakage current by four orders of magnitude when the bandgap of CNTs is reduced from 0.9 to 0.45 eV. The variation of CNT diameter obtained from our Raman measurements suggests that the bandgap ranges from 0.45 to 0.7 eV. Thus variations in CNT diameter can explain most of the leakage current variability, particularly when the uncertainty in CNT diameter distribution from Raman and TEM measurements is considered.

Figure 3b shows output characteristics for one of the best CNTFETs. The output characteristics show good saturation ($V_D < -1.5$ V) and linear characteristics below saturation

($V_D > -1.5$ V). This device shows an I_{on}/I_{off} ratio of 10^7 and a sub-threshold slope of 110 mV/dec at $V_D = -1$ V.

Conclusions

We have developed a metal-catalyst-free CNT growth method that uses Ge/Si/O nanoparticles created by annealing a thin Ge film on SiO₂. As this CNT growth process does not use a metal catalyst, CNTFETs can be integrated with the front-end of a CMOS process. Raman measurements showed that RBM peaks were present and the disorder induced D-band was absent in our samples, indicating SWNTs with a low defect density. The synthesized CNTs were applied to fabricate back gate CNTFETs with Pd source/drain contacts. The best CNTFET has a state-of-the-art on/off current ratio of 3×10^8 and a steep sub-threshold slope of 110 mV/dec.

Acknowledgment

We would like to acknowledge EPSRC for supporting this work.

References

- [1] J. Appenzeller, *Proc. IEEE*, **96**, 201 (2008).
- [2] K. Besteman, J. Lee, F. Wiertz, H. Heering, and C. Dekker, *Nano. Lett.*, **3**, 727 (2003).
- [3] F. Kreupl, A. Graham, G. Duesberg, W. Steinhögl, M. Liebau, E. Unger, and W. Hönlein, *Microelectronic Engineering*, **64**, 399 (2002).
- [4] M. Haque, K. Teo, N. Rupasinghe, S. Ali, I. Haneef, S. Maeng, J. Park, F. Udrea, and W. Milne, *Nanotechnology*, **19**, 25607 (2008).
- [5] P. Nikolaev, M. Bronikowski, R. Bradley, F. Rohmund, D. Colbert, K. Smith, and R. Smalley, *Chem. Phys. Lett.*, **313**, 91 (1999).
- [6] M. Kusunoki, M. Rokkaku, and T. Suzuki, *Appl. Phys. Lett.*, **71**, 2620 (1997).
- [7] S. Botti, R. Ciardi, M. Terranova, S. Piccirillo, V. Sessa, M. Rossi, and M. Vittori-Antisari, *Appl. Phys. Lett.*, **80**, 1441 (2002).
- [8] T. Uchino, K. N. Bourdakos, C. H. de Groot, P. Ashburn, M. E. Kiziroglou, G. D. Dilliway, and D. C. Smith, *Appl. Phys. Lett.*, **86**, 233110 (2005).
- [9] D. Takagi, H. Hibino, S. Suzuki, Y. Kobayashi, and Y. Homma, *Nano Lett.*, **7**, 2272 (2007).
- [10] T. Uchino, G. Ayre, D. C. Smith, J. L. Hutchison, C. H. de Groot, and P. Ashburn, *J. Electrochem. Soc.*, **156**, K144 (2009).
- [11] B. Liu, W. Ren, L. Gao, S. Li, S. Pei, C. Liu, C. Jiang, and H. Cheng, *J. Am. Chem. Soc.*, **131**, 2082 (2009).
- [12] S. Huang, Q. Cai, J. Chen, Y. Qian, and L. Zhang, *J. Am. Chem. Soc.*, **131**, 2094 (2009).
- [13] T. Uchino, J. L. Hutchison, G. Ayre, D. C. Smith, C. H. de Groot, and P. Ashburn, *Jpn. J. Appl. Phys.*, in press.
- [14] A. Jorio, C. Fantini, M. Dantas, M. Pimenta, A. Filho, G. Samsonidze, V. Brar, G. Dresselhaus, M. Dresselhaus, A. Swan, M. Unlu, B. Goldberg, and R. Saito, *Phys. Rev. B*, **66**, 115411 (2002).

- [15] L. Rispal and U. Schwalke, *IEEE Electron Device Lett.*, **29**, 1349 (2008).
- [16] Z. Chen, J. Appenzeller, J. Knoch, Y. Lin, and P. Avouris, *Nano Lett.*, **5**, 1497 (2005).
- [17] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, *Nature*, **424**, 654 (2003).
- [18] M. Yang, K. Teo, W. Milne, and D. Hasko, *Appl. Phys. Lett.*, **87**, 253116 (2005).
- [19] J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, P. Avouris, *IEEE Trans. Electron Devices*, **52**, 2568 (2005).
- [20] J. Guo, S. Datta, and M. Lundstrom, *IEEE Tran. Electron Devices*, **51**, 172 (2004).

Table I. Comparison of the CNTFET results in this work with reported results in the literature for Pd-contacted CNTFETs.

| | This work | Rispal et al. ¹⁵ | Chen et al. ¹⁶ | Javey et al. ¹⁷ | Yang et al. ¹⁸ |
|---------------------|-------------------|-----------------------------|---------------------------|----------------------------|---------------------------|
| I_{on}/I_{off} | 3.0×10^8 | 2.5×10^7 | 2.0×10^7 | 4.0×10^6 | 2.0×10^6 |
| SS (mV/dec) | 110 | 170 | 120 | 150 | 560 |
| I_{on} (μ A) | 3.0 | 3.7 | 4.0 | 20 | 2.0 |
| I_{off} (pA) | 0.01 | 0.15 | 0.2 | 5.0 | 1.0 |

FIGURE CAPTIONS

Fig. 1 (a) Histogram of the nanoparticle height distribution just after nanoparticle fabrication obtained from AFM measurements. The nanoparticles were produced by annealing a 3-nm-thick Ge film on SiO₂ in Ar/H₂ for 10 mins at 850°C after a pre-anneal at 950°C in H₂. (b) FE-SEM image after CNT growth.

Fig. 2 (a) Raman spectra of CNTs grown from the Ge nanoparticles. All of 36 measured Raman spectra show no D-band peak, indicating a low defect density. The inset shows RBM peaks, indicating that SWNTs are present. (b) Diameter distribution of CNTs which is estimated from the RBM peaks. Thicker CNTs with a diameter of more than 2.0 nm may exist but the Raman notch filter prevents measurements at lower wave numbers.

Fig. 3 Electrical characteristics for Pd contacted back gate CNTFETs (channel length is around 2.0 μm) produced using metal-catalyst-free CNTs grown from a thin Ge film on SiO₂. The gate insulator was a 45-nm-thick SiO₂ layer. (a) Twelve typical sub-threshold characteristics at V_D = -1 V. (b) Output characteristics for V_G = -1.0, -1.5, -2.0, -2.5 V.

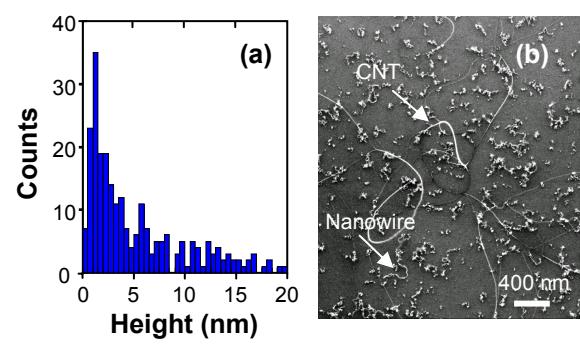


Fig. 1

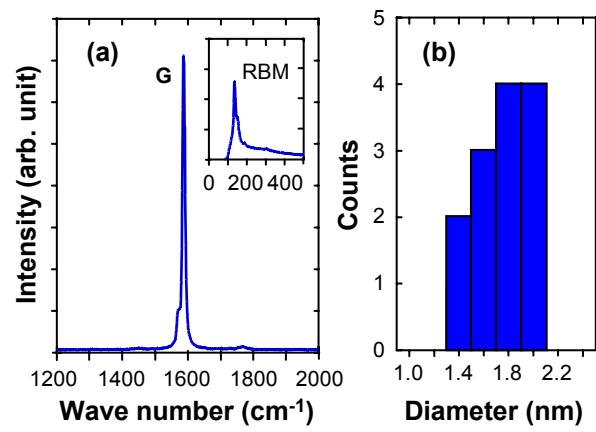


Fig. 2

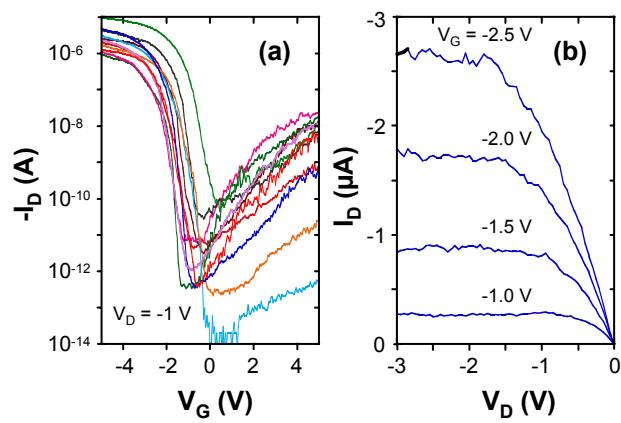


Fig. 3