Improved Drive Current in RF Vertical MOSFETS Using Hydrogen Anneal

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***Abstract*—This letter reports a study on the effect of a hydrogen anneal after silicon pillar etch of surround-gate vertical MOSFETs intended for RF applications. A hydrogen anneal at 800 °C is shown to give a 30% improvement in the drive current of 120-nm n-channel transistors compared with transistors without the hydrogen anneal. The value of drive current achieved is 250 μA/μm, which is a record for thick pillar vertical MOSFETs. This improved performance is obtained even though a sacrificial oxidation was performed prior to the hydrogen anneal to smooth the pillar sidewall. The values of subthreshold slope and DIBL are 79 mV/decade and 45 mV/V, respectively, which are significantly better than most values reported in the literature for comparable devices. The H_2 anneal is also shown to decrease the OFF-state leakage current by a factor of three.**

***Index Terms*—Fillet local oxidation (FILOX), hydrogen anneal, vertical MOSFET.**

I. Introduction

Surround-gate thick pillar vertical MOSFETs are being researched because they offer a high drive current per unit silicon area and can be easily integrated in a mature CMOS technology for low-cost RF transistors [1]–[5]. One of the challenges of vertical MOSFETs for this application is susceptibility to surface roughness and etch damage on the sidewalls of the silicon pillar. Sidewall roughness and etch damage are caused by lithography and reactive ion etching (RIE) processes and give rise to mobility degradation due to surface roughness scattering. Dry etch damage also occurs during polysilicon gate etch, and we have recently shown how the device architecture and the Fillet local oxidation (FILOX) process can be optimized to eliminate damage during gate etch [6]. Pillar sidewall roughness is usually reduced by means of sacrificial oxidation, which has the effect of smoothing the sidewall surface. The surface morphology of silicon is also known to be affected by hydrogen (H_2) annealing and has been investigated in the past for FinFET technology [7]. At nanometer pillar dimensions, the smoothing of the fin surface is easily achieved by H_2 anneal, but in thick pillar vertical MOSFETs, it is not clear that the H_2 anneal will have such a significant beneficial effect. To date, there have been no reports in the literature on the effects of such annealing on the performance of vertical MOSFETs.

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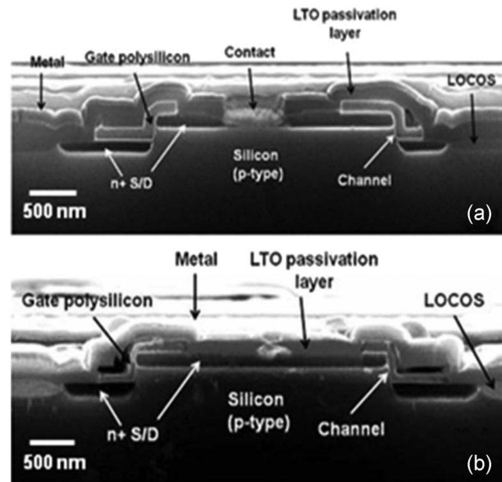

Fig. 1. Cross-sectional SEM image of the completed surround-gate vertical MOSFETs (a) without and (b) with H_2 anneal.

In this letter, we, therefore, report, for the first time, the effect of H_2 annealing on the characteristics of vertical MOSFETs with large pillar dimensions. It is shown that H_2 annealing gives a significant improvement in drive current even after a sacrificial oxidation has been performed. H_2 annealing of 120-nm n-MOSFETs also has an excellent subthreshold slope of 79 mV/decade and a DIBL of 45 mV/V.

II. Device Fabrication

Boron-doped (0.75–1.25 $\Omega \cdot$ cm) (100) wafers were taken as the starting material, and a p-type body was formed by boron implantation (2×10^{14} cm^{-2}, 100 keV) and a thermal drive in. Then, oxide "hard mask" was formed, and RIE was used to define a 350-nm Si pillar. To eliminate the dry etch damage and to reduce the surface roughness on the pillar sidewall, a 20-nm oxide layer was grown by dry oxidation at 900 °C and was stripped off using an HF dip. The H_2 anneal was performed for 3 min in an ASM Epsilon II epitaxial reactor in 100% H_2 at a pressure of 40 torr and a temperature of 800 °C. Then, a so-called Frame-gate FILOX vertical MOSFET was implemented in these Si pillars in a mature CMOS technology using 0.5-μm SCMOS design rules, full details of which are given in [6].

III. Results

Fig. 1 shows the cross-sectional SEM micrographs of the completed Frame-gate vertical MOSFET (a) without and

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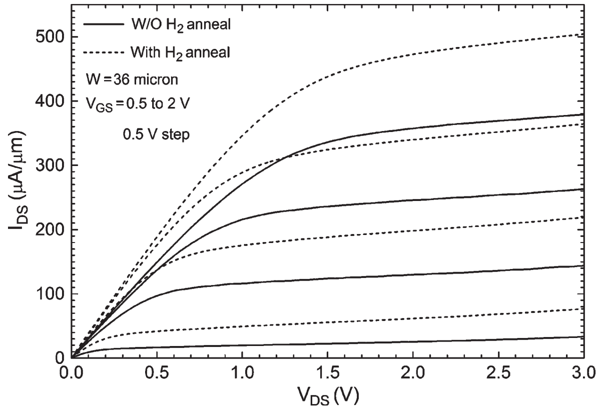

Fig. 2. Comparison of output characteristics of 120-nm n-channel surround-gate vertical MOSFETs with and without a H_2 anneal during the DOT mode of operation.

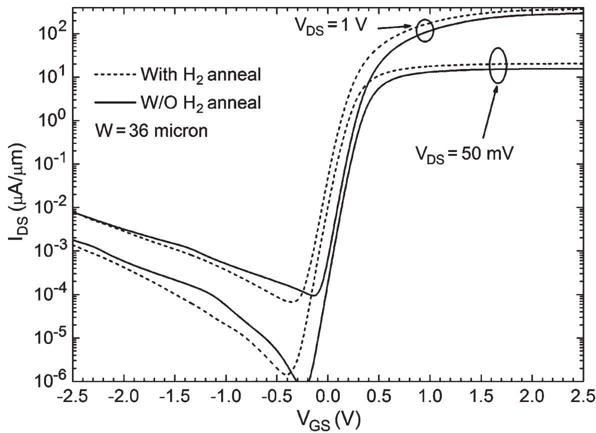

Fig. 3. Transfer characteristics of 120-nm n-channel surround-gate vertical MOSFETs with and without H_2 anneal during the DOT mode of operation.

(b) with a H_2 anneal after stain etch. No significant difference in the pillar height and width could be found for the devices with and without a H_2 anneal. The devices exhibit identical values of junction depth (190 nm) and channel length (120 nm). Similarly, high magnification images showed no discernable difference in pillar shape after H_2 anneal.

Fig. 2 shows the output characteristics of 120-nm surround-gate vertical MOSFETs with and without H_2 anneal during the drain-on-top (DOT) mode of operation. The H_2 annealed transistor shows a significantly improved drive current in comparison to the device without H_2 anneal. The drive currents for a gate voltage overdrive of 1 V and a $V_{\rm DS}$ of 1.5 V are found to be 250 and 190 μA/μm for devices with and without H_2 anneal, respectively, indicating a 30% drive current improvement. Measurements were performed on multiple transistors with a variety of different channel widths, and a similar 30% improvement in performance was observed at all widths. A similar trend was also observed for source-on-top (SOT) operation.

Fig. 3 shows the transfer characteristics of 120-nm surround-gate vertical MOSFETs during the DOT mode of operation. For the device without H_2 anneal, a subthreshold slope of 80 mV/decade and a DIBL of 40 mV/V are observed. For the H_2 annealed device, a similar subthreshold characteristic is observed with a subthreshold slope and DIBL of 79 mV/decade and 45 mV/V, respectively. However, the H_2 anneal appears to have

TABLE I

COMPARISON OF RESULTS OF THE 120-nm SURROUND-GATE VERTICAL MOSFETs WITH AND WITHOUT H_2 ANNEAL WITH REPORTED RESULTS FROM THE LITERATURE. $I_{\rm on}$ HAS BEEN CALCULATED FOR $V_{\rm DS} = V_{\rm DD}$ AND FOR A 1-V GATE OVERDRIVE. TO ENSURE A MEANINGFUL COMPARISON, FULLY DEPLETED THIN PILLAR VERTICAL MOSFETs ARE EXCLUDED FROM THE TABLE

Parameter	L (nm)	t_{ox} (nm)	N_A (10^{17}/cc)	V_{DD} (V)	Ion (μA/μm)	S (mV/dec)	DIBL (mV/V)
Schulz et al [1]	100	3	20	1.5	240	102	70
Schulz et al [1]	50	3	70	1.5	80	166	300
VRG [3]	100	2.8	35	1.5	140	90	30
VRG [3]	50	2.8	35	1.5	100	105	90
Mori et al [4]	100	7	20	1.5	160	100	73
Gili et al [2]	125	3	40	1.5	127	107	80
Frame gate (w/o H_2 anneal)	120	2.8	10	1.5	190	80	40
Frame gate (with H_2 anneal)	**120**	**2.6**	**10**	**1.5**	**250**	**79**	**45**

reduced the threshold voltage (V_T). While the device without H_2 anneal exhibited a threshold voltage of 0.28 V, the threshold voltage of the H_2 annealed device is found to be reduced to a value of 0.20 V. H_2 annealing also reduces the OFF-state leakage current which is around a factor of three for a drain bias of 50 mV. A similar effect of the H_2 anneal is observed for SOT mode of operation.

IV. DISCUSSION

The aforementioned results show that the beneficial effects of H_2 anneal can be exploited on thick pillar vertical MOSFETs suitable for RF applications in a mature CMOS technology. Table I compares the electrical results of our vertical MOSFETs with other such devices reported in the literature. As can be seen, the H_2 annealed device has a state-of-the art value of drive current, as well as maintaining excellent values of subthreshold slope and DIBL. While the majority of the devices exhibits a drive current of $\leq 200\ \mu$A/μm at the bias conditions presented in Table I, the H_2 annealed device exhibits a drive current of 250 μA/μm even though the device has a slightly longer channel length of 120 nm. We have also compared the silicon area of our fabricated vertical MOSFETs with comparable lateral MOSFETs using 0.5-μm design rules, and it is found that the vertical MOSFETs give a 53% area saving for a 36-μm channel width. The peak transconductances (G_M) of H_2 annealed transistors were measured, and the values of 1.4×10^{-3} and 1.1×10^{-2} A/V were obtained for $V_{\rm DS} = 0.05$ and 1 V, respectively, which are noticeably better than those reported for planar MOSFETs with comparable 0.5/0.7-μm technology [8], [9] and also better than some aggressively scaled planar MOSFETs reported in [9] and [10]. This beneficial effect of the H_2 anneal could be integrated with our recently reported FILOX process for overlap capacitance reduction and silicidation process for S/D series resistance reduction [5] to deliver a significant benefit from VMOS devices for RF applications in mature lateral CMOS technologies.

The improved drive current in the 120-nm H_2 annealed device can be explained by surface smoothing due to the H_2 anneal and also by reduction of the interface state density $(D_{\rm it})$ [7]. Hence, the mobility degradation associated with surface roughness scattering is reduced, thereby giving a drive current improvement. However, the H_2 anneal also gives a V_T reduction

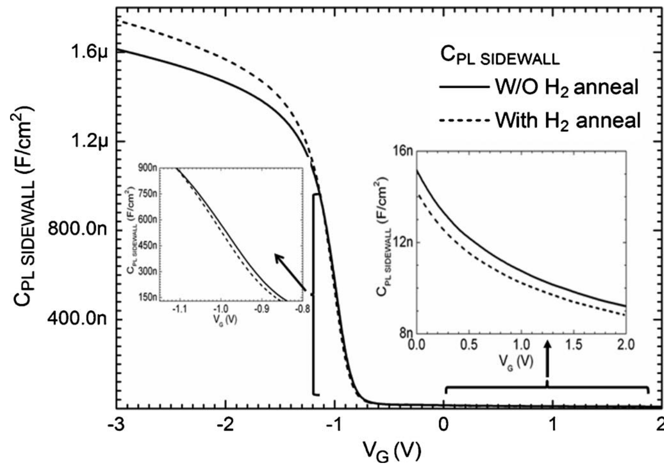

Fig. 4. Measured pillar sidewall capacitance ($C_{\mathrm{PL\,SIDEWALL}}$) as a function of voltage. Results are presented for capacitors with and without H_2 anneal.

of around 80 mV. Such a reduction of V_T has also been reported for H_2 annealed FinFETs in the past and has been explained by the loss of fin width and height due to the H_2 anneal [7]. However, Fig. 1 shows that, for the thick pillar vertical MOSFETs of this letter, there is no noticeable loss of pillar height and width due to the H_2 anneal, and hence, V_T reduction in these devices merits discussion.

Fig. 4 shows $C_{\mathrm{PL\,SIDEWALL}}$ measured at 1 MHz as a function of gate voltage for pillars with and without H_2 anneal. These measurements were performed on sidewall test capacitors, which were realized by dry etching of the gate polysilicon. As can be seen, the accumulation capacitance in the H_2 annealed capacitor is significantly higher than that in the unannealed capacitor. The gate oxide leakage currents in the two types of capacitors are identical, and hence, this implies that the gate oxide in the H_2 annealed capacitor is thinner than that in capacitors without H_2 anneal. This is understandable as a rough surface, and dangling bonds usually favor oxidation. Using the method described in [11], the estimated gate oxide thicknesses are found to be 2.6 and 2.8 nm for the devices with and without H_2 anneal, respectively. A 0.20-nm reduction of oxide thickness accounts for approximately half (36 mV) of the observed 80-mV V_T reduction and contributes to only 8% of the observed drive current improvement. The rest of the 44 mV of V_T reduction can be explained by a reduction in the acceptor-type interface state density in the upper half of the Si bandgap, as can be seen from the slightly steeper slope and reduced $C_{\mathrm{PL\,SIDEWALL}}$ in inversion for the hydrogen annealed capacitor (inset in Fig. 4). Evidence of such a reduction in D_{it} is also apparent from the reduced OFF-state leakage of the H_2 annealed transistor (Fig. 3), as interface states are known to enhance GIDL in MOSFETs [12]. The symmetry in the observed GIDL and V_T reductions during DOT and SOT operation of the H_2 annealed transistors implies a similar D_{it} reduction at the pillar top and bottom. A lower D_{it} near the S/D regions would reduce GIDL, while a reduced D_{it} in the channel would affect V_T. A rough estimation of the D_{it} reduction can be obtained from the V_T reduction in the H_2 annealed transistor which is found to be 3.5×10^{11} cm^{-2}. Theoretically, such a reduction of D_{it} has a minor effect on the subthreshold slope (1.5 mV/decade).

V. Conclusion

Hydrogen anneal at 800 °C has been applied after silicon pillar etch and sacrificial oxidation to improve the surface roughness of thick pillar vertical MOSFETs suitable for RF applications in a mature CMOS technology. It has been shown that the hydrogen anneal gives a significantly increased drive current and a three times lower OFF-state leakage. For 120-nm channel length transistors, the hydrogen anneal gives a 30% improvement in drive current in comparison to devices without the hydrogen anneal. The values of drive current achieved constitute the state of the art for thick pillar vertical MOSFETs. The transistors also have an excellent subthreshold slope of 79 mV/decade and a DIBL of 45 mV/V. The electrical results show that the hydrogen anneal has reduced the threshold voltage by approximately 0.08 V. Capacitance/voltage measurements have shown that this can be explained by a combination of a thinner gate oxide and a reduced acceptor-type interface state density on the hydrogen-smoothed pillar sidewall.

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