

# Silicon Compatible ZnO Nanowire FET: Modeling and Simulation

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## INTRODUCTION

Zinc oxide is a II-VI compound semiconductor, which crystallizes in the wurtzite phase and has a wide direct band gap of 3.37 eV and has seen applications in electronics, MEMS and optoelectronic devices.

### Advantages of ZnO semiconductor:

1. Silicon compatible fabrication process
2. Lower temperature growth than polysilicon with higher electrical performance
3. High mobility transistor performance in field effect transistor (FET), visible light emitter and chemical sensors [1][8].
4. Cost effective thin film material for electronics and optoelectronics application

### Issues:

1. Controlling the dopant density in ZnO because ZnO is intrinsically n-type
2. Debatable n-type conductivity (oxygen vacancies, zinc interstitials or other impurities)
3. Little work on integration with Si material in the nanoscale
4. High surface defect states especially in nanowires which have higher surface-to-volume ratio [6]

### Objective:

Based on these issues, the main objective of this work is to:

1. To model the ZnO nanowire based on its surface defect states using Silvaco ATLAS simulation tool
2. Simulate the model and compare with experimental data for verification
3. To study the properties of defects that exist from different fabrication process

## REVIEW OF FABRICATED DEVICES

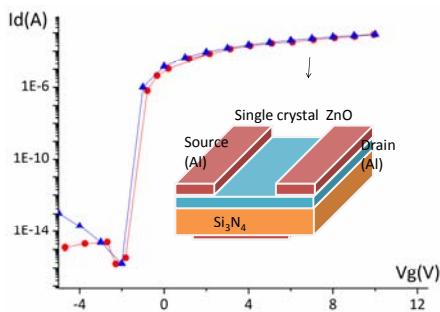
Thin Film	Fabrication method	I (on) / I (off)	Field Mobility (cm <sup>2</sup> /Vs)
Fortunato et al (2004)	RT sputter	3e5 @ Vd=20V	27
Hossain et al(2004)	Pulsed Laser Deposition	1e6 @ Vd=0.1V	5.26
Hirao et al(2007)	RF sputter	4.6e6 @ Vd=10V	50.3
C. C. Liu et al (2009)	RT sputter (RT)	1.4 e6 @ Vd=20V	117
Nanowire			
Chang et al(2006)	Vapor Trap Passivate SiO <sub>2</sub> /Si <sub>3</sub> N <sub>4</sub>	1e3 @ Vd=0.5 V 1e4 @ Vd=5mV	30 3118
Ra et al (2008)	ALD ZnO	1e5 @ Vd=0.2V	80
Park et al (2004)	Catalyst-free MOVPE With passivation polyimide	1e7 @ Vd=1V 1e5@ Vd=1V	75 1000
Sakurai et al(2009)	Ga-doped VLS	-	42
<b>This work</b>	<b>ALD and VLS</b>	<b>&lt;1e6 @ Vd=1V</b>	<b>&gt; 75</b>

### Simulation considerations:

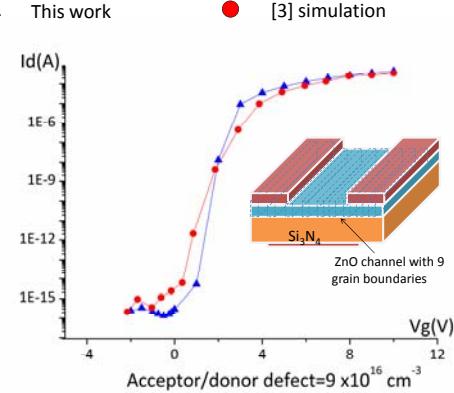
1. The surface defect states deteriorate the mobility, on/off ratio and subthreshold swing, thus the interface states of nanowire/thin film-insulator is important
2. High surface trap states leads to high subthreshold slope
3. Due to interface traps, additional capacitance will exist that leads reduction in mobility

## RESULTS & DISCUSSION

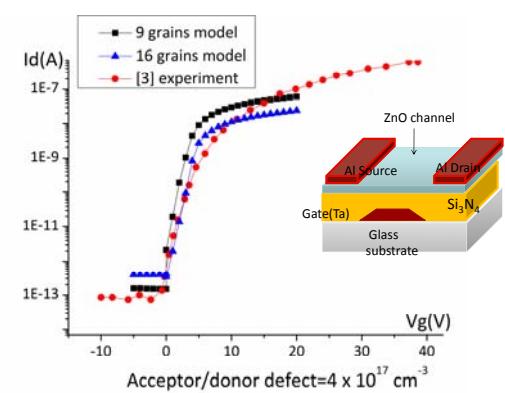
→ ZnO TFT simulation and comparison to [3]



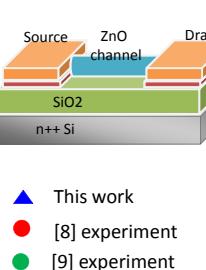
▲ This work



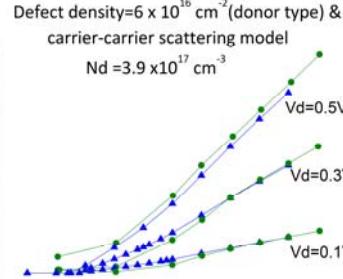
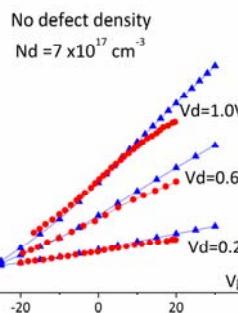
● [3] simulation



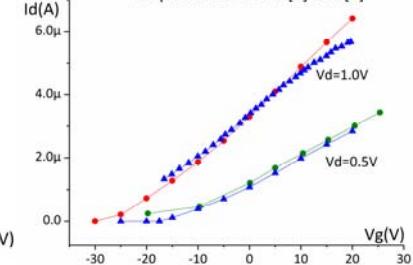
→ ZnO nanowire model verification with experimental results [8][9]. 3D nanowire simulation.



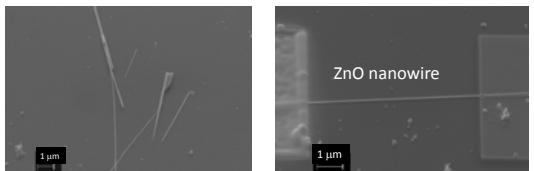
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● [8] experiment  
● [9] experiment



Comparison between [8] and [9]



## FUTURE WORK



1. Characterization of single ZnO nanowires-I-V characterization and Raman Spectra
2. Fabricate the nanowire into Field Effect Transistor by top-down and bottom-up technique that can be applied in biosensor, electronics gate etc

## CONCLUSION

1. Different fabrication method cause defect densities to be varied.
2. Defects and carrier scattering lead to low carrier mobility.
3. It is important to understand defect reductions mechanism based on model and experimental results
4. Successfully used Silvaco ATLAS device simulator to study the trap states and defect distribution that exist in ZnO based devices
5. Excellent agreement of thin film and nanowire model with experimental results.

## REFERENCES

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