Statistical Power Analysis for Nanoscale CMOS

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***Abstract*— With the scaling down of CMOS technology, process variations are becoming significant. Power consumption is a major constraint on IC yield. However, there has been little research on statistical power analysis compared with that on timing analysis. Here, both the static and dynamic power are considered. We characterize a cell library containing mean power. A standard deviation power library is extracted from Monte Carlo simulations. Then, the mean and variance of the power are derived. The proposed technique is validated on benchmark circuits at 35 nm. We compare the results with SPICE simulations and show that the difference is acceptable.**

I. INTRODUCTION

In the manufacture of nanoscale CMOS integrated circuits (IC), more and more process variations arise due to the limitations of physics and technology [1], [2]. Process variations can be systematic or random, the former are deterministic and predictable but the latter are uncertain and include extrinsic and intrinsic variations. The intrinsic variation is due to atomic level fluctuations and occurs within a die, which is regarded as the main source of process variations at nano scales. The effects include random discrete doping (RDD), line-edge roughness (LER), oxide thickness (t_{ox}) roughness (OTR) and poly-silicon granularity (PSG) [1]–[5].

Process variations lead to variations in device characteristics and IC performance. Timing performance used to be taken as the IC yield criterion. However, with shrinking gate length (L), t_{ox} and threshold voltage (V_{th}), the leakage power increases exponentially and limits IC yield for low power applications at 65 nm technology and below [6]. On the other hand, because delay is inversely proportional to the dynamic power, the best chips from the timing viewpoint may dissipate unacceptable power. Therefore, industries and designers are concerned about the trade-off between performance, power and yield (PPY) [6]–[10].

Statistical timing analysis has been investigated intensively in the last decade [11], but there has been little research on power variation. Power includes static and dynamic components. It is a critical parameter affecting packaging, cooling, battery lifetime and chip reliability. The static power (SP) is induced by leakage current and includes subthreshold leakage (I_{sub}) and gate leakage (I_{gate}); both increase significantly with decreasing L, t_{ox} and V_{th} [6]. The dynamic power (DP) includes short circuit power and power dissipated by charging and discharging of internal and external load capacitances. The increase of process variation gives rise to more uncertainty in L, t_{ox} and V_{th}, which are considered as the main culprits for timing and power fluctuations [10],[12]. Although statistical analysis of leakage power has been reported [6],[9],[10],[13]–[15], similar investigations of DP have not been widely done up to now. Moreover, the statistical power analysis by Monte Carlo (MC) SPICE simulations is time-consuming and impractical for large scale designs. Therefore, a usable statistical power analysis technique is needed.

In this paper, we present a statistical power analysis technique for nanoscale CMOS design. Variation in V_{th} (σV_{th}) is taken to represent intrinsic process variations and V_{th} is assumed independent and Gaussian distributed, which is acceptable for in-die analysis [4]. SP and DP are statistically analyzed by the proposed technique based on two cell libraries. One is a standard cell library (SCL) written with mean powers (μ_P) from MC simulations. μ_P of a design is extracted from the SCL by gate-level analysis. The other library is called the standard deviation library of power (SDLP), containing standard deviations (σ) of SP (σ_{SP}) and DP (σ_{DP}) at specific input transition times (t_r/t_f) and load capacitance (C_L). σ_{SP} and σ_{DP} of cells are extracted from the SDLP, and σ_P of a design is calculated by statistically adding all the cells' σ_{SP} and σ_{DP}. The validity of the proposed technique is verified by comparing with MC method on ISCAS benchmark circuits at 35 nm.

II. POWER VARIATION OF CMOS CELLS DUE TO INTRINSIC VARIATIONS

A. INTRINSIC VARIATION MODELLING

The main sources of intrinsic variations are RDD, LER and PSG for "bulk" MOSFETs with polysilicon gates [16]. Simulations demonstrate that σV_{th} induced by the three sources is almost the same as the total σV_{th} measured at 45 nm [16]. RDD results from fluctuations of dopant number and doping profile in the device active region, which are hard to control as the dopant number and gate area get smaller [2]. It is found that σV_{th} from RDD has a power law relationship with doping density and is inversely proportional to the square root of gate area [1]. LER is due to incident photon number variation during lithography exposure, absorption rate and chemical attributes of photoresist [1]. It gives rise to significant L variation at sub-50 nm. PSG has been identified as an important source

TABLE I

STATIC POWER VARIATION OF STANDARD CMOS CELLS

CELLS	STATES	μ_{SP} (nW)	σ_{SP} (nW)
INVERTER	A	10.18	12.13
INVERTER	!A	3.947	4.213
NAND	!A & !B	0.381	0.305
NAND	!A & B	3.988	4.421
NAND	A & !B	2.806	2.722
NAND	A & B	21.09	18.17
NOR	!A & !B	7.882	5.940
NOR	!A & B	7.498	8.269
NOR	A & !B	10.31	12.18
NOR	A & B	0.649	0.645

of intrinsic fluctuations, because of the diffusion along the grain boundaries and penetration of dopants through the gate oxide into the channel from the high doping regions in the gate [16].

The V_{th} variation from the above three combined sources is assumed to be Gaussian [4], [5]. In this work, variations in V_{th} are used to represent the effects of intrinsic variations on device characteristics. Simulation of power dissipations is done by using σV_{th}=30mV as an input parameter for 35 nm MOSFET models [17]. The BSIM4 models are extracted by a 3D atomistic simulator [2].

B. STATIC POWER VARIATIONS

The power dissipated by a MOSFET in steady state is known as static or leakage power, for which the dominant source is the I_{sub} formed by the diffusion of minority carriers in the off state. I_{sub} varies exponentially with V_{th}, assuming L_{eff}, W_{eff} and t_{ox} are constants [10]. Fig. 1 shows the dependence of SP on V_{th} for a CMOS inverter. SP at low and high inputs is determined by the n- and p-MOSFETs, respectively. It is reported that subthreshold leakage power will reach up to 50% of the total power for mobile systems at 65 nm technology [13]. Moreover, because of the exponential dependence on V_{th}, SP is more affected by process variations.

$$\Delta I_{sub} = -I_{sub}\frac{\Delta V_{th}}{nV_T} \tag{1}$$

At room temperature and $n \approx 1$, a 30mV σV_{th} results in ΔI_{sub} with almost the same value as the nominal I_{sub}. Increasing ΔI_{sub} has an adverse influence on power yield for lower power products. Table I shows the μ_{SP} and σ_{SP} of INVERTER, 2-input NAND and 2-input NOR for 10 000 MC simulations with 30mV σV_{th}. It is found that μ_{SP} and σ_{SP} are approximately the same for the cells; this is consistent with the prediction of equation (1). In addition, SP from a p-MOSFET is larger than that from an n-MOSFET because I_{0P} is several times I_{0N} from the definition. The SP difference between the low and high input of INVERTER confirms the above analysis.

C. DYNAMIC POWER VARIATIONS

Dynamic power dissipation occurs when a stimulus is applied to the circuit irrespective of whether the output logic changes or not and is composed of internal and switching

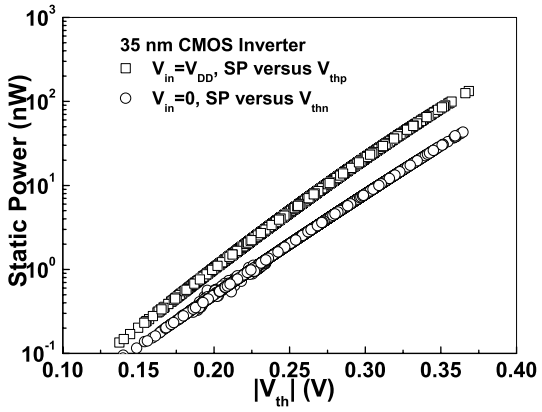

Fig. 1. The dependence of static power on V_{th} of 35 nm CMOS inverter.

power. The internal power dissipated within a cell includes short circuit power (P_{SC}) during the inputs transition procedure as both n- and p-MOSFETs switch on simultaneously, and the power consumed on charging and discharging the internal load (P_{int}). The switching power (P_{SW}) of a driving cell is dissipated by the load capacitance at the output of the cell.

$$DP = P_{SC} + P_{int} + P_{SW} \tag{2}$$

All three components have a dependence on the input t_r/t_f; P_{SC} is also affected by device dimensions and V_{th}; P_{int} is determined by cell properties; and P_{SW} is influenced by C_L. In cell-based IC design, DP is extracted from two-dimensional lookup tables characterizing DP at pre-specified t_r/t_f and C_L. To investigate the dependence of σ_{DP} on switching speed and C_L at constant σV_{th} while ignoring fluctuations of L and t_{ox}, MC simulations are done under different conditions. Fig. 2 shows the σ_{DP} of INVERTER, NAND and NOR gate with (a) input slew and (b) C_L varying, data points are extracted by 10 000 iterations MC simulations. It is seen that the σ_{DP} are affected by both t_r/t_f and C_L for all the cells. Therefore, we propose to extract the σ_{DP} of cells from a newly generated cell library written with the simulation data. This is described in the next section.

III. STATISTICAL POWER ANALYSIS

We select σV_{th} to reflect the intrinsic variations and ignore fluctuations of L and t_{ox} for demonstrating our SPA technique. Firstly, the statistical analysis of SP for standard cells is done by MC simulations, μ_{SP} and σ_{SP} (Table I) are obtained and written to the SCL and SDLP, respectively. From gate-level analysis, the probabilities of different static values (PS) can be obtained. PS is determined by circuit configuration and input waveforms. SP of a cell is the leakage powers of static values multiplied by the corresponding PS.

$$\mu_{SPC} = \mu_{SP1} \times PS_1 + \mu_{SP2} \times PS_2 + \cdots \tag{3}$$

$$\sigma^2_{SPC} = (\sigma_{SP1} \times PS_1)^2 + (\sigma_{SP2} \times PS_2)^2 + \cdots \tag{4}$$

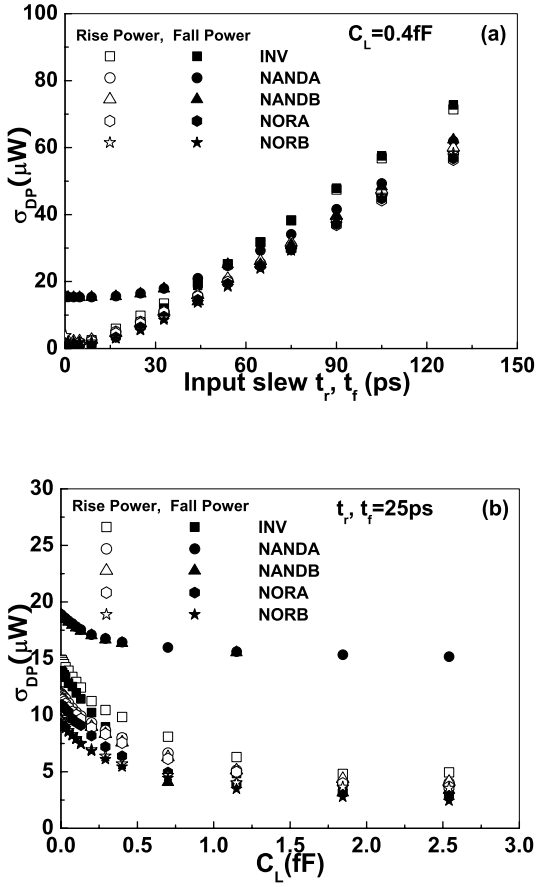

Fig. 2. σ_{DP} of INVERTER, NAND and NOR at 35 nm with (a) input slew and (b) FO varying at σV_{th}=30mV. NANDA(B), NORA(B): output transition activated by input signals at input A(B).

The μ_{SP} and σ_{SP} of a design is then calculated by,

$$\mu_{SPD} = \mu_{SPC1} + \mu_{SPC2} + \mu_{SPC3} + \mu_{SPC4} + \cdots \quad (5)$$

$$\sigma^2_{SPD} = \sigma^2_{SPC1} + \sigma^2_{SPC2} + \sigma^2_{SPC3} + \sigma^2_{SPC4} + \cdots \quad (6)$$

Then, we characterize DP for the SCL and SDLP. The SCL includes lookup tables of energy dissipations during input transitions at different t_r/t_f and C_L. The values are mean energy dissipations obtained from MC simulations. DP is affected by both the frequency (f) of input signals and the switching activities of cells. The μ_{DP} of a cell is extracted by gate-level analysis from the SCL, and the design's μ_{DP} is sum of that of all cell DP. The σ of energy dissipations from MC simulations are written to the SDLP, so σ_{DP} of cells and design can be extracted from it.

$$\mu_{DPD} = \mu_{DPC1} + \mu_{DPC2} + \mu_{DPC3} + \mu_{DPC4} + \cdots \quad (7)$$

$$\sigma^2_{DPD} = \sigma^2_{DPC1} + \sigma^2_{DPC2} + \sigma^2_{DPC3} + \sigma^2_{DPC4} + \cdots \quad (8)$$

The total power and its variation of a design is obtained by the sum of SP and DP of all cells,

$$\mu_P = \mu_{SPD} + \mu_{DPD} \quad (9)$$

$$\sigma^2_P = \sigma^2_{SPD} + \sigma^2_{DPD} \quad (10)$$

Because the power values of the libraries are extracted by MC method, accuracy of the proposed technique should be comparable with transistor-level SPICE simulation.

IV. RESULTS AND DISCUSSION

First, the proposed SPA technique is used to analyse SP of ISCAS benchmark circuits. Table II is the statistical analysis of SP by SPA and MC simulations. 10 000 iterations MC are done at 30mV σV_{th} without input stimulus. It is found the maximum difference between the two methods in both μ_{SP} and σ_{SP} is 2.15%.

Then, the SPA is applied to ICs with different input signals, of which both SP and DP are involved. μ, σ of SP and DP are extracted by the same procedure from the SCL and SDLP, respectively. MC simulations are done by supplying the same input stimulus. MC method simulates the total power but cannot distinguish proportions of SP and DP. So, the comparison of total power between the SPA and MC method is given.

We analyse power variations of ISCAS-85 C432, a 27-channel interrupt controller synthesized to 192 standard cells. Table III shows comparisons between the results of the proposed SPA and MC simulations. The powers are analysed at different operating frequencies with different combinations of input stimulus, which are selected randomly. The differences in μ_P and σ_P between SPA and MC are several percent for all selected inputs combinations. Fig. 3 shows power distributions operating at 100MHz analysed by the SPA and MC method, distribution of SPA is produced by assuming Gaussian and using the extracted μ, σ. The distributions from the two methods are close to each other in the figure, confirming the validity of the SPA.

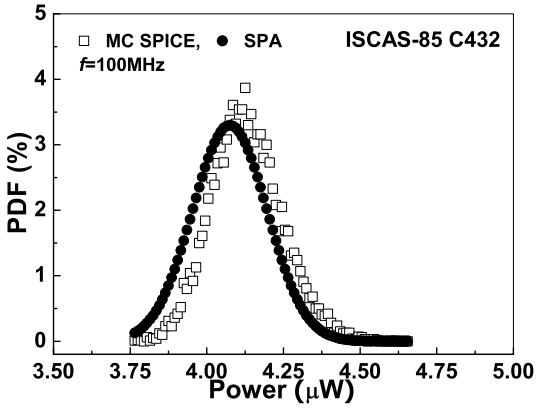

Fig. 3. Power distributions of ISCAS C432 at 100MHz.

V. CONCLUSIONS

In this work, we presented a SPA technique to analyse both static and dynamic power. The proposed SPA technique

TABLE II

STATISTICAL ANALYSIS OF STATIC POWER FOR ISCAS BENCHMARK CIRCUITS BY SPA AND MC SIMULATIONS

ISCAS	Cells no.	μ_{SPA} (μW)	μ_{MC} (μW)	Errors (%)	σ_{SPA} (nW)	σ_{MC} (nW)	Errors (%)
74182	21	0.1371	0.1371	0.00	36.52	35.75	2.15
74283	56	0.4515	0.4519	0.09	74.26	73.35	1.24
74L85	65	0.5255	0.5238	0.32	76.49	75.33	1.54
74181	96	0.7311	0.7292	0.26	89.88	88.49	1.57
C432	192	1.4930	1.4904	0.17	128.5	127.3	0.94
C6288	3431	23.500	23.458	0.18	523.5	516.3	1.39

TABLE III

COMPARISON OF POWER VARIATIONS OF ISCAS C432 BETWEEN THE PROPOSED SPA AND MC SIMULATIONS

f	μ_{SPA-SP}	μ_{SPA-DP}	σ_{SPA-SP}	σ_{SPA-DP}	μ_{SPA}	μ_{MC}	Errors	σ_{SPA}	σ_{MC}	Errors
Hz	μW	μW	nW	nW	μW	μW	%	nW	nW	%
100M	1.471	2.604	120.72	14.39	4.075	4.131	1.36	121.57	115.91	4.89
200M	1.511	6.693	121.06	32.49	8.204	8.136	0.84	125.34	118.31	5.94
333M	1.510	10.96	120.82	53.22	12.47	12.37	0.81	132.02	125.61	5.10
500M	1.509	16.10	120.56	78.16	17.61	17.46	0.85	143.67	136.49	5.27
800M	1.508	24.82	118.75	121.3	26.33	26.13	0.76	169.75	159.27	6.58
1.00G	1.749	27.72	139.85	184.66	29.47	30.43	3.16	231.58	231.24	0.15
1.00G	1.521	42.19	117.95	177.40	43.71	43.97	0.59	213.03	202.61	5.14

extracts powers by extrapolating from cell libraries characterized by Monte Carlo (MC) simulations. The standard cell library (SCL) contains the mean values (μ) and the standard deviation (σ) library of power (SDLP) includes the σ of static and dynamic powers. μ_P and σ_P of cells in a design are extracted by gate-level analysis from the SCL and SDLP, respectively. μ_P and σ_P of a design is the statistical sum of that of cells. Power variations of ISCAS benchmark circuits at 35 nm with 30mV of σV_{th} are analysed by using the proposed SPA technique and MC method; the errors of SPA compared with MC are acceptable.

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