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Improved sub-threshold slope in short-channel vertical MOSFETs using FILOX oxidation

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ABSTRACT

This paper investigates the origins of sub-threshold slope degradation in vertical MOSFETs (v-MOSFETs) due to dry etching of the polysilicon surround gate. Control v-MOSFETs exhibit a degradation of sub-threshold slope as the channel length is reduced from 250 to 100 nm, with 100 nm transistors having a value of 125 mV/dec and a DIBL of 210 mV/V. The effect of the polysilicon gate etch is investigated using a frame-gate architecture in which the polysilicon gate overlaps the side of the pillar, thereby protecting the channel from etch damage. This device shows no degradation of short channel effects when the channel length is scaled and exhibits a near-ideal sub-threshold slope of 76 mV/dec and a DIBL of 33 mV/V at a channel length of 100 nm. Gated diode measurements unambiguously demonstrate that this improved sub-threshold slope is due to the elimination of etch damage at the top and bottom of the pillar created during polysilicon gate etch. An alternative method of eliminating dry etch damage is then investigated by optimizing the Fillet Local Oxidation (FILOX). These devices give a sub-threshold slope of 81 mV/dec and a DIBL of 25 mV/V at a channel length of 100 nm. The improved immunity to dry etch damage is due to the creation of a thick protective oxide at the top and bottom of the pillar during the FILOX process.
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1. Introduction

Thin pillar, fully-depleted, surround gate v-MOSFETs are being researched as candidates for end-of-roadmap CMOS technology because they have many advantages such as better short channel effects and improved drive current [1–5] per unit area. These devices also offer a steeper sub-threshold slope because the surround gate provides better control of the channel. Thick pillar, surround gate, v-MOSFETs have also been researched because they offer lithography-independent channel length scaling, decoupling of the gate length from the packing density and an improved current drive per unit silicon area compared with conventional lateral CMOS [6–21].

The main disadvantages of v-MOSFETs are high overlap capacitance and susceptibility to dry etch damage. The problem of overlap capacitance has been addressed using Fillet Local Oxidation (FILOX) [19,20]. This process uses a nitride spacer on the pillar sidewall and local oxidation to reduce the overlap capacitance at the top and bottom of the pillar. The problem of dry etch damage is illustrated in Table 1, which shows values of sub-threshold slope and Drain Induced Barrier Lowering (DIBL) for a variety of thick pillar v-MOSFETs reported in the literature. Results for thin pillar, fully depleted v-MOSFETs have been omitted from the table because we wish to show values of sub-threshold slope without any distortion introduced by the action of the surround gate. It can be seen that the values of sub-threshold slope are typically between 90 and 150 mV/dec, which are a long way from the ideal values that are desirable in these short-channel MOSFETs. With the exception of the device reported in [15], these devices should all exhibit sub-threshold slopes of 70–80 mV/dec, given the values of gate oxide thickness and body doping. These results suggest that there is a fundamental issue of sub-threshold slope degradation in short-channel v-MOSFETs.

In this paper, we investigate how the process used to fabricate the polysilicon surround gate influences the sub-threshold slope of v-MOSFETs. The effect of the polysilicon gate etch is investigated in FILOX v-MOSFETs by fabricating transistors with different channel lengths and different degrees of gate over-etch. It is shown that the polysilicon gate etch can be optimized to give an excellent sub-threshold slope, thereby demonstrating that the degradation of sub-threshold slope is due to dry etch damage. This conclusion is verified using a frame-gate architecture in which the polysilicon gate overlaps the side of the pillar and hence protects the pillar from dry etch damage. When properly optimized, 100 nm FILOX v-MOSFETs exhibit a sub-threshold slope of 81 mV/dec, which agrees very well with the ideal value of 78 mV/dec for the given oxide thickness and body doping.

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Table 1
Comparison of frame-gate and surround gate v-MOSFETs fabricated in this work with devices reported in the literature.

Parameter	Schulz [6]	VRG [17]	Mori [15]	Gili [16]	Moers [21]	Jayanarayan [18]	Frame gate (this work)	Transistors with small gate over-etch (this work)
L (nm)	100	100	100	70	50	50	100	100
t_{ox} (nm)	3	2.8	7	3	6.6	4	2.7	2.7
N_A (10^{17}/cc)	20	35	20	30	2	25	15	15
S (mV/dec)	102	90	100	95	150	135	70–83	76–83
DIBL (mV/V)	70	30	73	120	210	170	30–35	25–35

2. Experimental procedure

Boron-doped (0.75–1.25 Ω cm) (1 0 0) wafers were taken as the starting material and a p-type body was formed by boron implantation (1.2×10^{14}/cm^2, 75 keV, 7° tilt) and high temperature drive-in. Transistors with four different channel lengths were then produced by varying the Si pillar dry etch, with pillar heights varying from 300 to 450 nm. A sacrificial oxidation was performed to reduce the surface roughness on the pillar sidewall and a 10 nm stress relief oxide was thermally grown at 900 °C. For the FILOX process, a 90 nm silicon nitride was deposited at 720 °C, anisotropically etched to create a nitride fillet and subsequently a 60 nm FILOX oxide layer was thermally grown at 1100 °C [19,20]. An SEM cross-section of the transistor at this point in the process is shown in Fig. 1. The source and drain were implanted with 6×10^{15}/cm^2, 100 keV arsenic at 0° tilt and the nitride fillet and pad oxide were subsequently removed by wet etch. A 2.7 nm gate oxide was then grown at 700 °C and a 150 nm in situ phosphorous doped (1×10^{20}/cm^3) polysilicon gate was deposited and patterned by dry etch to create a surround gate. The dry etch was performed with an Applied Materials Precision 5000 Mark II system using Cl_2/HBr chemistry and the underlying SiO_2 layer was used as an etch-stop. In control transistors, the over-etch was around 150 nm to minimise overlap capacitance at the top of the pillar. In other transistors, the polysilicon gate over-etch was varied to investigate the effect of this dry etch on short channel effects. Finally, the wafers were annealed at 1100 °C for 10 s for dopant activation.

Two different device layouts were used (Fig. 2) to investigate the effects of the polysilicon gate etch. Fig. 2a shows the conventional layout, where a polysilicon gate spacer surrounds the pillar sidewall and two gate tracks are used to contact the polysilicon spacer at either side of the pillar. Fig. 2b shows the frame-gate architecture, where a thin frame of polysilicon around the pillar perimeter protects the pillar sidewall from dry etch damage.

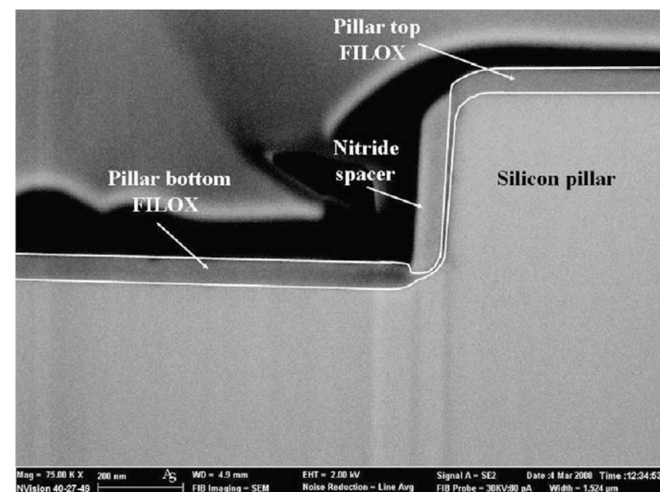

Fig. 1. SEM cross-section of the vertical MOSFET process directly after the FILOX [19] oxidation. The edge of the FILOX oxide layer has been highlighted for clarity.

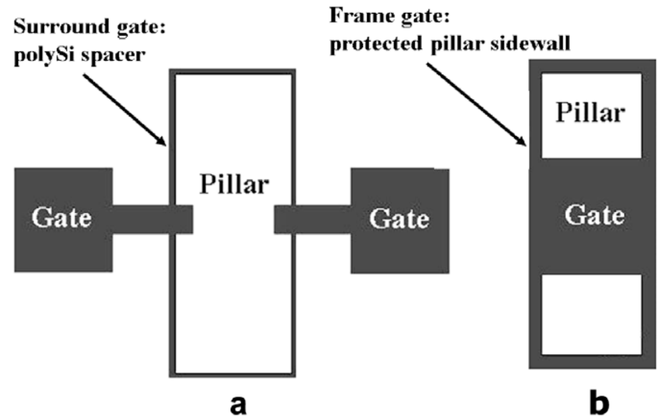

Fig. 2. Schematic vertical MOSFET layouts showing the two types of fabricated device: (a) a surround-gate vertical MOSFET and (b) a frame-gate vertical MOSFET.

The gate oxide thickness was measured from the second derivative of the high frequency capacitance/voltage characteristic [22]. This method gives the capacitance at flat band condition and has been reported to agree within ±0.2 nm with TEM results [22]. A sidewall oxide capacitance C_{ox} of 1.25 μF/cm^2 was measured using special test capacitors and a gate oxide thickness of 2.7 nm obtained. The substrate doping was also extracted from this measurement and a value of 1.5×10^{18}/cm^3 obtained. A similar method was used to measure the FILOX oxide thickness at the end of the process and a value of 40 nm obtained. This value is less than the 60 nm shown in Fig. 2 because some of the FILOX oxide has been removed by the wet etch of the stress relief oxide prior to gate oxide growth.

To extract the channel length (L) we have used profilometer and SEM cross-section measurements of the pillar heights and electrical measurements of gate-channel capacitance (C_{GC}) on transistors with different channel lengths [23]. Measured pillar heights of 300, 350, 400 and 450 nm were obtained on the four different wafers and the corresponding channel lengths were measured as 100, 150, 200 and 250 nm, respectively. We have also extracted channel length by the drain conductance method [24] and performed process simulations of the source/drain anneal to verify the junction depth [25]. These measurements gave channel lengths of 100–105 nm for a pillar height of 300 nm and a junction depth of 190 nm which are in good agreement with the above results.

3. Results

3.1. Short channel effects in FILOX v-MOSFETs

Fig. 3a shows the effect of channel length scaling on the sub-threshold characteristics of control FILOX v-MOSFETs for a drain bias of 50 mV. For a channel length of 250 nm, a steep sub-threshold slope is obtained, but the slope significantly degrades as the channel length is scaled down to 100 nm. The measured values of sub-threshold slope are presented in Fig. 3b, which shows a

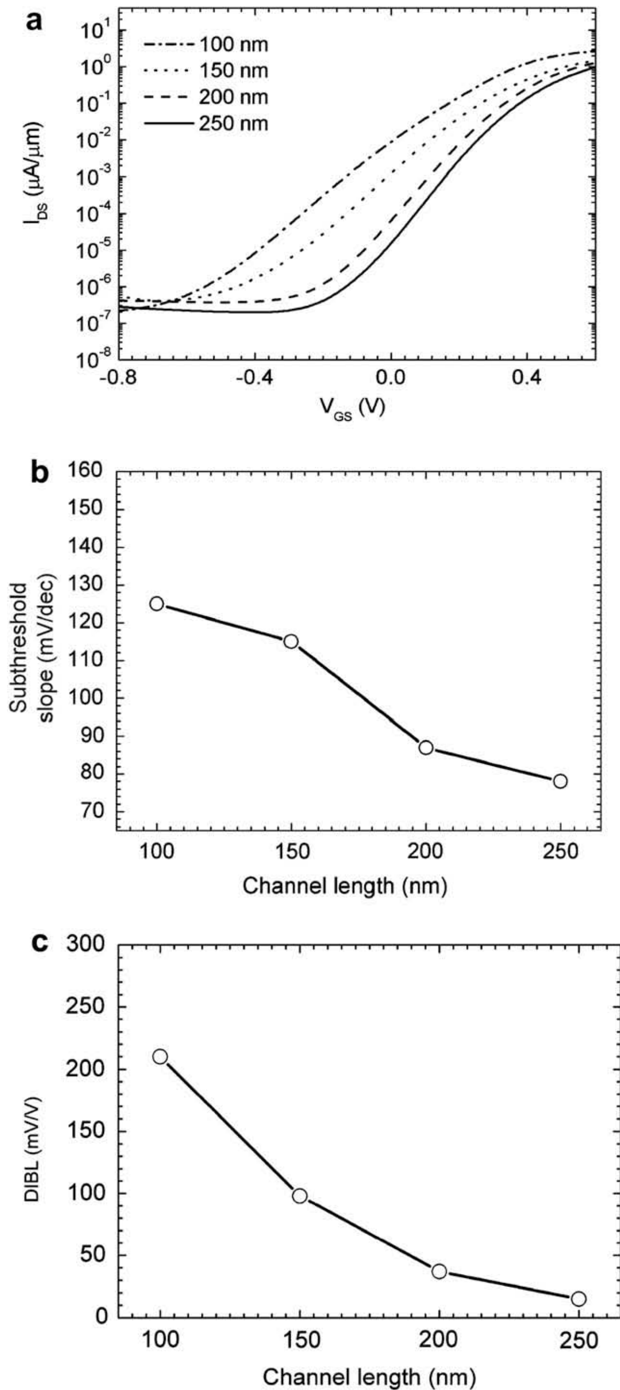

Fig. 3. Electrical characteristics of control FILOX vertical MOSFETs at different channel lengths: (a) sub-threshold characteristics, (b) sub-threshold slope as a function of channel length and (c) DIBL as a function of channel length. The results are presented for a configuration in which the source is on top of the pillar (SOT).

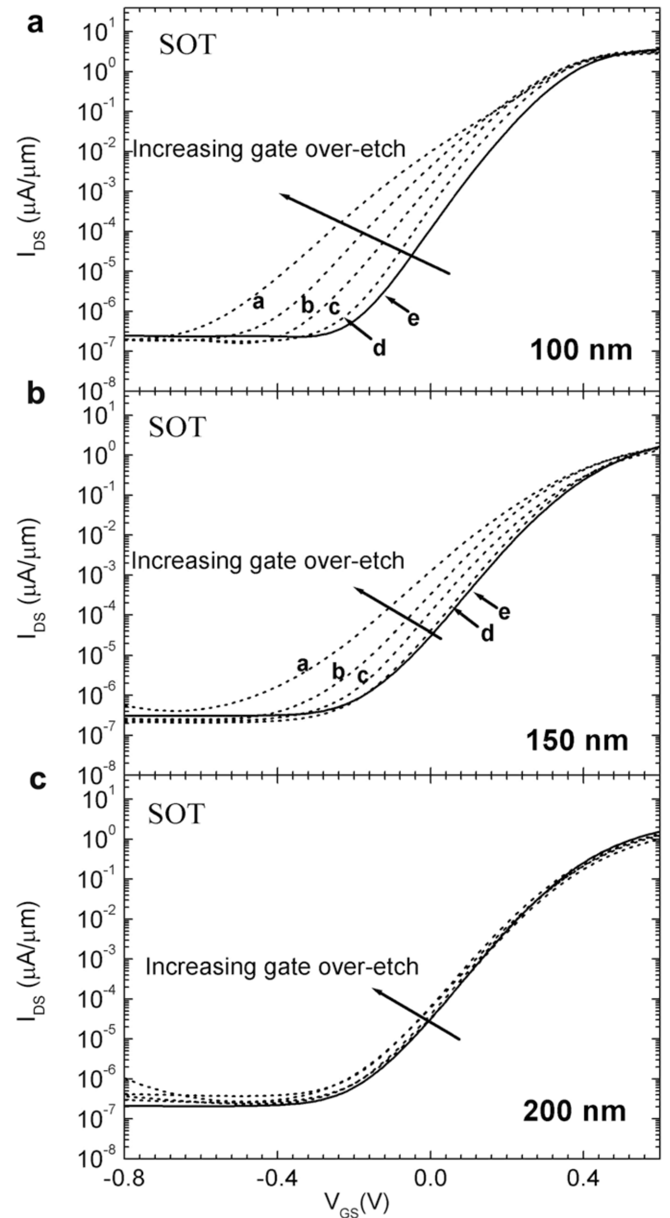

Fig. 4. Effect of increasing gate over-etch on the sub-threshold characteristics of FILOX vertical MOSFETs with channel lengths of: (a) 100 nm, (b) 150 nm and (c) 200 nm. The results are presented for a configuration in which the source is on the top of the pillar (SOT) and for a drain bias of 50 mV.

near-ideal sub-threshold slope of 78 mV/dec for a channel length of 250 nm. However, as the channel length is decreased, the sub-threshold slope progressively degrades to a value of 125 mV/dec at a channel length of 100 nm. Fig. 3c shows the DIBL as a function of channel length for control v-MOSFETs and shows a similar degradation with decreasing channel length. For a channel length of 250 nm, DIBL is 15 mV/V and this degrades to 210 mV/V when the channel length is scaled to 100 nm. These results clearly show the presence of short channel effects in the control FILOX v-MOSFETs.

To investigate the cause of these short channel effects, Fig. 4 shows the effect of polysilicon gate over-etch on the sub-threshold characteristics of FILOX transistors with channel lengths of 100, 150 and 200 nm. The transistors were connected with the source on top (SOT) of the pillar. For the channel length of 100 nm shown in Fig. 4a, a significant degradation of the sub-threshold characteristic is observed with increasing polysilicon gate over-etch. The sub-threshold slope degrades to a value of 125 mV/dec for the biggest over-etch (device a) whereas the transistor with the smallest over-etch has a sub-threshold slope of 82 mV/dec (device e). The threshold voltage was measured using the linear extrapolation method and a 20% reduction in the threshold voltage was obtained as the polysilicon gate over-etch increased. For a 150 nm channel length, Fig. 4b shows a smaller degradation of sub-threshold slope from 82 mV/dec (device e) to 110 mV/dec (device a). A 15% reduction in the threshold voltage was also observed with increasing

polysilicon gate over-etch. For a 200 nm channel length Fig. 4c shows a very small degradation of the sub-threshold slope from 81 to 87 mV/dec and a small threshold voltage reduction of 8%. For a 250 nm channel length (not shown) no degradation of sub-threshold slope was observed and the threshold voltage reduction was less than 3%.

To further investigate any possible asymmetries in the short channel effects, Fig. 5 shows the effect of polysilicon gate over-etch on the transfer characteristics of 100 nm transistors connected with the drain on top (DOT) of the pillar. Again, a significant degradation of sub-threshold slope is observed with increasing gate poly-silicon dry etch. The sub-threshold slope degrades from a value of 81 mV/dec for the smallest over-etch (device e) to a value of 130 mV/dec for the largest over-etch (device a). This degradation in sub-threshold slope is slightly larger than that seen in Fig. 4a for the transistor connected with the source on top of the pillar. The threshold voltage was calculated using the linear extrapolation method and a 20% reduction obtained, which is similar to that seen for SOT operation. It can therefore be concluded that the degradation of sub-threshold slope is seen for both SOT and DOT configurations.

The above results suggest that dry etch damage is responsible for the degradation of short channel effects in control FILOX v-MOSFETs. To investigate this possibility we have made gated diode measurements [26,27] on transistors with a large (device a in Fig. 4) and a small (device e in Fig. 4) gate over-etch, as shown in Fig. 6 for diodes on the pillar top and bottom. A forward bias of 0.4 V was applied between source/drain and body and the gate voltage was swept from −1 V to +1 V. For the pillar top diode subjected to a large over-etch, Fig. 6a shows a significant peak in the diode current (3.2×10^{-11} A/μm), which is indicative of the presence of interface states [26,27]. Under a small forward bias (gated diode forward bias voltage, $V_b < 0.7$ V), the diode operates with a contribution from the current in the sub-threshold region and hence the diode current comprises a small diffusion current component but a large SRH generation/recombination current arising from recombination at $Si–SiO_2$ interface traps. The maximum recombination rate occurs when the surface potential coincides with the intrinsic Fermi level. For the transistor with a small over-etch, no peak is observed and the diode current at the gate voltage of −0.6 V is three times lower, with a value of 1.1×10^{-11} A/μm. For the pillar bottom diodes given a large over-etch, Fig. 6b again shows a peak in the current, with a value of 3×10^{-11} A/μm which is a similar order to that observed for the pillar top diode. In contrast, for the device with a small gate over-etch, a small current peak is seen with a value of 1.4×10^{-11} A/μm, which again ~3 times lower that for the device with a large over-etch. These results lead us to the conclusion that significant interface states are created at the $Si–SiO_2$ interface during the polysilicon gate etch. An approximate value of interface state density was calculated from the gated diode results presented in Fig. 6 and a ΔD_{it} of around $10^{12}/cm^2$ was obtained for the transistor with a large gate over-etch (device "a" in Fig. 4).

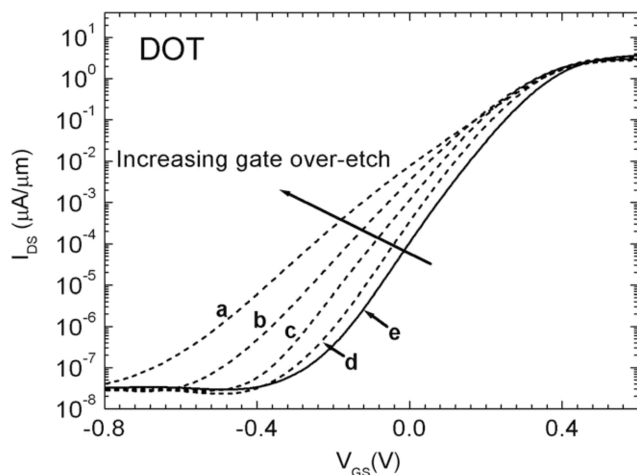

Fig. 5. Sub-threshold characteristics of 100 nm FILOX vertical MOSFETs with increasing amounts of gate over-etch. The results are presented for a configuration in which the drain is on top of the pillar (DOT) and for a drain bias of 50 mV.

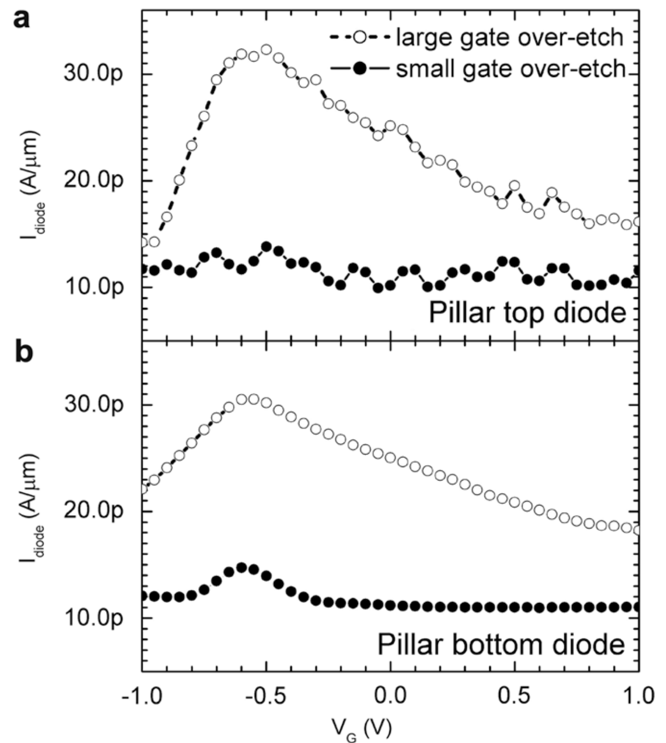

Fig. 6. Diode current as a function of gate voltage for gated source/body and drain/body diodes. Results are shown for different amounts of gate polysilicon over-etch: (a) pillar top diode and (b) pillar bottom diode. A forward bias of 0.4 V was applied between source/drain and body, and the gate voltage was swept from −1 V to +1 V.

3.2. Elimination of short channel effects in FILOX v-MOSFETs

Dry etch damage can be eliminated using the frame-gate architecture shown in Fig. 2, which protects the pillar sidewalls during the dry etch of the polysilicon gate. Fig. 7a shows the effect of channel length scaling on the sub-threshold characteristics of frame-gate v-MOSFETs for a drain bias of 50 mV. It can be seen that steep sub-threshold slopes are obtained for all channel lengths and there is no evidence of a degradation when the channel length is scaled. This result confirms that the degradation of sub-threshold slope seen in control transistors is due to dry etch damage. Fig. 7b presents the values of sub-threshold slope as a function of channel length. For a channel length of 250 nm the sub-threshold slope is 70 mV/dec and there is only a small increase to a value of 76 mV/dec as the channel length is scaled to 100 nm. Considering the gate oxide thickness of 2.7 nm and the body doping density of $1.5 \times 10^{18}/cm^3$, 100 nm transistors would be expected to exhibit an ideal sub-threshold slope of 78 mV/dec; this is in excellent agreement with the measured sub-threshold slope of 76 mV/dec. Fig. 7c shows DIBL as a function of channel length for frame-gate v-MOSFETs, and a small degradation of DIBL from 12 to 33 mV/V is seen on scaling from a channel length of 250–100 nm. These values of DIBL are considerably better than those for the control v-MOSFET shown in Fig. 3c (from 15 to 210 mV/V).

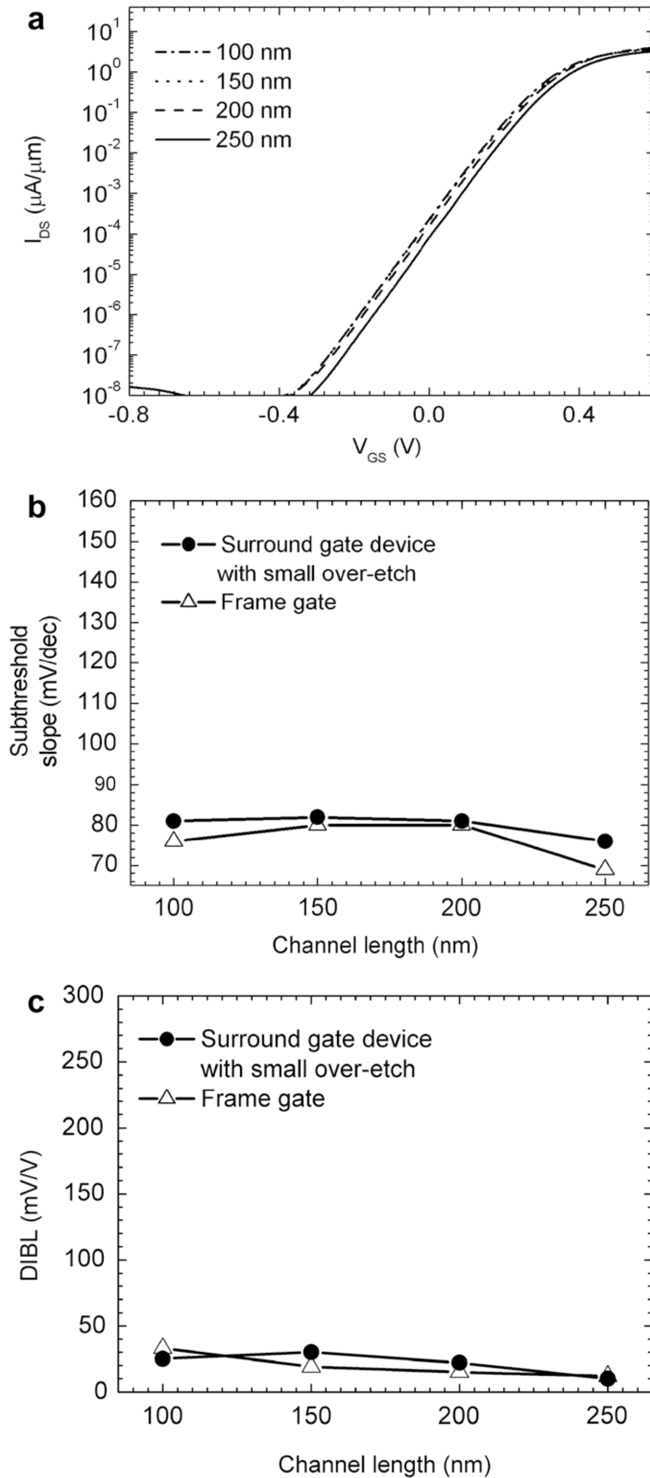

Fig. 7. Electrical characteristics of frame gate FILOX vertical MOSFETs at different channel lengths: (a) sub-threshold characteristics, (b) sub-threshold slope as a function of channel length and (c) DIBL as a function of channel length. For comparison, Figs. 8b and c show results for a surround gate FILOX vertical MOSFET with a small over-etch. All results are presented for a configuration in which the source is on top of the pillar (SOT).

An alternative method of reducing dry etch damage is to reduce the over-etch of the polysilicon gate, as was shown in Fig. 4. Values of sub-threshold slope for optimized devices (device e in Fig. 4) are presented in Fig. 7b for comparison with the frame-gate transistors. At a channel length of 250 nm, a sub-threshold slope of 76 mV/dec is obtained and this degrades to a value of 81 mV/dec at a channel length of 100 nm. These results are very comparable with those for the frame gate transistor and indicate that dry etch damage can be totally eliminated in FILOX v-MOSFETs by optimizing the polysilicon gate dry etch. Fig. 7c shows values of DIBL for optimized FILOX v-MOSFETs. These results are also comparable with those for the frame gate transistor. The DIBL degrades from 10 mV/V to a value of 25 mV/V when the channel length is scaled from 250 to 100 nm.

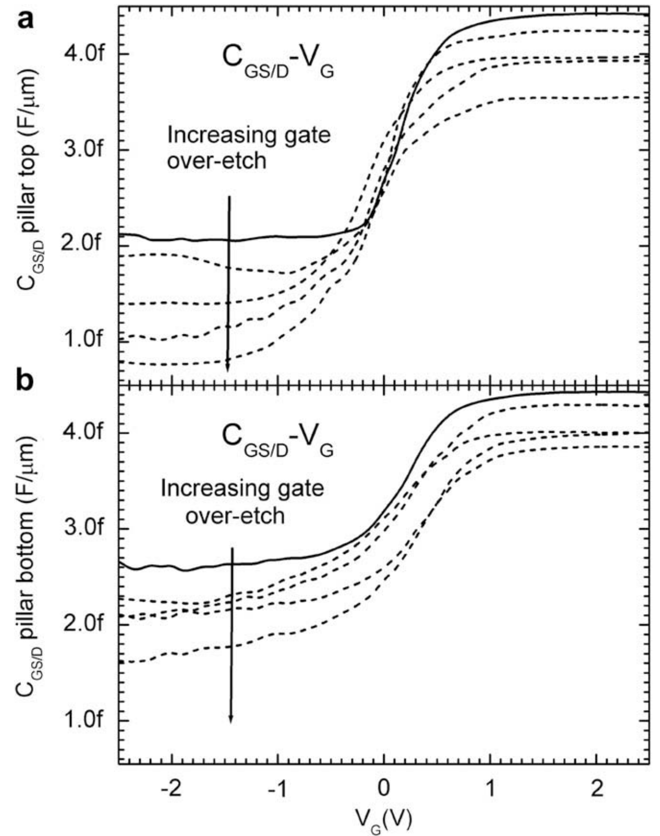

Fig. 8. Gate–source/drain capacitance ($C_{GS/D}$) characteristics at the pillar top and pillar bottom for FILOX vertical MOSFETs with different amounts of polysilicon gate over-etch: (a) $C_{GS/D}$ at the pillar top and (b) $C_{GS/D}$ at the pillar bottom. $C_{GS/D}$ of individual transistors was estimated from measurements on test structures with 500 transistors connected in parallel.

To investigate the effect of polysilicon gate over-etch on the overlap capacitance, Fig. 8 shows the gate–source/drain capacitances ($C_{GS/D}$) at the pillar top and pillar bottom as a function of gate voltage for 100 nm channel length transistors with different amounts of polysilicon gate over-etch. Measurements were made on test structures with an array of 500 transistors connected in parallel and the parasitic interconnect capacitances were decoupled by measurements on dummy metal line structures. However, the measured capacitances in accumulation represent overlap capacitances whereas measured capacitances in inversion represent the sum of overlap and gate-channel capacitances. Fig. 8a shows $C_{GS/D}$ at the pillar top and it can be seen that $C_{GS/D}$ in accumulation significantly reduces with increasing gate over-etch. Transistors with a small over-etch have a gate/drain overlap capacitance of 2 fF/μm, while those with a large over-etch have a lower value of 0.8 fF/μm. Fig. 8b shows that similar results are obtained for $C_{GS/D}$ at the pillar bottom, with a small over-etch giving a value of 2.6 fF/μm and a large over-etch a value of 1.7 fF/μm. For the frame-gate transistors no significant change in the overlap capacitance has been found with increasing gate over-etch. The values of

$C_{GS/D}$ at the pillar top and pillar bottom were found to be around 2.4 and 2.8 fF/μm, respectively.

4. Discussion

The proposed explanation for the dry etch damage is shown in the schematic cross-section in Fig. 9 for a FILOX v-MOSFET with a large gate over-etch. With increasing over-etch, both the height and the width of the polysilicon surround gate are reduced. The SEM cross-section in Fig. 1 indicates that the nitride fillet extends close to the top of the pillar and hence the thick FILOX oxide will not extend far down the side of the pillar, as illustrated schematically in Fig. 9a. Hence a large polysilicon gate over-etch will expose gate oxide at the top of the pillar, so that dry etch damage is created at the top of the pillar where the thin gate oxide is exposed. Similar dry etch damage can occur at the bottom of the pillar, where the thin gate oxide is exposed by the thinning of the polysilicon surround gate. In devices where the polysilicon gate over-etch is smaller (Fig. 9b), the thin gate oxide at the pillar top is well protected by the thick FILOX oxide and at the pillar bottom is protected by the thicker polysilicon surround gate.

Evidence for significant polysilicon thinning has been obtained from measurements of the series resistance of the polysilicon surround gate made on test structures fabricated along with the transistors. Fig. 10 shows current/voltage characteristics of a 280 μm poly silicon surround gate taken between two contacts, for increasing degrees of gate over-etch. It can be seen that the series resistance increases with increasing over-etch, rising from a value of 350 to 940 Ω/μm. This increase by a factor of nearly three demonstrates that significant thinning of the polysilicon surround gate is occurring and hence explains why dry etch damage is seen at the bottom of the pillar as well as the top. To further investigate the effect of dry etch on the sidewall poly silicon spacer, SEM images were taken and it was found that the poly silicon spacer thickness at the pillar bottom reduced from 130 to 70 nm with increasing gate over-etch whereas the poly silicon spacer height varied from 210 to 150 nm. This result is in excellent agreement with the reduced $C_{GS/D}$ (Fig. 8) and with the increased poly silicon fillet resistance (Fig. 10) of the over-etched transistors. It should be noted that the FILOX process could be further optimized by introducing an over-etch of the nitride fillet shown in Fig. 1. This would subsequently cause the thick FILOX oxide to extend further down the side of the pillar as shown in Fig. 9c and would provide protection from dry etch damage at the top of the pillar. Similarly, the introduction of a nitride over-etch would lead to thinning of the nitride fillet and would cause the FILOX oxide to extend closer to the pillar sidewall. This would provide protection from dry etch damage at the bottom of the pillar. A further benefit of this approach would be that a polysilicon gate over-etch could be introduced without a large increase in gate/source and gate/drain overlap capacitance.

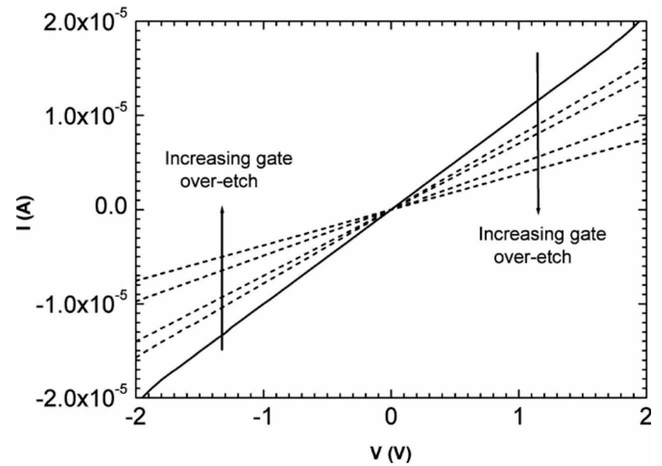

Fig. 10. Gate series resistance obtained from current/voltage characteristics of a 280 μm polysilicon surround gate. Results are shown for different amounts of polysilicon gate over-etch.

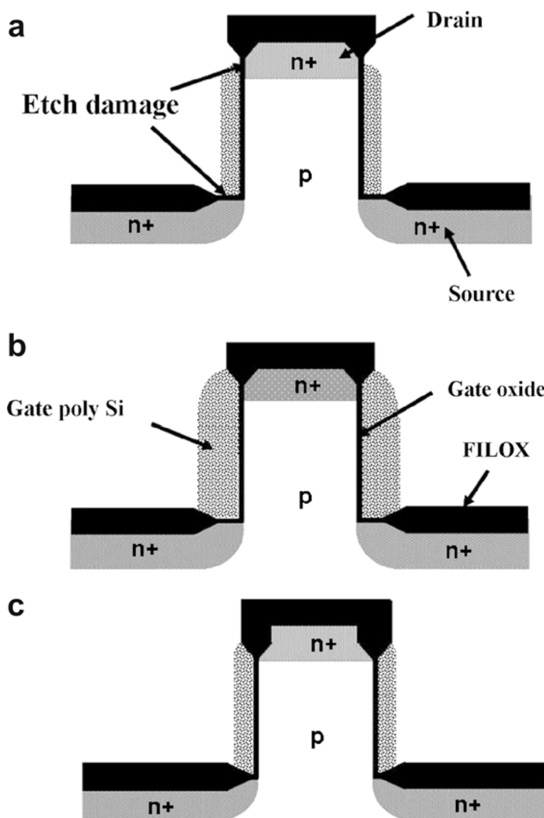

Fig. 9. Schematic cross-sections of surround gate FILOX vertical MOSFETs with different amounts of polysilicon gate over-etch: (a) large gate over-etch, (b) small gate over-etch and (c) large gate over-etch and optimized nitride spacer over-etch.

Table 1 shows a comparison of values of sub-threshold slope and DIBL obtained on our devices with values reported in the literature for other v-MOSFETs. As discussed earlier, results for thin pillar, fully depleted v-MOSFETs have been omitted because we wish to show values of sub-threshold slope without any distortion introduced by the fully-depleted body. The clear advantage of the FILOX process can be readily seen, as the values of sub-threshold slope are significantly lower than previously reported. Furthermore, in all cases except that of Moers et al. [21], the lower values of sub-threshold slope are obtained in spite of the use of a lower body doping. These results suggest that dry etch damage introduced during polysilicon gate etch is a general problem in v-MOSFETs. Furthermore, the results clearly demonstrate that the thick FILOX oxide provides excellent protection from the dry etch damage. The values of sub-threshold slope and DIBL approach almost ideal values, which have previously only been reported for thin pillar, fully depleted v-MOSFETs [1–3].

5. Conclusions

We have investigated the effect of poly-silicon gate over-etch on the degradation of the electrical characteristics of v-MOSFETs and have reported a unique advantage of Fillet Local Oxidation (FILOX) in improving the short channel behavior of v-MOSFETs. This process provides immunity against dry etch damage during

the critical polysilicon gate etch because a thick, protective FILOX oxide is formed at the top and bottom of the pillar, which protects against dry etch damage. In control v-MOSFETs given a large gate over-etch, a degradation of sub-threshold slope from 78 mV/dec to 125 mV/dec is apparent, as the channel length is scaled from 250 to 100 nm. Gated diode results are consistent with the view that this degradation is due to dry etch damage at the top and bottom of the pillar where the gate oxide is exposed by the gate etch. Measurements have also been made on v-MOSFETs with a so-called frame-gate architecture in which the pillar sidewall is protected from dry etch damage. These devices show no degradation of short channel effects when the channel length is scaled and exhibit an excellent sub-threshold slope of 76 mV/dec at a channel length of 100 nm. The sub-threshold slope can also be improved by optimizing the gate over-etch, which gives a sub-threshold slope of 81 mV/dec and a DIBL of 25 mV/V at a channel length of 100 nm.

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