Fabrication of Silicon-based single spin quantum devices using Hydrogen silsesquioxane electron beam resist.

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Hydrogen silsesquioxane (HSQ) has recently become a serious candidate as a high resolution electron beam resist because of its small line edge roughness and high etching resistance [1,2] and is particularly useful for nanoscale patterning of silicon-on-insulator (SOI) for applications in quantum information processing [3]. By using this high resolution resist, we attempt to build a Si based integrated single spin quantum bit system on thin SOI. Our design, shown schematically in Fig. 1, consists of a pair of double quantum dot (QD) transistors. The QDs in each transistor are weakly coupled to each other and to their respective source and drain terminals via tunnel barriers (channel constrictions). The side gates provide electrostatic control of the dots' electron states. One of the two transistors acts as an electrometer to detect changes in the charge configuration in the other, which is operated as a turnstile for electrons [4]. It is crucial to have a narrow separation d_1 for the electrometer current to be sufficiently sensitive to changes in the turnstile QDs' electron occupation. Here we target and achieve a d_1 of ~60 nm which, through combining 3D COMSOL capacitance analysis with Monte-Carlo based single electron circuit simulations, should generate shifts in electrometer current of tens of pA when single electrons are transferred between the turnstile's two QDs. Fig. 2 shows the simulated electrometer's source to drain current, I_{DS} (left axis), and the variation in electron occupation number (right axis), n_{QD1} and n_{QD2}, in QD_1 and QD_2 of the turnstile respectively as a function of an applied side gate voltage V_{G1}. The I_{DS} trace clearly shows distinctive negative shifts in magnitude corresponding to detection of single electron transfers in the QDs of the turnstile.

We also target and achieve constrictions d_2 as narrow as ~25 nm that act as tunnel barriers and dot diameters as small as 50 nm. In order to control the electrochemical potentials of the quantum dots efficiently we achieved extremely narrow gaps d_3 of ~50 nm between the side gates and the quantum dots. Fabrication of this high density nanometer scale structures by electron beam lithography is seriously limited by proximity effects. In consequence, patterns containing nanowires adjacent to the side gates often have uneven sidewalls. This results in unintentionally formed QDs as presented in an earlier work [5]. We carried out extensive dose optimizations in the immediate vicinity of the critical features to reduce these proximity effects. Through this, we obtain high density and extremely well defined double QD structures with side gates by using HSQ e-beam resist.

The double QD transistor layout was written on 60 nm thick HSQ coating a 90 nm thick SOI wafer. A 1 nA beam current at 100 keV acceleration voltage with a 60 µm aperture that generates an estimated spot size of 4 nm was used to write the patterns. A typical line dose for writing the nanowires and constrictions (Fig. 1) was 4 nC/cm. The samples were developed in a 2.45% tetramethylammonium hydroxide developer and rinsed in deionized water. Fig. 3 contains a scanning electron microscope (SEM) image of patterned HSQ on an SOI wafer clearly showing well defined double QD structures dimensionally consistent with the target designs (Fig. 1) within an error margin of ±5 nm. Transfer of this resist pattern into SOI (Fig. 4) was performed by reactive ion etching with an achieved etching rate of 1.21 nm/s for Si with 2:1 selectivity with HSQ. The etched nanowires and constrictions are observed to have clearly defined vertical sidewalls and are of the targeted dimensions. To our knowledge this is the first successful attempt at obtaining such high density lithographically defined quantum devices.

Further work will include a size reducing pattern dependent oxidation [5], top gate and the ohmic contact definition in order to achieve the complete device and a detailed electrical characterization.

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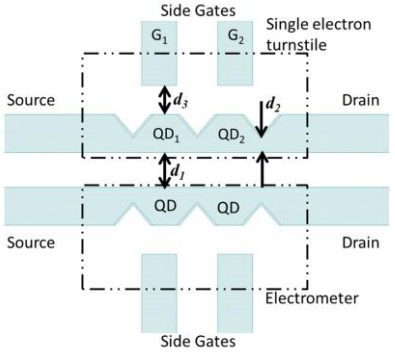

Figure 1. Schematic view of the dual double quantum dot transistor layout.

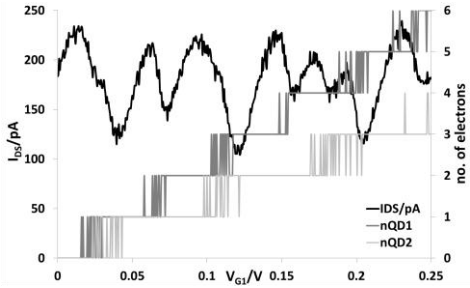

Figure 2. Simulated electrometer response current and turnstile QDs' electron occupation as a function of side gate voltage.

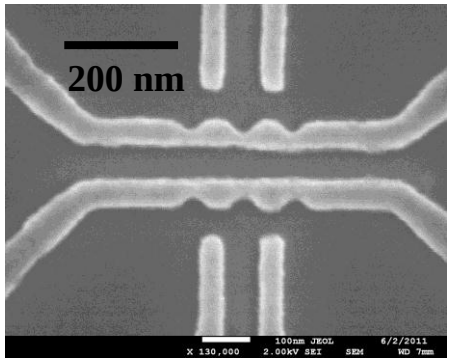

Figure 3. An SEM image of the nanoscale design of Fig.1 patterned into 60 nm thick HSQ resist on an SOI wafer.

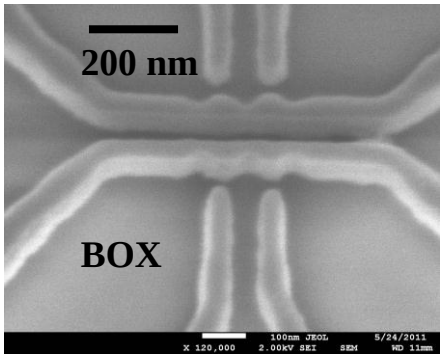

Figure 4. An SEM image of the QD devices etched into SOI. The sample was tilted by 20°.