Analysis of Resistive Bridge Defect Delay Behavior in the Presence of Process Variation

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***Abstract*—Recent research has shown that tests generated without taking process variation into account may lead to loss of test quality. Using transition delay test, this paper analyzes the behavior of resistive bridge defect under the influence of process variation. The effect of process variation is incorporated by using three transistor parameters: gate length (L), threshold voltage (V_{th}) and effective mobility (μ_{eff}), where each follows Gaussian distribution. Through HSPICE simulations using a 65-nm gate library, this paper brings the following two contributions: firstly, it analyzes the delay behavior of bridge defect using all three transition delay classes to determine the most effective class of transition test that achieves maximum coverage in the presence of process variation. Secondly, recent research has shown that low-voltage testing improves detectability of bridge fault; this work compares bridge resistance coverage using logic test and delay test at multiple voltage settings to identify the best voltage setting and test type for detecting resistive bridge defects.**

***Index Terms*—Resistive bridge defects, transition delay test, process variation, logic test, low voltage test.**

I. Introduction

The impact of process variation on integrated circuit performance cannot be ignored due to continuous scaling of CMOS [1], [2]. Fabrication process variation is mainly due to sub-wavelength lithography, random dopant distribution, line edge roughness and stress engineering [3], [4]. There is a general consensus in research community that transistor gate length and threshold voltage are the two leading sources of process variation; recently mobility (μ_{eff}) has also emerged as a source of variation due to variation in effective strain in a strained silicon process and should be included in the analysis together with the other two parameters, i.e., L and V_{th} [4]. In a recent study, it has been shown that more than 30% error in the drive current of a transistor is observed on a 65-nm device due to process variation, when compared to a transistor nominal operating condition [4]. Process variation also has negative effect on the quality of manufacturing test, leading to test escapes as in the case of bridge defects [5].

Resistive bridge defect represents a major class of defects in deep-submicron CMOS and have received increased attention on modeling, simulation and test generation [6], [7]. The behavior of resistive bridge defect under the influence of process variation has been analyzed when considering logic test [5], [8]. In [5] using ISCAS 85, 89 benchmarks and a 45-nm gate library, it was shown that tests generated for nominal scenario without considering process variation can lead to as much as 10% loss of fault coverage (referred as weighted average test robustness in [5]) due to additional faults. This is because process variation affects the drive strength and logic threshold of a gate leading to generation of new faults, which are undetectable through a test generated without considering process variation [5]. In [8] using BSIM4 transistor model, a fast and accurate modeling technique is proposed to incorporate the effect of process variation on resistive bridge defects. It also proposes an approximation algorithm to calculate the critical resistance of a bridge defect using BSIM4 transistor model. This technique is 7 times faster with 0.8% worst case error in calculating bridge critical resistance in comparison to HSPICE [8]. Critical resistance of a bridge fault is the crossing point between faulty and fault-free behavior [8] and the circuit behaves as a fault-free design when bridge resistance value is higher than its critical resistance value. In this paper, when considering logic test, we use the same model (as in [8]) to calculate the critical resistance of a bridge fault-site.

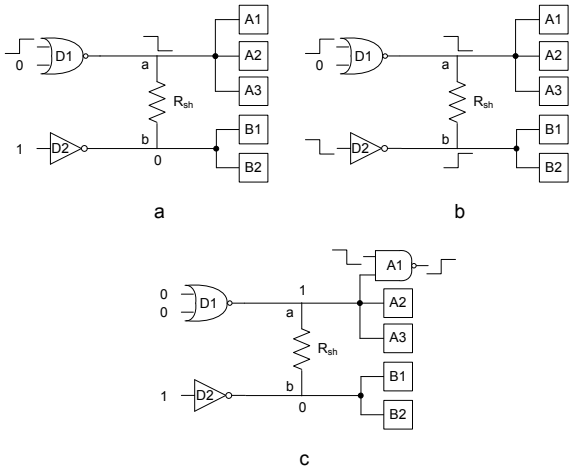

Fig. 1. Transition delay test classification: (a) Class-I; (b) Class-II; (c) Class-III.

When considering transition delay test, it is classified into three classes for resistive bridge defects [9]. These three classes are shown in Fig. 1 and discussed in detail in Sec. II-A.

Through simulations in nominal operating conditions on a number of resistive bridge fault-sites, it was shown in [9] that delay test coverage is higher than logic test, this study also compares the resistance coverage of each of the three delay test classes. To the best of our knowledge, there is no study that analyzes the impact of process variation on delay behavior of resistive bridge defects, which is the aim of this paper. This paper brings the following two contributions: firstly, we investigate the delay defect behavior of resistive bridge using all three transition delay test classes to determine the most effective class of transition test that achieves maximum coverage in the presence of process variation, we also provide results for nominal operating conditions. Secondly, it is well-known that low-voltage testing increases the detectable resistance range of bridge fault [7], therefore we compare bridge resistance coverage using logic test at low-voltage setting with delay test at nominal voltage.

This paper is organized as follows: Section II presents the methodology for analyzing resistive bridge behavior in the presence of process variation. Section III reports the simulation setup and results, and finally Section IV concludes the paper.

II. Methodology

This section introduces the methodology to analyze the impact of process variation on resistive bridge using transition delay test. Section II-A classifies the resistive bridge transition test into three classes. Section II-B introduces an interpolation method to calculate the bridge critical resistance of the transition delay fault, using the known fault-free transition delay values through a simple linear interpolation method. Finally, the effect of process variation on the bridge critical resistance is modeled by three parameters (L, V_{th} and μ_{eff}) with the fluctuations of $\mu \pm 3\sigma$ [4], which is described in Section II-C.

A. Resistive Bridge Transition Delay Test Classification

In [9] the bridge transition delay test is classified into three classes, which are shown in Fig. 1. In Fig. 1, R_{sh} represents the resistive bridge, D_1 and D_2 are the gates driving the bridge nets while A_1 to A_3 and B_1, B_2 are the driven gates. Class-I is shown in Fig. 1-(a), as can be seen there is only 1 transition at faulty node (node a) while the other node (node b) is held at a constant value, and the transition fault is detected through the transition delay at the output of driven gate A_1, and/or A_2, and/or A_3. Class-II is shown in Fig. 1-(b), which is due to two transitions at faulty nodes (both node a and b) and the transition fault is detected as in case of Class-I test. Class-III fault is shown in Fig. 1-(c), which is due to transition at the input of the driven gate (gate A_1) connected to the faulty node (node a) and the transition fault is detected at the output of the same gate (gate A_1). In this work we analyze the effect of these 3 types of delay faults to determine the most suitable type for detecting resistive bridge faults in nominal operating conditions and under the influence of process variation.

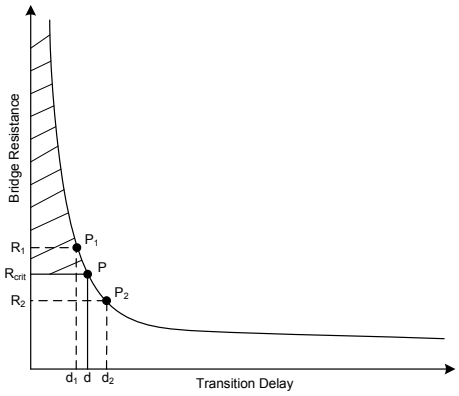

Fig. 2. Bridge critical resistance calculation when considering delay test.

B. Bridge Critical Resistance Calculation

Removing the bridge defect R_{sh} shown in Fig. 1, the circuit behaves as a fault-free case. Transition delay from a fault-free case is called fault-free transition delay, and the maximum amount of detectable bridge resistance through any class of delay test is called bridge critical resistance. After that value the faulty case is undetectable and it is called benign region [9] (shaded area in Fig. 2). In order to calculate the critical resistance of a bridge, the fault-free transition delay is inserted into the delay vs. resistance curve which is obtained from SPICE simulation of the fault-site by sweeping the value of R_{sh} from 0Ω to (typically) 20,000Ω [7] with a step size of 500Ω to find out the smallest delay interval. Experimental results indicate that in general transition delay reduces exponentially with the increase of bridge resistance. This is shown in Fig. 2. Point P represents the fault-free case and it includes the fault-free transition delay (d) and the critical bridge resistance (R_{crit}). Points P_1 and P_2 represent the data points of delay vs. resistance curve obtained from the faulty case and points P_1 and P_2 are the smallest delay intervals that includes the fault-free transition delay d. By applying a simple linear interpolation method, Eq. (1) can be derived. The value of bridge critical resistance R_{crit} can be calculated from Eq. (2). This method is used to determine bridge critical resistance through transition delay test in all the experiments discussed in this paper.

$$\frac{d - d_2}{R_{crit} - R_2} = \frac{d_1 - d_2}{R_1 - R_2} \tag{1}$$

$$R_{crit} = (d - d_2)\,\frac{R_1 - R_2}{d_1 - d_2} + R_2 \tag{2}$$

C. Incorporation of Process Variation

A recent study describes the parameter extraction technique (for process variation) using a 65-nm CMOS library with a PTM model [4], [10]. Three transistor parameters are recognized as the leading sources of process variation, which include: gate length (L), threshold voltage (V_{th}), and mobility[1]

[1]Mobility varies due to variation in effective strain in a strained silicon process [4].

TABLE I
VARIED PROCESS PARAMETERS

Parameter	Mean (μ)	Std. Deviation (σ)
L	60-nm	$\pm$4% (2.4-nm)
V_{thn}	0.423-V	$\pm$5% (21.15-mV)
V_{thp}	-0.365-V	$\pm$5% (18.25-mV)
μ_{effn}	491 cm^2/V.s	$\pm$21% (103.1 cm^2/V.s)
μ_{effp}	57.4 cm^2/V.s	$\pm$21% (12.05 cm^2/V.s)

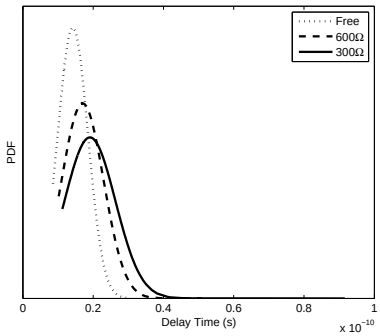

Fig. 3. The effect of bridge resistance on delay behavior under the influence of process variation.

(μ_{eff}). These parameters follow Gaussian distribution ($\pm 3\sigma$ variation) with standard deviations of 4% for L, 5% for V_{th} and 21% for μ_{eff}. Negligible spatial correlation is found in between these parameters, i.e., they can be treated as independent random variables following Gaussian distribution. These results are validated by comparing with the measured data using a fabricated device. Note the parameter fluctuations (correlated or otherwise) do not imply that these parameters are independent, for example as L decreases, V_{th} also decreases, this effect is also known as V_{th} roll-off [11]. Our experiments are based on a ST Microelectronics 65-nm gate library using the same PTM model cards that are used in [4], which is why we have also assumed the same parameter fluctuations. The mean and standard deviation for both NMOS/PMOS transistors are shown in Table I. More details on how process variation is incorporated can be found in [8]. Recent research has shown that it is sufficient to consider $\pm 3\sigma$ variation of process parameters, when modeling process variation for logical part of the design [5], [12], and higher variation effects ($\pm 6\sigma$ or more) are considered for (SRAM and Flash) memories [3]. This work also deals with the logical part of the design, which is why we have also considered $\pm 3\sigma$ variation effects.

Fig. 3 uses the probability density function (PDF) of normal distribution to show the delay behavior of a fault-site shown in Fig. 1-(a) under the influence of process variation by varying three parameters (L, V_{th} and μ_{eff}) using Gaussian distribution with $\pm 3\sigma$ variation. For this example, we inserted two resistive bridge defects (R_{sh} is 300Ω and 600Ω) and compared the behavior with fault-free case. In Fig. 3 the line $free$ represents the transition delay distribution of the fault-free case and the lines marked with 600Ω and 300Ω represent the transition

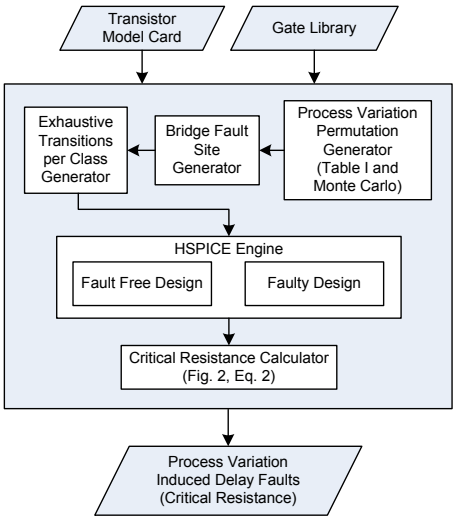

Fig. 4. Simulation flow of process variation-aware transition delay test of resistive bridge defect.

delay obtained from faulty cases under the influence of process variation. As can be seen, as resistance increases, the difference of transition delay in faulty and fault-free cases reduce and further higher values of bridge resistance ($R_{sh} > 600\Omega$) behave like a fault-free case as shown in Fig. 2. This trend is found for all three classes (Fig. 1) of transition delay faults.

III. SIMULATION RESULTS

Experiments are conducted using a 65-nm ST Microelectronics gate library and PTM transistor model card [10] on Intel Xeon Quad Core 2.7 GHz processor with 12 GB RAM. The gate library consists of a variety of gates including simple (NAND, NOR, INV) and compound gates (AO22, OA22 etc.), each with different drive strengths. For illustration purposes 1.2-V is used as the nominal operating voltage in all experiments. The simulation flow for analyzing resistive bridge defect under the influence of process variation using transition delay test is shown in Fig. 4. It can be seen that the flow inputs are gate library and respective transistor models and the output is delay fault values (critical resistance) of the bridge fault-site in the presence of process variation. The flow has five main blocks. The Process Variation Permutation Generator incorporate the effect of process variation into the bridge fault-site. It varies three parameters (L, V_{th} and μ_{eff}) using Gaussian distribution with mean and standard deviation as shown in Table I. In total 600 permutations per fault-site are generated through Monte-Carlo simulation. The number of permutations are based on a recent study, which shows that the probability of generating a unique logic fault follows the law of diminishing returns, as it reduces significantly after 500 permutations [13]. The bridge fault-sites are generated using Bridge Fault-Site Generator for each of the three classes (Class-I, Class-II and Class-III) to build an active bridge fault-site (two nets are driven at opposite values) with specific input vectors to ensure that each gate within the fault-site can

propagate the transition fault for each class of transition delay test. Every bridge fault-site is generated by randomly selecting (driving and driven) gates from the gate library, using n driven gates per driven, where $n \in [1, 5]$. The bridge fault-site generator generates 350 fault-sites for each experiment because it was shown in [5] that the average number of fault-sites per design is less than 300 with coupling capacitance based layout extraction of bridges using ISCAS 85, 89 benchmarks. Each transition delay test class of the bridge fault-site is tested using exhaustive transition test, by using the Exhaustive Transitions Generator, which means that every possible input vector is applied to the fault-site for three different classes. For example, in case of Class-I delay test shown in Fig. 1, the transition signal is applied to every input of D_1 and D_2. The bridge fault-site is generated into two designs: faulty case with bridge resistance (as R_{sh} shown in Fig. 1) and fault-free case without bridge resistance. The faulty case generates transition delay of the driven gates by sweeping bridge resistance from 0Ω to 20,000Ω [7] with a step size of 500Ω using SPICE, which is stored in a database to hold delay vs. resistance values and is compared with delay value from fault-free case. This is used to calculate critical resistance of the bridge fault-site using a simple linear interpolation method (Fig. 2 and Eq. (2)). The transition delay in all the experiment is measured as the time interval between the transition signal crossing 20% of V_{dd} and 80% of V_{dd} for both rising delay and falling delay by using SPICE simulation. This time interval is based on values used in 65-nm ST gate library manual. The simulation flow shows in Fig. 4 can be used for evaluating resistive bridge defect under the influence of process variation using transition delay test with different technology nodes. The flow will require a gate library with respective transistor model card and appropriate values of mean and standard deviation for the three transistor parameters (Table I).

This setup is used to conduct three experiments. The first experiment (Section III-A) calculates the critical resistance (maximum detectable resistance) using three classes of transition delay test to determine the most effective class of delay test for testing resistive bridge. It also compares the results with logic test. This experiment is conducted in nominal operating conditions. The second experiment (Section III-B) compares the results using the same set of fault-sites as in Section III-A under the influence of process variation. The last experiment (Section III-C) compares the results of average critical resistance between logic test at lower V_{dd} setting and delay test at nominal V_{dd} setting under the influence of process variation.

A. Bridge Transition Delay Faults in Nominal Operating conditions

For the nominal operating conditions, the experiments are conducted using the flow shown in Fig. 4 without using process variation permutation generator for 350 fault-sites per class. The results are shown in Table II, which shows the critical resistance for the fault-site shown in Fig. 1 using all three classes of delay test. The input vectors are chosen to ensure exhaustive transition tests for each class. The critical bridge resistances of the bridge transition fault is calculated using the method shown in Fig. 2 and Eq. (2) in nominal operating conditions, and the critical resistance from logic test is calculated by using the model proposed in [8]. The column $Input$ in Table II shows different input vectors for D_1 and D_2 as shown in Fig. 1. ↑ and ↓ represent the rising signal and falling signal. Results in Table II show that in nominal operating conditions, the critical resistance obtained from delay test (maximum of 2916.4Ω) is significantly higher than the one from logic test (399.8Ω). Table II also shows that using delay test with different input transition signals applied to different inputs (D_1 and D_2) the critical resistance changes significantly, for example, in case of Class-I delay test the value of R_{crit} varies from 901.1Ω to 2916.4Ω. Note that every class has different maximum resistance coverage with different input vectors (critical resistance per class). The maximum resistance of Class-I is 2916.4Ω compared to Class-II of 2277.7Ω and Class-III of 2050.9Ω. In general, when considering 350 fault-sites with exhaustive test vectors, results are shown in Table III. It shows that Class-I has the largest coverage, and up to 48.5% cases show maximum detectable resistance using Class-I, and on average Class-I has the largest coverage in 46.9% cases while Class-II has the lowest coverage (19.9%) for testing resistive bridge defects.

TABLE II
CRITICAL RESISTANCE IN LOGIC TEST AND DELAY TEST IN NOMINAL OPERATING CONDITIONS.

Class	Input			R_{crit} (Ω)	
	D_1		D_2	Logic Test	Delay Test
I	↑	0	1	399.8	901.1
	↓	0	1		2087.9
	0	↑	1		1419.7
	0	↓	1		2916.4
	0	0	↑		1248.3
	0	0	↓		1598.6
II	↑	0	↓	399.8	897.8
	↓	0	↑		2122.1
	0	↑	↓		1377.8
	0	↓	↑		2277.7
III	0	0	1	399.8	967.6
	0	0	1		2050.9

TABLE III
PERCENTAGE OF CRITICAL RESISTANCE IN NOMINAL OPERATING CONDITIONS USING THREE CLASSES OF DELAY TEST.

	Class-I	Class-II	Class-III
Falling delay	45.3%	20.5%	34.2%
Rising delay	48.5%	19.4%	32.1%
Average	46.9%	19.9%	33.2%

TABLE IV
CRITICAL RESISTANCE IN LOGIC TEST AND DELAY TEST UNDER THE INFLUENCE OF PROCESS VARIATION.

Class	Input			Logic Test		Delay Test	
	D_1		D_2	Min (Ω)	Max (Ω)	Min (Ω)	Max (Ω)
I	↑	0	1	39.1	2968.7	0	9905
	↓	0	1			0	8645
	0	↑	1			0	7438
	0	↓	1			0	8313
	0	0	↑			0	7215
	0	0	↓			0	6957
II	↑	0	↓	39.1	2968.7	0	9410
	↓	0	↑			0	7825
	0	↑	↓			0	7700
	0	↓	↑			0	8438
III	0	0	1	39.1	2968.7	0	9354
	0	0	1			0	9625

TABLE V
PERCENTAGE OF MAXIMUM RESISTANCE RANGE OF EACH OF THE THREE CLASSES OF DELAY TEST UNDER PROCESS VARIATION.

	Class-I	Class-II	Class-III
Falling delay	38.4%	28.4%	33.2%
Rising delay	33.7%	34.2%	32.2%
Average	36.0%	31.3%	32.7%

B. Bridge Transition Delay Faults under the influence of Process Variation

Process variation permutation generator shown in Fig. 4 is used to model the impact of process variation by considering variation of three un-correlated parameters (L, V_{th} and μ_{eff}). The process variation permutation generator generates 600 permutations of three parameters for each fault-site following Gaussian distribution within the range of $\pm 3\sigma$ using Monte-Carlo simulation in SPICE. For the fault-site shown in Fig. 1, the results are shown in Table IV. The "Min" and "Max" values in Table IV represent the minimum and maximum values of critical resistance, as a result of process variation across $\pm 3\sigma$ range. It can be seen that in logic test the critical resistance varies from 39.1Ω to 2968.7Ω, but in delay test the critical resistance varies from 0Ω to 9905Ω, which is significantly higher. In this case, Class-I covers highest resistance range in comparison to the other two classes. Fig. 5 shows the change in critical resistance for three different resistive bridge transition tests shown in Fig. 1 and using logic test, under the influence of process variation. Next, using 350 fault-sites we show the maximum resistance coverage by each class using exhaustive test under the influence of process variation. Results in Table V show that on average Class-I has the largest coverage (36.0%) and it is up to 38.4% using transition delay test and Class-II has the lowest chance (31.3%) for testing resistive bridge under the influence of process variation as well as in nominal operating conditions (Table III). These results clearly indicate that Class-I has the highest coverage range among three classes of delay test, and the coverage of each class is always better than logic test.

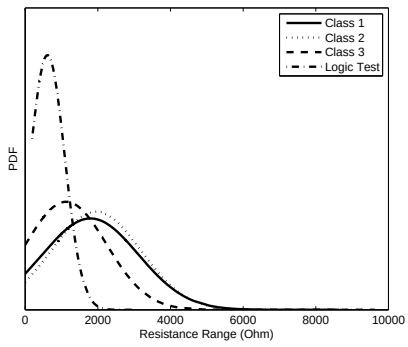

Fig. 5. Critical resistance range for logic test and different classes of delay test under the influence of process variation.

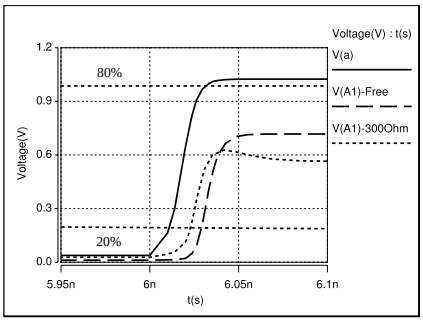

Fig. 6. Transition signal reduction due to process variation and resistive bridge defect.

Next, we show how process variation affects the delay behavior of a fault-site shown in Fig. 1-(a), where the design is operating at 1.2-V V_{dd} and single transition is applied at the input of gate D1 and it is observed at the output of gate D1 (node a) and gate A1 (node A1). The behavior is shown in Fig. 6. It can be seen that the voltage V(a) is reduced (slightly above 80% V_{dd}) because of decreased drive strength of gate D1 due to process variation. Furthermore, the logic threshold voltage and drive strength of the driven gate (A1) is also affected by process variation leading to a faulty behavior (V(A1) $<$ 80% V_{dd}) as observed at the output of gate A1. Fig. 6 also shows the delay behavior of the same fault-site with a resistive bridge ($R_{sh} = 300\Omega$), it can be seen that the delay increases further and it behaves like a stuck-at fault, which can be detected through both logic and delay test.

C. Comparison between Delay Test at Nominal Operating Conditions and Logic Test at Lower Voltage Setting

Results in Section III-A and Section III-B show the resistance coverage using delay test is significantly larger than logic test both in nominal operating conditions and under the influence of process variation while using the same supply voltage (V_{dd} = 1.2-V). Previous research shows that lowering supply voltage setting can achieve higher resistance coverage

TABLE VI
AVERAGE CRITICAL RESISTANCE OF LOGIC TEST AT 0.8-V V_{dd} SETTING AND DELAY TEST OF CLASS-I AT 1.2-V V_{dd} SETTING IN NOMINAL OPERATING CONDITIONS AND UNDER PROCESS VARIATION.

		Nom	$\pm 3\sigma$ Variation	
Method	Voltage	(Ω)	Min (Ω)	Max (Ω)
Logic Test	0.8-V	1118.8	247.2	5447
Delay Test	1.2-V	2353.3	120.3	10269

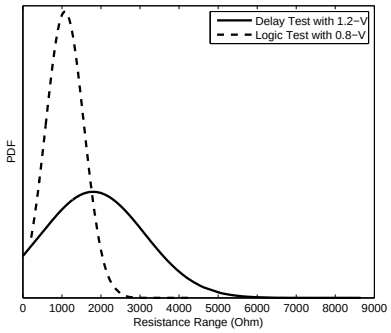

Fig. 7. Critical resistance range for logic test at V_{dd} = 0.8-V and Class-I transition delay test at V_{dd} = 1.2-V under the influence of process variation.

both in case of logic and delay test [7], [14]. Next, we compare the results of logic test at lower supply voltage setting (V_{dd} = 0.8-V) while delay test at V_{dd} = 1.2-V using 350 fault-sites both in nominal operating conditions and under the influence of process variation to compare the resistance coverage. For the fault-site shown in Fig. 1, results are shown in Fig. 7 by using the Class-I transition fault and low V_{dd} logic test under the influence of process variation. Fig. 7 clearly shows that delay test at nominal operating voltage covers higher resistance range when compared with logic test at lower supply voltage. Results of average critical resistance from 350 fault-sites are shown in Table VI. The value of "Nom" represents the critical resistance in nominal operating conditions. The values of "Min" and "Max" represent the minimum and maximum critical resistances under the influence of process variation. On average from 350 fault-sites, Class-I transition delay fault has critical resistance value of 2353.3Ω in nominal operating conditions and varies from 120.3Ω to 10,269Ω under the influence of process variation which is significantly higher than the values at lower V_{dd} logic test.

IV. CONCLUSION

This paper has presented a detailed analysis of delay behavior of resistive bridge defect under the influence of process variation. The effect of process variation is modeled by using three transistor parameters: L, V_{th} and μ_{eff}, using Gaussian distribution. We analyzed the effect of three delay test classes. The experiments are conducted on a 65-nm gate library show that the resistance coverage achieved by using any class of delay test is significantly higher than logic test and this trend continues even with low-voltage logic test and nominal voltage delay test. When comparing three different classes of delay test under the influence of process variation, it is found that maximum coverage is achieved using Class-I delay test (Fig. 1-(a)) and on average it covers maximum resistance in 36% cases, followed by Class-III (Fig. 1-(c)), which achieves maximum coverage in 32.7% cases and Class-II (Fig. 1-(b)) achieves maximum coverage in 31.3% cases. This trend continues in nominal operating conditions as well. This work is carried out using Monte-Carlo simulation through SPICE and on average each simulation takes about 19 minutes per fault-site due to including the effect of process variation. This motivates our continuing work on developing a fast and accurate fault-simulator for testing resistive bridge defects in the presence of process variation by developing an analytical model which incroporates BSIM4 transitior model to calculate transition delay efficiently.

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