

Design and Analysis of Double Spin Qubits Integrated on Ultra-thin Silicon-on-insulator

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Abstract— This paper presents the design and analysis of a Si-based integrated spin qubit system on ultrathin silicon-on-insulator. A new design layout is proposed for the double spin qubits co-integrated with a single electron electrometer, a μ -ESR and a nanomagnet. Three dimensional FEM simulations are performed to calculate the capacitance parameters among quantum dots and other building blocks for the proposed structure. Monte Carlo based single electron circuit simulation is then performed to demonstrate single electron transfer operation. The single electron transfer characteristics are analyzed and used to optimize the system structural parameters and layout.

I. INTRODUCTION

The first Si-based qubit was proposed by Kane [1] using nuclear spins of phosphorous donor atoms in silicon benefitting from the very long decoherence time of nuclear spins in Si. However, the proposal requires extreme bottom-up nanotechnologies, e.g. STM lithography, to control the number and position of the P donor atoms within the silicon wafer. An exquisite degree of control over single electron spins has been demonstrated for quantum dots (QDs) defined on the two-dimensional electron gas formed at the GaAs/AlGaAs heterojunction by using top-down lithography technology [2]. Unfortunately the coherence of electron spins deteriorates rapidly in GaAs due to its rich nuclear spin density; electron spins can be confined in silicon based QDs, benefiting from the low nuclear spin density of silicon based materials. Recently, QDs capable of confining few electrons have become feasible in silicon [3], providing a motivation for this research. In this paper, we propose a new Si-based double spin qubit system on ultrathin silicon-on-insulator (SOI) and present the design layout of the integrated system as well as preliminary simulation of single-electron turnstile operation adopted for initialization of single spins.

II. INTEGRATED SINGLE-SPIN QUBIT SYSTEM

The proposed system of integrated single-spin qubits is schematically shown in Fig. 1. The system is to be formed on

an ultrathin undoped SOI substrate and features double single-spin transfer devices (SSTDs) built as parallel SOI nanowires (NWs) where their edges are interconnected by another short NW. There is an upper metal gate used to induce a weak inversion channel in the NWs. The individual SSTDs are equipped with a pair of lower poly-Si control gates (LTG1a,b and LTG2a,b), and one other poly-Si gate (JG) is placed in the middle of the interconnect. This SSTD pair is integrated with three other key components: (1) an in-plane single-electron electrometer formed adjacent to the edge of the upper SSTD, (2) a micro electron spin resonance (μ -ESR) device formed by using a metallic waveguide and placed near the interconnect NW, and (3) a nanomagnet which generates a magnetic field gradient along with the interconnect NW.

This platform aims to demonstrate the full operation of double spin qubits by integrating the following three key techniques in one compact footprint:

The first technique is a precisely controlled single electron transfer technology developed in [4], where a single-electron turnstile device on an SOI substrate has been successfully demonstrated to realize room-temperature single-electron memory and logic circuits. This technique is adopted to confine a single electron in the QDs formed adjacent to the corners of the individual SSTDs.

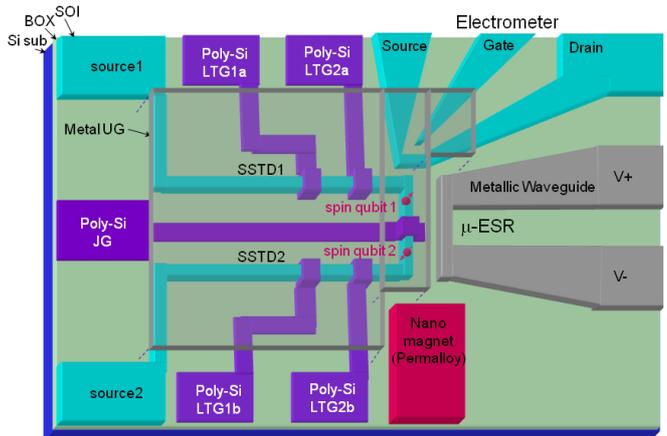


Figure 1. Schematic diagram of the double spin Qubit system.

The second technique is high-speed charge detection using a radio frequency single electron transistor (RF-SET) developed in [5], where operation of Si RF-SETs with MHz bandwidth and near quantum limited charge sensing performance have been demonstrated. A single-shot measurement of the Si qubits, i.e. an unaveraged measurement of electron spin within the spin relaxation time T_1 can be realised by using the Si RF-SET device.

The third key technique to be employed is the detection of single-spin states based on a spin-to-charge conversion method by utilizing spin-dependent single-electron tunnelling rates [6]. This spin measurement method employs energy selective readout based on the Zeeman energy splitting in a single QD.

Basic operation of the proposed spin qubit system is shown in Figs. 2(a) – (d). Firstly, two individual electrons are transferred from the electrodes, source1 and source2, towards the edge of the NWs (Fig. 1(a)). The two single-spins are called the spin qubit 1 and 2 hereafter. The L-shaped corners at the bottom of the NWs act as an electrostatic potential barrier caused by pattern-induced oxidation (PADOX) process, and the spin qubits 1 and 2 are therefore confined in the QDs formed between the 2nd lower gates (LTG2a and LTG2b) and the L-shaped corners. A sufficiently high external magnetic field is then applied to initialize the two spin qubits.

The nanomagnet placed near the edge of SST2D2 generates a significant magnetic field gradient and causes different magnitudes of Zeeman splitting for the 1st and 2nd spin qubits.

Manipulation and entanglement of the two spin qubits are achieved by applying a positive voltage to JG, sufficiently large enough so that the spin qubits 1 and 2 surmount the

potential barriers at the corners and interact with each other in the QD formed on the interconnect (Fig. 2(c)). After entanglement, the bias voltage to the JG is switched to negative, and the two spin qubits are pushed back to the individual QDs on the SSTDs. Finally the spin state of the spin qubit 1 is detected with the single-electron electrometer by using the spin-to-charge conversion method. This method utilizes a difference in the tunnelling probability of the spin qubit 1 from the QD back to the adjacent QD between the LTG1a and LTG2a due to a finite Zeeman splitting under an external magnetic field (Fig. 2(d)). The system presented here is purely based on single-electron-spin operation, and is significantly different to previous Si charge qubits [7] where a few tens of electrons were involved on a fabricated qubit.

The proposed fabrication process for the double spin qubit platform is to pattern the NW MOSFET channel and the electrometer on an ultrathin intrinsic SOI substrate using electron beam lithography. Thermal oxidation will be used to reduce the effective channel dimensions and subsequent pattern transfer will be done with dry etching and deposition. The poly-Si gate width and spacing are intended to be about 100 nm. After all the patterning is completed, an interlayer oxide and an upper metallic gate will be deposited.

III. DESIGN AND ANALYSIS OF OPERATION OF A SINGLE SPIN TRANSFER DEVICE

Structural design and simulation of interconnected double single spin transfer devices (SSTDs) with an electrometer is performed by combining 3D finite element method (FEM) based capacitance simulation with Monte Carlo single electron circuit simulation.

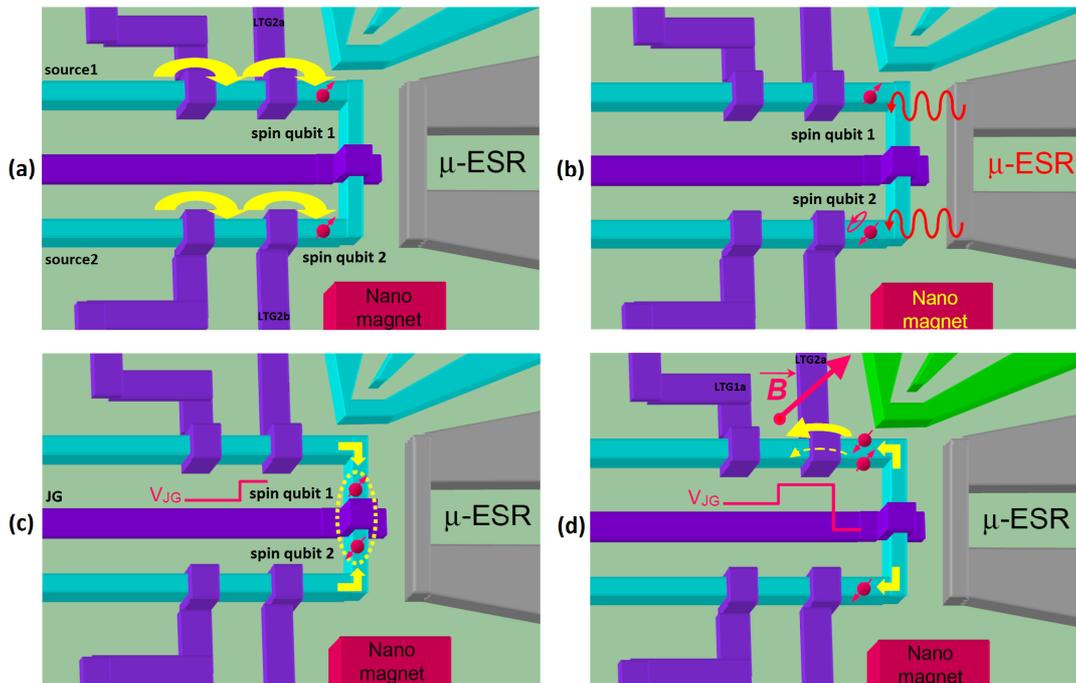


Figure 2. Operation of single spin qubits (upper gate is not shown for clarity). (a) single electron transfer into quantum boxes, (b) selective rotation by using μ -ESR, (c) entanglement and (d) readout using spin to charge conversion.

A. 3D FEM Capacitance Simulation

The platform shown in Fig. 1 is intended to have the following structural overview: the NW MOSFET channel and the electrometer are to be patterned on a 50 nm thick intrinsic SOI substrate; with NW channel width of 100 nm or less. The poly-Si gate width and spacing are intended to be less than 100 nm, and the distance between the qubit and the electrometer is about 100 nm. The interlayer oxide that covers the whole structure just below the upper metal gate will be about 50 nm in thickness.

Figure 3(a) shows a 3D model of the system. 3D structural data of the SSTD pair, the electrometer and multiple gate electrodes, based on the platform dimensions described above, are precisely input into the simulation in which potential distributions are calculated. Fig. 3(b) shows the potential distributions through the model when a potential of 1 V is applied to the substrate, the capacitance values are then obtained by integrating the surface charge density of various parts of the structure. During the simulations, a number of important structural parameters such as shape of the 3D structure, its dimensions, and its material properties were varied and their effects on the capacitance values were closely examined.

B. Single Electron Circuit Simulation

Here we focused on the single SSTD simulation which constitutes the first stage of simulations to be performed for the whole structure. The capacitance matrices extracted from the 3D FEM simulations are fed into the single-electron circuit simulator CAMSET [8].

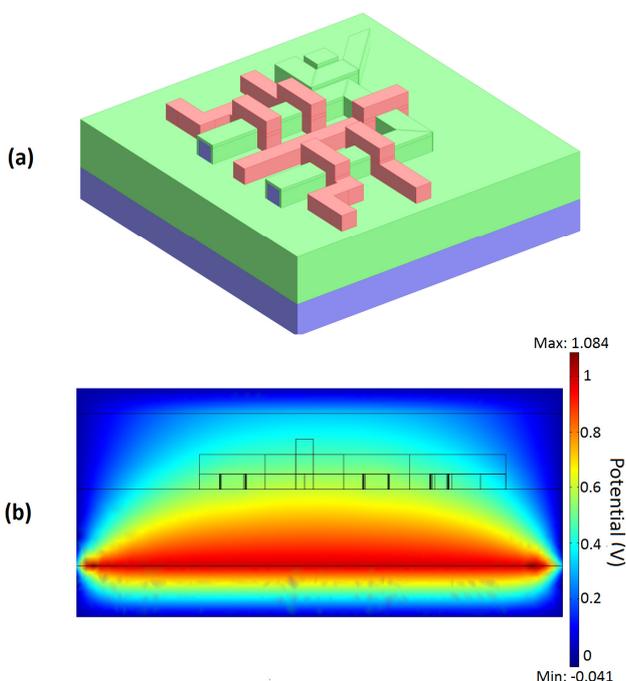


Figure 3. (a) 3D solid model of the double SSTDs integrated with the electrometer (upper gate and upper oxide are not shown for clarity) and (b) electric potential distribution when $V = 1$ V is applied to the substrate.

Fig.4 shows a circuit schematic of the SSTD used in this study. For simplicity, the MOSFETs in the SSTD were represented by single electron transistors (SETs) shown in the inset of Fig. 4. All simulations were performed at $T = 4.2$ K.

The simulation procedure is as follows. Initially, the I - V characteristics of each transistor shown in Fig. 4 were simulated to determine the Coulomb Blockade (CB) gap. After that, a voltage sequence for single electron transfer was developed as shown in Fig. 5. A positive voltage of 0.2 V is applied to the top gate (Fig. 5(a)), followed by a negative potential of -54 mV applied to the source (Fig. 5(b)). This negative voltage shifts the operating point of the SET to outside the CB region, and causes the transfer of one electron across the SET from the source to quantum dot A (QDA), which corresponds to the quantum dot between gates LTG1a and LTG2a in Fig. 1. Since the operating point of the SET cannot remain outside the CB region, it shifts back inside the CB region [9]. Turning the upper gate and the source voltages to zero, the transferred electron is confined to QDA. A potential of 275 mV is then applied to V_{g2} (Fig. 5(c)) to turn the second SET on and transfer the electron from QDA to quantum dot B (QDB), which corresponds to the quantum dot between gates LTG2a and JG in Fig. 1. V_{g2} is then switched back to zero confining the electron to QDB. With both SETs turned off, the electron is stored in QDB.

The results (Fig. 5 (d) – (e)) clearly show that single electron transfer operations have been achieved by adopting the pulse sequence shown in Fig. 5.

IV. DISCUSSION

The time required for a single electron to be transferred from source1 to QDB was estimated to be 1.85 μ s from the simulation result in Fig. 5. The turnstile device of Fig. 4 used tunnel resistance and capacitance values of 5 M Ω and 0.371 aF, respectively. These values determine the time scale (1.85 μ s) of the single electron circuit simulation. This time scale can be improved by optimizing the tunnel resistance and capacitance values of the structure.

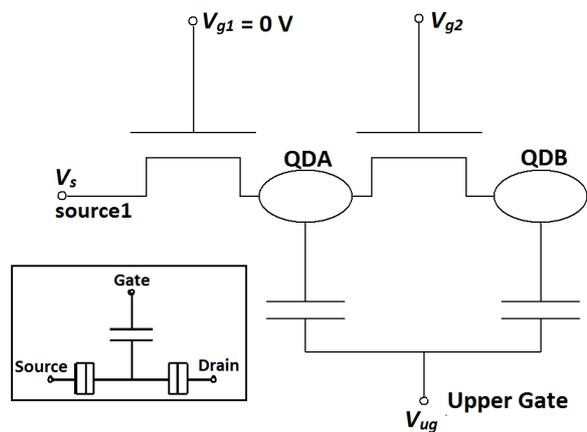


Figure 4. Schematic view of the single spin transfer device (SSTD). In the single electron circuit simulations, for simplicity purposes the SSTD MOSFETs are represented by single electron transistors (shown in the inset figure), simulations were performed at 4.2 K with tunnel resistance of 5 M Ω and tunnel capacitance of 0.371 aF.

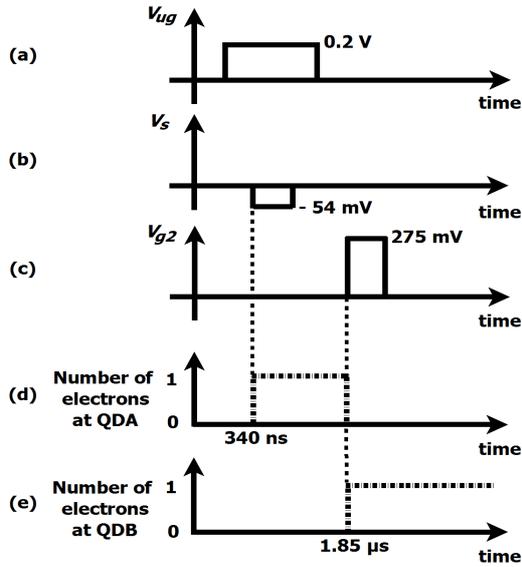


Figure 5. Single electron transfer operation through the upper SSTD of the double spin qubit system, showing the voltage pulse sequence used and the number of electrons at QDA and QDB.

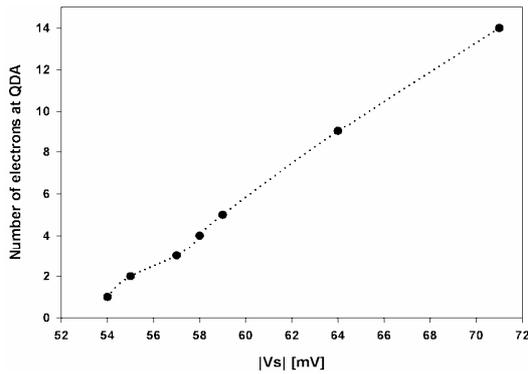


Figure 6. Effect of varying the source voltage (V_s) on the number of electrons transferred from source1 to QDA.

Here we discuss the controllability of the number of electrons to be transferred in the device. To transfer the desired number of electrons across the SSTD, the voltage scheme of Fig. 5 relies on choosing appropriate values for the upper gate and the source voltages. The upper gate voltage defines the operating point of the SET within the CB region, while the source voltage pulse determines the shift of the SET operating point outside the CB region. We fixed the pulse height of the upper gate voltage at 0.2 V and changed the pulse height of the source voltage. Fig. 6 proves that changing the pulse height of the source voltage directly affects the number of electrons transferred to QDA.

Finally we briefly mention future prospect of this work. The first part of the double spin qubit platform to be fabricated will be the SSTD integrated with the electrometer, once fabricated; it will provide a great insight into single electron transfer and detection operations. The spin to charge conversion principle can also be demonstrated in the future using the SSTD with the application of a magnetic field. After sufficient experimental verification and optimization of the

transfer and detection operations, the SSTD will evolve into an integrated SSTD pair which will be further characterised and tested, leading finally to the integration of the SSTD pair with a μ -ESR and a nanomagnet.

V. CONCLUSION

We proposed in this paper a practical system of two spin qubits by integrating all the key components in one compact silicon platform, which features excellent versatility, scalability and compatibility with conventional VLSI technology. This is the minimum necessary system to demonstrate the full operation of double spin qubits but can be scaled-up in a straightforward way to large scale systems in the future. Structural design and analysis of the system was carried out using 3D finite element method capacitance simulation, and dynamical analysis of single electron transfer operation through a single spin transfer device was demonstrated using Monte Carlo based single electron circuit simulation.

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