Focused Ion Beam Lithography and Deposition of Tungsten Contacts on Exfoliated Graphene for Electronic Device Applications

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We report a rapid prototyping method using focused ion beam (FIB) technique for accurate contacting of graphene layers and realization of a graphene devices using this method.

Graphene, a single monolayer of graphite, has recently attracted considerable research interest. It is considered a possible successor of silicon in the post-Moore era due to its unique mechanical and electronic properties. Although several methods exist for the production of graphene [1], mechanically exfoliated graphene offers the largest mono-crystalline and defect free domains. Due to the random size, shape and distribution of exfoliated flakes, however, mainly maskless fabrication processes are employed for device fabrication. Direct electron-beam lithography is already widely in use for graphene contacting [2,3], however it is resist based (a known contaminant) and requires samples with elaborate alignment structures. Another method is the use of scanning electron microscopes (SEM) integrated with a FIB gun [4], which allow in-situ e-beam examination of the graphene and individual milling or deposition of various materials though the use of a gas injection systems (GIS). A time stable and accurate (sub-µm) alignment of SEM and FIB beam in the coincident point, however, is inherently impossible due to the geometric configuration of the two beams. Thus normally imaging of the graphene using the FIB beam is necessary for nm-scale alignment. This, however, changes the properties of graphene, implants Ga-ions or even creates defects. Therefore an alignment mark procedure is used in this work and no FIB imaging of the graphene is necessary. Small trenches are sometimes observed along the edges of FIB-deposited features [5]. This is due to the competing etching and deposition process. Measures have been successfully applied in this work to avoid trenching in the channel region.

The device fabrication was carried out using a *Zeiss Nvision 40* workstation extended by a *Raith ELPHY Quantum* lithography attachment. All FIB milling and deposition was done using 30 keV. Graphene layers are mechanically exfoliated from highly oriented pyrolytic graphite (HOPG) on top of 300 nm thick SiO_2 on a p-type silicon substrate. Graphene flakes (1-5 layers) are located using optical inspection and checked using Raman spectroscopy. The FIB work involves three fabrication stages: (i) Locating the graphene flake under electron beam. Three or more alignment marks are milled close to the graphene using FIB (10 pA current, alignment accuracy to SEM picture ≤ 3 µm). (ii) Measurement of alignment mark position with respect to the graphene, and generation of an individual pattern file. (iii) Realignment of the FIB write field to the marks (6x6 μm^2 area around marks is imaged using FIB) followed by tungsten deposition (10 pA, 0.4 µs dwell time, 4 nm spacing, $W(CO)_6$ at ~$1.8x10^{-5}$ mbar chamber pressure) and line milling (10 pA, 0.1 ms dwell time, 1 nm spacing) based on pattern file. Large contact probe pads (Ti/Au) are then aligned by optical litography to the FIB tungsten tracks. Figure 1 shows a 3D schematic of the device. The channel width W_c is controlled by trenches, which also ensures current isolation to the channel area. An SEM micrograph of the channel region of a fabricated device is shown in Fig. 2. The tungsten thickness measured by AFM is ~10 nm. The device after contact pad deposition is shown in Fig. 3.

Preliminary source-drain resistance measurements on a 5-layer graphene flake show linear behavior up to 4 V. The channel resistance shows slight modulation by the applied gate voltage V_g (Fig. 4), indicating limited electric field (from back gate bias) penetration through the graphene layers. This is consistent with reports in literature [3]. Tungsten resistivity of 125 µΩcm was measured on a test structure without channel gap and is close to other reported values [5]. Measurements on a dummy structure (1 µm gap) on clean SiO_2 show negligible leakage currents.

Protoyping of devices with mono- and bi-layer graphene and channel width of ≤ 300 nm is in progress. It is expected that these show transistor-like behavior.

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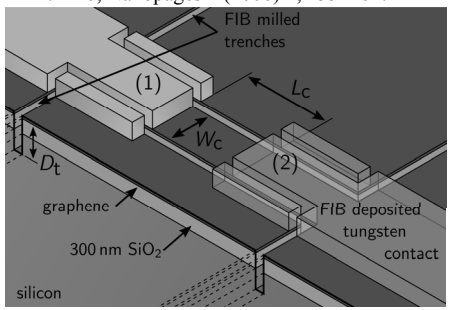

Figure 1. 3D schematics of device (not to scale). After tungsten contact deposition on top of the graphene, trenches are milled in order to restrict current flow to the channel region with width W_c and length L_c. Voltage applied between (1) and (2).

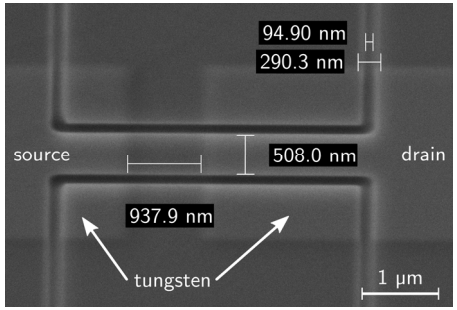

Figure 2. SEM micrograph showing the channel region of fabricated device. Multilayer graphene in channel region not visible in SEM. Trenches extend to graphene edges in order to eliminate alternative conduction paths.

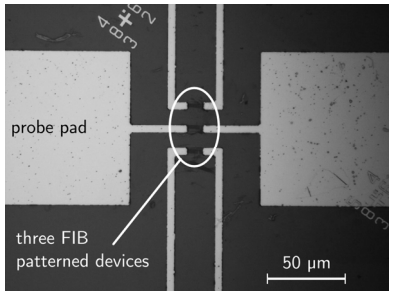

Figure 3. Optical microscope picture of contacted devices. Metallization realized by lift-off of 20/300 nm Ti/Au.

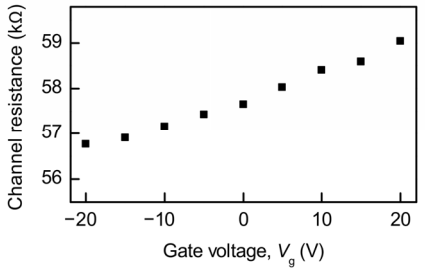

Figure 4. Measured channel resistance modulation by applied back gate voltage V_g. Channel resistance measured for source-drain voltages from -4 to 4 V.