Electrical Characteristics of Top-Down ZnO Nanowire Transistors Using Remote Plasma ALD

S. M. Sultan, K. Sun, O. D. Clark, T. B. Masaud, Q. Fang, R. Gunn, J. Partridge, M. W. Allen, P. Ashburn, and H. M. H. Chong, *Member, IEEE*

Abstract—Top-down fabrication is used to produce ZnO nanowires by remote plasma atomic layer deposition over a SiO₂ pillar and anisotropic dry etching. Nanowire field-effect transistors (FETs), with channel lengths in the range of 1.3–18.6 μm , are then fabricated using these 80 nm $\times$ 40 nm nanowires. Measured electrical results show n-type enhancement behavior and a breakdown voltage ≥ 75 V at all channel lengths. This is the first report of high-voltage operation for ZnO nanowire FETs. Reproducible well-behaved electrical characteristics are obtained, and the drain current scales with $1/L$, as expected for long-channel FETs. A respectable $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 2×10^6 is obtained.

Index Terms—Atomic layer deposition (ALD), field-effect transistor (FET), nanowire, remote plasma, top-down fabrication, ZnO.

I. INTRODUCTION

ZINC oxide is a metal oxide semiconductor with considerable potential for applications in electronics, optoelectronics, and sensors due to its wide and direct bandgap of 3.37 eV, its large excitonic binding energy of 60 meV, and its low cost [1], [2]. Even though there have been numerous reports on ZnO deposition techniques, recent attention has been focused on conventional atomic layer deposition (ALD) as the preferred growth method due to the low growth temperature and good control of thickness, composition, and uniformity [3]. ZnO thin-film transistors (TFTs) fabricated with thermal and plasma-enhanced ALD have shown excellent electrical characteristics [3], [4].

The growth of ZnO nanowires by bottom-up self-assembly has received considerable attention [2], and ZnO nanowire field-effect transistors (FETs) have been reported with excellent values of mobility [5]–[7]. However, the output characteristics of these devices show poor saturation and operation up

Fig. 1. (a) Schematic illustration of ZnO deposition over a SiO₂ pillar. (b) Schematic illustration of ZnO nanowires after etch. (c) Optical image of fabricated ZnO nanowire FET. (d) SEM cross section of ZnO nanowire formed at the side of a SiO₂ spacer.

to voltages of only a few volts. Furthermore, the control of nanowire location is difficult with bottom-up self-assembly, and hence, there is no clear route to addressable nanowire FETs. Recently, Ra *et al.* have demonstrated top-down fabrication of ZnO nanowires for sensor applications [8], but again, the output characteristics only showed low-voltage operation up to about 2 V. For successful circuit design in applications such as displays, much higher operating voltages are required [9], [10], and it is also necessary to be able to design transistors with different channel lengths.

In this letter, we report the electrical characteristics of top-down fabricated ZnO nanowire FETs using remote plasma ALD. The technology uses mature $> 1 \mu\text{m}$ photolithography and anisotropic reactive ion etching (RIE) to produce nanowires with 80 nm $\times$ 40 nm dimensions. Nanowire FETs with different channel lengths are fabricated, and well-behaved electrical characteristics are obtained, with excellent values of breakdown voltage.

II. DEVICE FABRICATION

A p-type Si wafer was used as the substrate, which also acted as the transistor back gate. A 200-nm SiO₂ layer was thermally grown and then anisotropically reactive ion etched to form 100-nm pillars with steep sides, as shown in Fig. 1(a). A 35-nm (measured by ellipsometry) layer of ZnO was then deposited at 150 $^{\circ}\text{C}$ using remote plasma ALD in an Oxford Instruments Plasma Technology (OIPT) FlexAl system using diethyl zinc as the precursor, an RF power of 100 W, a pressure of 57.5 mtorr, and an O₂ flow of 60 sccm. The advantage of using remote plasma ZnO ALD compared to water-based oxidation [3]–[5] is the reduction of OH impurities which can increase film resistivity.

Manuscript received October 5, 2011; accepted October 29, 2011. Date of publication December 12, 2011; date of current version January 27, 2012. This work was supported by the Malaysian Ministry of Higher Education through a doctoral scholarship. The review of this letter was arranged by Editor M. Passlack.

S. M. Sultan, K. Sun, O. D. Clark, T. B. Masaud, P. Ashburn, and H. M. H. Chong are with the School of Electronics and Computer Science, University of Southampton, SO17 1BJ Southampton, U.K. (e-mail: sms08r@ecs.soton.ac.uk; ks07r@ecs.soton.ac.uk; odc@ecs.soton.ac.uk; tbm206@ecs.soton.ac.uk; pa@ecs.soton.ac.uk; hmhc@ecs.soton.ac.uk).

Q. Fang and R. Gunn are with Oxford Instruments Plasma Technology, BS49 4AP Bristol, U.K. (e-mail: Qi.Fang@oxinst.com; Robert.Gunn@oxinst.com).

J. Partridge and M. W. Allen are with The MacDiarmid Institute, University of Canterbury, Christchurch 8140, New Zealand (e-mail: jim.partridge@canterbury.ac.nz; martin.allen@canterbury.ac.nz).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2011.2174607

Fig. 2. Output characteristic of a ZnO nanowire FET comprising two parallel nanowires of length $L = 8.6 \mu\text{m}$.

ZnO nanowires were fabricated using an anisotropic reactive ion CHF_3 etch in an OIPT 80+ system to form nanowires at the sides of the SiO_2 pillars, as shown in Fig. 1(b). Fig. 1(c) shows an optical image of the completed ZnO nanowire FET, and Fig. 1(d) shows a cross-sectional scanning electron microscope (SEM) image of a single nanowire. The nanowire height is approximately 80 nm and is determined by the height of the SiO_2 pillar and the amount of overetch of the ZnO layer (by 20% in this case). The nanowire width is approximately 40 nm at the base, which compares with a thickness of 35 nm after deposition. SEM images after deposition indicate that the ZnO layer is approximately 20% thicker on the pillar sidewall than on the planar surfaces, which accounts for this discrepancy. Aluminum source and drain electrodes were deposited by e-beam evaporation and patterned by lift-off. The Al contacts were then annealed at 350 °C for 2 min to improve the ohmic contact.

III. RESULTS

Fig. 2 shows the output I_D - V_D characteristic of a ZnO nanowire FET with two parallel nanowires and a channel length $L = 8.6 \mu\text{m}$ measured in the dark at room temperature. The transistor operates in the n-type enhancement mode, and the output characteristics show a well-defined linear region at low bias and excellent saturation at higher bias, indicating clear pinchoff behavior. A breakdown voltage of 75 V is obtained at $V_G = 0 \text{ V}$ and $I_D = 5 \text{ nA}$.

To test the scalability of our top-down ZnO nanowire process, Fig. 3 shows results for nanowire FETs with channel lengths of 1.3, 8.6, and 18.6 μm . Well-behaved output characteristics are obtained at all channel lengths, with clearly defined linear and saturation regions. The poor saturation seen in Fig. 3(a) for the 1.3- μm transistor suggests the presence of short-channel effects. Similar behavior has been observed in short-channel ZnO TFTs [11]. At $V_G = 10 \text{ V}$ and $V_D = 5 \text{ V}$, drain currents of 110 and 8.8 nA are obtained for $L = 1.3$ and 18.6 μm , respectively. This factor of 12.4 difference in drain current is consistent with the expected value of 14.3 obtained from the $1/L$ scaling behavior of long-channel FETs [12]. Breakdown voltages of 79 and 78 V were measured for channel lengths of 1.3 and 18.6 μm , respectively.

Fig. 3. Output characteristics of ZnO nanowire FET comprising two parallel nanowires with channel lengths L of (a) 1.3 μm , (b) 8.6 μm , and (c) 18.6 μm .

Fig. 4. Transfer characteristics for devices with different channel lengths and different numbers of parallel nanowires. (i) Sixteen-nanowire FET with $L = 8.6 \mu\text{m}$, (ii) two-nanowire FET with $L = 1.3 \mu\text{m}$, (iii) two-nanowire FET with $L = 8.6 \mu\text{m}$, and (iv) two-nanowire FET with $L = 18.6 \mu\text{m}$. The inset shows the transconductance (g_m) and field-effect mobility (μ_{FE}) as a function of gate bias at $V_D = 0.5 \text{ V}$ for $L = 8.6 \mu\text{m}$ plot.

To test the reproducibility of the fabrication process, Fig. 4(a) shows the transfer characteristic of a device with 16 parallel nanowires. This device has a drain current of 35.7 nA at $V_D = 5 \text{ V}$ and $V_G = 10 \text{ V}$, which compares with a drain current of 4.3 nA for the transistor with two parallel nanowires. The $\times 8.3$

difference in current demonstrates that the drain current scales in a reproducible way.

Fig. 4(a) also shows subthreshold characteristics for nanowire FETs with different channel lengths at $V_D = 5$ V. Subthreshold slopes of 1.02, 0.69, and 0.9 V/dec are obtained for transistors with channel lengths of 1.3, 8.6, and 18.6 μm , respectively. The poor value of subthreshold slope for the 1.3- μm device can be explained by short-channel effects due to poor control of the channel by the gate as a result of the thick gate oxide. The 8.6- μm transistor shows a respectable $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 2×10^6 , measured between $V_G = 20$ and 3 V.

IV. DISCUSSION

The transistor operation up to a voltage of 75 V shown in Fig. 2 is significantly better than the 3-V operation reported by Park *et al.* [6] and the 1.5-V operation reported by Cha *et al.* [7] for ZnO nanowire transistors fabricated by bottom-up self-assembly. This high operating voltage in small-dimension nanowire devices indicates the suitability of this device for applications such as high-resolution flat panel displays [9], [10], which require a supply voltage of 15–20 V. This is the first demonstration of high-voltage operation for ZnO nanowire transistors. The output characteristics obtained with our process are also significantly better behaved than those reported for ZnO nanowire transistors fabricated by bottom-up self-assembly. These devices tend to show either a lack of saturation or very poor saturation [6], [7]. Furthermore, the use of a top-down fabrication technique has enabled us to easily fabricate nanowire transistors with different channel lengths, thereby demonstrating the suitability of this approach for circuit design in applications such as display electronics. The realization of transistors with different channel lengths in bottom-up processes would be much more difficult to achieve.

The field-effect mobility μ_{FE} can be calculated from the peak transconductance g_m given in the inset in Fig. 4, following the method in [6]. An electron mobility of $0.5 \text{ cm}^2/\text{V} \cdot \text{s}$ is obtained, which is consistent with the range of values from 0.3 to $17 \text{ cm}^2/\text{V} \cdot \text{s}$ reported for ZnO TFTs fabricated using ALD [14]. A mobility toward the bottom end of this range might be expected for our nanowire FETs due to roughness from the nanowire RIE, which has not been optimized. To test this possibility, the mobility was measured on TFTs on the same wafer as the nanowire transistors. A mobility of $1.0 \text{ cm}^2/\text{V} \cdot \text{s}$ was obtained, which is higher than the value obtained on nanowire transistors. This result suggests that there is considerable scope to improve the mobility of our nanowire FETs by optimizing the ZnO ALD process.

Reported values of mobility for bottom-up ZnO nanowire FETs show wide variation, with values ranging from 0.53 [15] to $3118 \text{ cm}^2/\text{V} \cdot \text{s}$ [5]. This very high value of mobility was obtained on passivated nanowires, and much lower values of 20–80 $\text{cm}^2/\text{V} \cdot \text{s}$ were obtained on unpassivated nanowires. A similar improvement in mobility from 75 to 1000 $\text{cm}^2/\text{V} \cdot \text{s}$ was reported by Park *et al.* when their nanowires were passi-

vated with polymer [6]. It is likely, therefore, that much higher values of mobility could be achieved in our ZnO nanowire FETs by using a passivation layer.

In conclusion, we have successfully demonstrated the top-down fabrication of ZnO nanowire FETs using remote plasma ALD and anisotropic RIE. Transistors with channel lengths in the range of 1.3–18.6 μm have been fabricated, and a breakdown voltage of ≥ 75 V has been achieved at all channel lengths which is ample for applications such as active-matrix display electronics. Well-behaved electrical characteristics are obtained, and the drain current scales as $1/L$, as expected for long-channel FETs.

ACKNOWLEDGMENT

S. M. Sultan would like to thank the Faculty of Electrical Engineering, Universiti Teknologi Malaysia, Johor Bahru, for supporting her doctoral studies.

REFERENCES

- [1] U. Özgür, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. J. Cho, and H. Morkoc, "A comprehensive review of ZnO materials and devices," *J. Appl. Phys.*, vol. 98, no. 4, p. 041301, Aug. 2005.
- [2] S. J. Pearton, D. P. Norton, and F. Ren, "The promise and perils of wide-bandgap semiconductor nanowires for sensing, electronic, and photonic applications," *Small*, vol. 3, no. 7, pp. 1144–1150, Jul. 2007.
- [3] S. Kwon, S. Bang, S. Lee, S. Jeon, W. Jeong, H. Kim, S. C. Gong, H. J. Chang, H.-H. Park, and H. Jeon, "Characteristics of the ZnO thin film transistor by atomic layer deposition at various temperatures," *Semicond. Sci. Technol.*, vol. 24, no. 3, p. 035015, Mar. 2009.
- [4] D. A. Mourey, D. A. Zhao, J. Sun, and T. N. Jackson, "Fast PEALD ZnO thin-film transistor circuits," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 530–534, Feb. 2010.
- [5] P.-C. Chang and J. G. Lu, "ZnO nanowire field-effect transistors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2977–2987, Nov. 2008.
- [6] W. I. Park, J. S. Kim, G.-C. Yi, M. H. Bae, and H. J. Lee, "Fabrication and electrical characteristics of high-performance ZnO nanorod field-effect transistors," *Appl. Phys. Lett.*, vol. 85, no. 21, pp. 5052–5054, Nov. 2004.
- [7] S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amaratunga, G. W. Ho, M. E. Welland, D. G. Hasko, D.-J. Kang, and J. M. Kim, "High performance ZnO nanowire field-effect transistor using self-aligned nanogap gate electrodes," *Appl. Phys. Lett.*, vol. 89, no. 26, p. 263102, Dec. 2006.
- [8] H.-W. Ra, K.-S. Choi, J.-H. Kim, Y.-B. Hahn, and Y.-H. Im, "Fabrication of ZnO nanowires using nanoscale spacer lithography for gas sensors," *Small*, vol. 4, no. 8, pp. 1105–1109, Aug. 2008.
- [9] S.-H. K. Park, C.-S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J.-I. Lee, K. Lee, M. S. Oh, and S. Im, "Transparent and photo-stable ZnO thin-film transistors to drive an active matrix organic-light-emitting-diode display panel," *Adv. Mater.*, vol. 21, no. 6, pp. 678–682, Feb. 2009.
- [10] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In-Ga-Zn-O thin-film transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, p. 044305, Aug. 2010.
- [11] H.-H. Hsieh and C.-C. Wu, "Scaling behavior of ZnO transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 89, no. 4, p. 041109, Jul. 2006.
- [12] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. New York: Wiley-Interscience, 2007.
- [13] Q. Zhang, J. Qi, Y. Yang, Y. Huang, X. Li, and Y. Zhang, "Electrical breakdown of ZnO nanowires in metal–semiconductor–metal structure," *Appl. Phys. Lett.*, vol. 96, no. 25, p. 253112, Jun. 2010.
- [14] P. F. Carcia, R. S. McLean, and M. H. Reilly, "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 88, no. 12, p. 123509, Mar. 2006.
- [15] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, "Single crystal nanowire vertical surround-gate field-effect transistor," *Nano Lett.*, vol. 4, no. 7, pp. 1247–1252, Jul. 2004.