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Circuit-level Modelling and Simulation of Carbon Nanotube Devices

by

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ABSTRACT

FACULTY OF ENGINEERING, SCIENCE AND MATHEMATICS
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The growing academic interest in carbon nanotubes (CNTs) as a promising novel class of electronic materials has led to significant progress in the understanding of CNT physics including ballistic and non-ballistic electron transport characteristics. Together with the increasing amount of theoretical analysis and experimental studies into the properties of CNT transistors, the need for corresponding modelling techniques has also grown rapidly. This research is focused on the electron transport characteristics of CNT transistors, with the aim to develop efficient techniques to model and simulate CNT devices for logic circuit analysis.

The contributions of this research can be summarised as follows. Firstly, to accelerate the evaluation of the equations that model a CNT transistor, while maintaining high modelling accuracy, three efficient numerical techniques based on piece-wise linear, quadratic polynomial and cubic spline approximation have been developed. The numerical approximation simplifies the solution of the CNT transistor's self-consistent voltage such that the calculation of the drain-source current is accelerated by at least two orders of magnitude. The numerical approach eliminates complicated calculations in the modelling process and facilitates the development of fast and efficient CNT transistor models for circuit simulation.

Secondly, non-ballistic CNT transistors have been considered, and extended circuit-level models which can capture both ballistic and non-ballistic electron transport phenomena, including elastic scattering, phonon scattering, strain and tunnelling effects, have been developed. A salient feature of the developed models is their ability to incorporate both ballistic and non-ballistic transport mechanisms without a significant computational cost. The developed models have been extensively validated against reported transport theories of CNT transistors and experimental results.

Thirdly, the proposed carbon nanotube transistor models have been implemented on several platforms. The underlying algorithms have been developed and tested in MATLAB, behavioural-level models in VHDL-AMS, and improved circuit-level models have been implemented in two versions of the SPICE simulator. As the final contribution of this work, parameter variation analysis has been carried out in SPICE3 to study the performance of the proposed circuit-level CNT transistor models in logic circuit analysis. Typical circuits, including inverters and adders, have been analysed to determine the dependence of the circuit's correct operation on CNT parameter variation.

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Chapter 1

Introduction

1.1 Overview

Since the discovery of carbon nanotubes (CNTs) by Iijima in 1991[1], this new type of material continues to attract attention for its great potential to be applied as metallic nanowires and active semiconductor devices in next generation integrated circuits (ICs). Significant progress has been achieved in terms of both understanding the fundamental electronic properties and exploring possible engineering applications of CNTs [2]. Nanoelectronic devices have been extensively explored since the demonstration of the first carbon nanotube field-effect transistors (CNTFETs) [3]. CNT based transistors have been demonstrated both theoretically and experimentally. The transport characteristics of CNTs have been considered to be of significant importance for a CNT based transistor and thus have been widely studied. Ideally, for a carbon nanotube with its length much shorter than the mean free path of conduction electrons, a ballistic regime is generally exhibited in the nanotube [4]. However, the transport mechanism of CNT transistors is complicated and the extensive existence of non-idealities may result in non-ballistic transport. The transport type in carbon nanotubes, ballistic or non-ballistic, depends on the energy region, on which the theoretical analysis of CNT transistors should be focused.

The modelling of carbon nanotube devices, especially CNT transistors, has been devel-

oped significantly during the past several years. A number of CNT transistor models have been proposed in both experimental and theoretical studies. Significant progress has been made in understanding the operation mechanisms of CNT transistors. Early research demonstrated that CNT transistors operate like metal-oxide-semiconductor field-effect transistors (MOSFETs) [5, 6] or Schottky-barrier (SB) transistors [7, 8]. Nevertheless, as more electronic characteristics of CNT devices are revealed, both behavioural-level and circuit-level models have recently emerged and been applied into the simulation of CNT logic circuits [9, 10, 11]. Common techniques for modelling CNT transistors depend on the numerical evaluation of integrals or internal Newton-Raphson iterations in the energy domain within the nanotube to find solutions of non-linear dependencies [12], which encounter calculation complexities and are consequently time-consuming. Additionally, early CNT transistor models can only describe ideal ballistic transport properties and are not sufficient for practical use. Recently, new techniques which use symbolic approximation of mobile charge densities [11] and count in subband effects of CNTs [13, 14] have been developed to improve the efficiency and availability of the models. Though great efforts have been made, CNT transistor models are still being developed and novel methodologies remain to be identified.

Similarly to the development of most electronic device models, simulation is needed in order to address scientific and technological questions in the rapidly developing field of modelling CNT transistors [15]. Currently, most CNT transistor models describe the DC transport characteristics within the channel, and simulation can be made to numerically identify the relations between different parameters and the flow of carriers through the carbon nanotube channel, which verify the performance of the proposed models and help to optimise them [9, 10, 11]. A number of theoretical CNT transistor models [12, 16] have been developed, which derive ideal ballistic output results in simulation but consume much CPU resource, and are thus not efficient enough for practical use. Therefore, novel numerical modelling techniques are needed to shorten the simulation periods without losing much accuracy, especially when applied to circuits. Although numerical modelling techniques have recently been proposed [9, 16], the simulation results diverge and there is a lack of comparisons with experiments. In the light of non-idealities (defects, misalignment, etc.) of CNTs, the proposed models are required to be able to

reflect these non-ideal effects on the transport characteristics of CNT transistors in simulation. The performance of the proposed models also needs to be compared with results obtained from both numerical analysis and experiments. Both theoretical analysis of the electronic properties of CNT transistor and improvement of the modelling techniques are needed.

Within this context, this chapter is organised as follows: Section 1.2 gives a broad view on CNT transistor design and illustrates the potential applications of CNT transistors and some main challenges that are tackled as part of this research. Section 1.3 presents the main objectives and contributions of this work. Finally, Section 1.4 outlines the structure of the thesis.

1.2 Carbon Nanotube Transistor Modelling

Semiconducting carbon nanotubes have impressive electronic features and as a result are promising new material for the next generation of ICs. CNT transistors have been constructed experimentally and their performance has been demonstrated to exceed conventional silicon FETs [17, 18]. Furthermore, the need for developing models which can describe the characteristics of CNT transistors is increasing. A number of current techniques for CNT transistor modelling employ MATLAB to numerically present the transport mechanism [12, 16, 19]. In numerical models, the electronic parameters of CNT transistors are quantified and the relationships between the inner components are also represented by mathematical equations. However, these models are based on ideal numerical equations and their performance in practice differs from that obtained in simulation since the non-ballistic transport characteristics of CNT transistors are not included in the proposed numerical models. Most recently reported models are based on numerically describing the transport characteristics of CNTs [20, 21, 22], which implies the importance of revealing the electronic mechanism of the nanotube. Although some theories have been suggested, there are still some phenomena that need theoretical explanation. For example, the doping mechanism of CNTs is quite different from silicon and plays a significant role in the mobility of the nanotube. This can explain why

most existing models are focused on the ballistic transport characteristics. Recently symbolic approximation for modelling charge densities in the ballistic region of a CNT transistor has been presented [11, 23]. The approximation technique permits a fast and accurate calculation of the charge densities within the CNT channel, which presents a closed-form solution to the drain-source current in a CNT channel as a function of parameters including temperature, terminal voltages, Fermi level, and CNT diameter of the transistor.

The aim of modelling CNT transistors is to predict the performance of circuits with CNT devices by running simulation before fabrication, expecting that the simulation results can reflect the performance of real devices. At present there is a gap between simulation and experimental results. One reason is that the electronic mechanism of CNTs are yet to be established; another reason is that the fabrication of CNT transistors is difficult to control and no uniform results are obtained from various experiments, which implies that feasible approaches to fabricating CNTs are still under development.

1.2.1 Research Challenges

There are a number of challenges in CNT device modelling and this research focuses on the following key challenges:

- A main challenge is the need for efficient and effective modelling techniques to provide fast and accurate simulation of CNT transistors. Some existing models employ numerical methods to present the physical characteristics but at the expense of high simulation time [12, 16]. Recently, symbolic and numerical approximation has been proposed to simplify the calculation complexity of CNT transistor models [11, 23], but more efforts are required in this area. In this research, the trade-off between accuracy and simulation time of models is investigated.

- Current CNT transistor models do not incorporate non-ballistic transport mechanisms including scattering and tunnelling. Also, there is little reported work showing discrepancies between computing simulation and experimental results of

CNT devices. To implement models that can describe both ballistic and non-ballistic characteristics of CNT transistors, theories explaining non-ballistic effects need to be revealed, and numerical equations have to be developed before these effects can be combined in the model. Furthermore, comparison between the simulation results of developed models and those from experiments needs to be carried out to validate the performance of the proposed models.

- Although a number of numerical CNT transistor models have recently been developed, there is a lack of research on SPICE-level implementation of CNT devices. Numerical or behavioural models can describe the general transport characteristics of the CNT transistor. However, some electronic effects that might affect the operation of CNT devices at circuit level, including the bulk effect of the transistor, are not included in the proposed models. SPICE models of CNT transistors which are suitable for practical circuit-level simulation need to be developed.

- Considering the variation of parameters of CNTs (Fermi level, diameter, band gap, and chirality, etc.) and the existence of defects (metallic nanotube [24] and impurities [25], etc.), variation analysis is necessary for practical CNT transistor models. Some experiments have demonstrated the effects caused by parameter variation [26, 27]. By including such variation in models, users would be able to predict better correlation between simulation and the measured results of practical circuits and obtain the percentage of functionally working devices via simulations.

1.3 Research Aims and Contributions

New modelling and simulation techniques are necessary for carbon nanotube devices to establish their potential in logic circuit design. The main aim of this research is to investigate and develop efficient models of CNT transistors based on numerical approximation. It is expected that new modelling techniques for CNT devices can be developed and circuits based on the proposed CNT transistor models can be simulated. This research also involves developing efficient CNT transistor models which can describe both ballistic and non-ballistic transport characteristics and their application for CNT circuit

design. Furthermore, the simulation of proposed models on various platforms (numerical, behavioural and circuit level) is required to analyse the performance of the developed CNT transistor models in logic circuits. This research makes contributions in nanoelectronic circuit design and development of fast and accurate CNT transistor models which allow CNT based circuits with large numbers of such devices to be simulated efficiently and accurately. The contributions of this research are:

- **Numerical approximation techniques for modelling transport characteristics of CNT transistors:** This contribution represents a significant improvement in achieving fast and accurate techniques for modelling CNT transistors. The proposed techniques are based on very efficient numerical approximations (piece-wise linear, piece-wise quadratic and cubic spline) of the non-equilibrium mobile charge density, which considerably accelerate the evaluation of the CNT drain-source current while maintaining high modelling accuracy. Piece-wise approximation can replace complicated calculations in the modelling process and contribute to provide fast and numerically efficient CNT transistor models, while cubic spline algorithm allows an automatic approximation process and operates more accurately. Presented results further reinforce the suggestion that numerical integrations and internal Newton-Raphson iterations can be avoided in the calculation of the self-consistent voltage V_{SC} of CNT transistors (explained in detail in Section 3.1), and a computational time saving of more than three orders of magnitude can be achieved. Three papers describing this contribution were published at the 2007 Nanoarch conference [28], the 2008 Design, Automation & Test in Europe (DATE) conference [29], and the 2008 Forum on specification & Design Languages (FDL) conference [30].

- **CNT transistor models with non-ballistic transport characteristics:** This contribution demonstrates that effects of elastic scattering, phonon scattering, strain and tunnelling may influence the transport characteristics of CNT transistors. A new model that can reflect these non-ballistic transport characteristics has been developed. A salient feature of the proposed model is its ability to incorporate both ballistic and non-ballistic transport effects without a significant computa-

tional cost. The proposed model has been extensively validated against reported CNT ballistic and non-ballistic transport theories and experimental results. A journal paper introducing the developed model which is capable of analysing both ballistic and non-ballistic performance of CNT transistors has been published in IEEE Transactions on Nanotechnology [31].

- **SPICE-level implementation of CNT transistor models:** Based on the numerical analysis of the self-consistent voltage developed as part of this project, both HSPICE and Berkeley SPICE3 CNT transistor models which combine both ballistic and non-ballistic transport characteristics have been obtained and simulations of both models have been carried out. To validate the performance of the proposed models, some reported experimental characteristics have been compared with the simulation results of the proposed models and the differences are within an acceptable range. This contribution has shown that the proposed SPICE-level models can derive fast and accurate performance with low supply voltages. Additionally, its power efficiency makes the proposed SPICE3 model particularly suitable for implementation in circuit-level simulators where large numbers of such devices may be used to build complex circuits. A paper describing this contribution has been published at the 2009 Forum on specification & Design Languages (FDL) conference [32].

- **Parameter variation analysis of CNT transistor models:** Following the implementation of the SPICE-level models of CNT transistors, variation analysis of the proposed SPICE3 model has been carried out and circuits with non-ballistic CNT transistors have been simulated to verify the feasibility of the model. Parameter variation which can wildly affect the transport characteristics of CNT transistors exists. Simulation of CNT transistors with Fermi level variation has been carried out and estimation of the percentage of working components out of all simulated devices has been made.

1.4 Thesis Organisation

This thesis is divided into seven chapters. Chapter 2 provides a literature review which introduces the development of CNT device modelling and presents the potential questions in modelling carbon nanotube transistors. Chapter 3 demonstrates new CNT transistor modelling techniques based on numerical piece-wise approximation (piece-wise linear and quadratic polynomial) of the non-equilibrium mobile charge density within the CNT channel. Ballistic models based on these numerical techniques have been simulated and their efficiency and accuracy have been established. Chapter 4 introduces the cubic spline algorithm for the numerical modelling of CNT transistors, which creates an automatic and accurate solution of the numerical relationship between the mobile charge density and the self-consistent voltage, leading to the speed-up of deriving the current through the channel without losing much accuracy. Behavioural-level implementation of the cubic spline based model has been carried out using VHDL-AMS and simulations of logic circuits based on the proposed CNT transistor model have been made. Chapter 5 presents a new model to incorporate both ballistic transport as well as non-ballistic effects of CNT transistors. The developed model has been developed based on the cubic spline approximation and simulated in MATLAB. The performance of the proposed model has been compared with reported experimental results. Chapter 6 indicates the SPICE-like implementation of CNT transistor models using numerical approximation of non-equilibrium mobile charge densities, and provides simulation results which demonstrate the applications of the proposed models in logic circuits. Detailed simulations of CNT devices using the developed models are presented. Also in Chapter 6, parameter variation analysis of the proposed SPICE3 model is carried out to demonstrate the feasibility of the model in practical circuits. Finally, Chapter 7 concludes the research contributions and discusses potential directions for further research.

Chapter 2

Literature Review

Chapter 1 highlighted the importance and challenges of developing modelling techniques for CNT transistors, suggesting novel numerical approximations to simplify the modelling process for both ballistic and non-ballistic transport characteristics of CNTs. Before explaining the specific work in the research, background knowledge of carbon nanotubes is described in this chapter, which covers a brief review of semiconductor device models in Sections 2.1 and 2.2. The electronic characteristics of CNTs are described in Section 2.3, and recent efforts on modelling CNT devices are introduced in Section 2.4. The latest research on circuit-level modelling and simulation of CNT transistors is also presented and serves as an orientation of this research in Sections 2.5 - 2.8. Section 2.9 provides a brief summary of parameter variation and its effect on the performance of CNT transistors. Finally, Section 2.10 concludes this chapter.

2.1 Semiconductor Device Models

Silicon has played a fundamental role in the semiconductor industry and most semiconductor device models are based on silicon materials. This section gives a brief introduction of traditional semiconductor devices and the development of these devices during the past decades.

The semiconductor is a type of solid material whose electrical conductivity is in between

a conductor and an insulator. Its special transport characteristics are determined by the small band gaps, which allow a number of environmental factors including temperature and light to control its electrical properties [33].

A p-n junction is a structure formed by combining p-type and n-type semiconductors together in very close contact [34]. The term junction refers to the region where the two regions of semiconductors meet. The p-n junction has been applied widely as a basic structure in modern electronics. One of the most popular applications of the p-n junction is the diode. In a p-n diode, conventional current can flow from the p-type side (the anode) to the n-type side (the cathode), but cannot flow in the opposite direction. Another type of semiconductor diode, the Schottky diode, is formed from the contact between a metal and a semiconductor rather than by a p-n junction [35].

One of the most important semiconductor devices is the bipolar junction transistor (BJT), which was invented at Bell Laboratories in 1947 [36]. In BJTs, both electrons and holes participate in the conduction process. Bipolar transistors have been extensively used in high-speed circuits, analogue circuits, and power applications [37]. The field-effect transistor (FET) is a type of transistor that depends on an electric field to control the conductivity of a channel of one type of charge carrier in a semiconductor material. FETs are sometimes called unipolar transistors to contrast their single-carrier-type transport with the dual-carrier-type operation of BJTs [38]. A traditional metal-oxide-semiconductor (MOS) structure is obtained by depositing a layer of silicon dioxide (SiO_2) and a layer of metal on top of a semiconductor die. As the silicon dioxide is a dielectric material its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor [39].

The MOSFET (metal-oxide-semiconductor field-effect transistor) was created by Kahng and Atalla in 1960 [40]. In a MOSFET, the source and drain are connected by a conducting surface channel through which carriers can flow when properly modulated by the gate voltage [41]. The source and drain regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. Recently, MOSFETs have been scaled down significantly and the Si-SiO_2 interface remains the most important combination [42].

Scaling down the dimensions of MOSFETs is a continuous trend. The difficulties with reducing the size of the MOSFET include the semiconductor device fabrication process, the need for very low voltages, and with poorer electrical performance the necessity of circuit redesign and innovation [43]. It has been stated that smaller transistors switch faster, which is the main motivation for scaling down the dimensions of semiconductor devices [44].

2.2 Modelling and Simulation of Semiconductor Devices

In this section, the development of semiconductor modelling techniques is reviewed and a general introduction of simulation is also included.

The physical properties of semiconductor devices are complicated and equivalent models are needed for reliable fabrication in practice. In order to ensure the correct operation of circuits employing semiconductor devices, it is necessary to model the physical phenomena observed in experiments and predict the performance of devices correctly in simulation [45]. The modern transistor has an internal structure that exploits complex electronic mechanisms. Providing information about how the device is formed, process models simulate the manufacturing steps and provide a microscopic description of device geometry to the device simulator [46].

Different from process models, with information about what the device looks like, the device simulator models the physical processes taking place in the device to determine its electrical behaviour in a variety of aspects: DC current-voltage behaviour, transient response, or dependence on device layout, such as long and narrow versus short and wide, or interdigitated versus rectangular, or isolated versus proximate to other devices [47]. Simulations can inform the device designer whether the device process will produce devices with the electrical behaviour needed by the circuit designer, and are used to inform the process designer about any necessary process improvements [48]. Once the process gets close to manufacture, the predicted device characteristics are compared with measurement on test devices to check that the process and device models are working adequately.

In the early years, initial semiconductor devices were modelled in a very simple way, for instance, mainly drift and diffusion current were considered for basic transistor models; but today more effects must be taken into account for a practical model. For example, leakage currents in junctions and insulator, saturation current and non-ballistic transport, quantum mechanical effects and even the combination of multiple materials. Techniques change and the models need updates to adjust for new physical effects, or to provide better performance [49, 50].

As part of the development of modelling techniques, various computer languages for modelling have been developed. VHDL-AMS is a derivative of the hardware description language VHDL [51]. It includes analogue and mixed-signal extensions (AMS) in order to define the behaviour of analogue and mixed-signal systems. The VHDL-AMS standard was created with the intention of enabling the designers of analogue and mixed signal systems and integrated circuits to create and use modules that encapsulate behavioural-level descriptions as well as structural-level descriptions of systems and components. VHDL-AMS has become an industry standard modelling language for mixed signal components and circuits [52].

SPICE (Simulation Program with Integrated Circuit Emphasis) was developed at the University of California, Berkeley, in the early 1970s [53]. It was introduced as a general purpose simulator for analogue electronic circuits which can be used in transistor-level design to check the integrity of circuit designs and to predict circuit behaviour.

Containing analysis and models needed for integrated circuits design, SPICE has become popular and is widely used in industry. SPICE can drive operating point solutions, transient analysis, and various small-signal analysis with components and parameters to simulate circuits with different structures [54].

2.3 Carbon Nanotube Characteristics

Carbon nanotubes, as novel materials with unique electronic characteristics, have been anticipated to be exploited to construct electronic devices for their better physical properties than those of conventional silicon, for example, longer mean free path, larger

carrier mobility, and higher transport current density. This section introduces the characteristics of carbon nanotubes and describes some of their potential applications.

2.3.1 General Introduction to Carbon Nanotubes

The nanotube can be conceptually viewed as a rolled-up graphene sheet [55]. A common way to describe the one-dimensional energy-lattice vector $(E - k)$ relation of the carbon nanotube, which governs its electronic property, is to quantise the two-dimensional $E - k$ of the graphene sheet along the circumferential direction of the nanotube [22]. Understanding the electronic characteristics of the graphene sheet helps to understand the electronic properties of carbon nanotubes. Graphene is known as a two-dimensional zero-gap semiconductor [56]; for most directions in the graphene sheet, there is a band gap, and electrons are not free to flow along those directions unless extra energy is applied. However, in certain special directions (with zero gap) graphene is metallic, and electrons flow freely along those directions. This feature is not obvious in bulk graphite, since there is always a conducting metallic path which can connect any two points, and hence graphite conducts electricity. However, when rolling up graphene to make a nanotube, a special direction is selected, which is the direction along the axis of the nanotube. Depending on this direction, metallic and semiconducting nanotubes can be obtained [57].

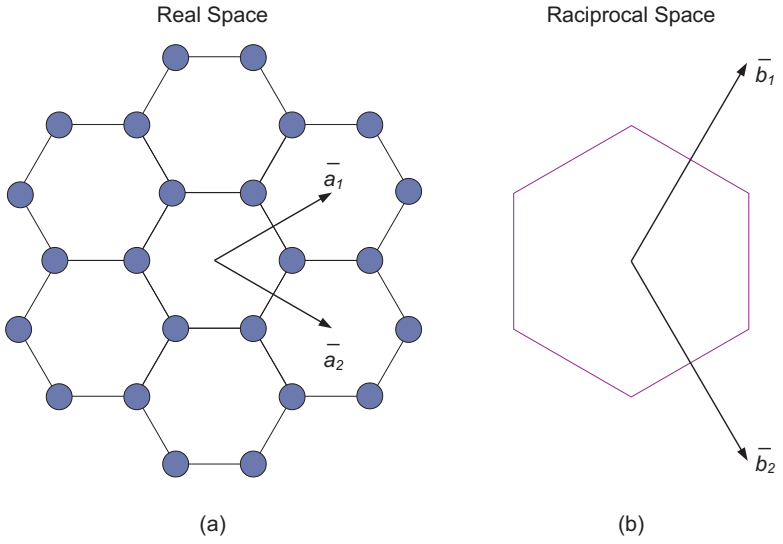

FIGURE 2.1: The graphene lattice in real space and reciprocal space with the basis lattice vectors [55].

The two-dimensional graphene lattice in real space can be created by translating one unit cell by the vectors $\overrightarrow{T} = n\overrightarrow{a_1} + m\overrightarrow{a_2}$ with integer combinations (n,m), where $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ are basis vectors of the real space lattice (as shown in Figure 2.1(a)) and $\overrightarrow{b_1}$ and $\overrightarrow{b_2}$ are basis vectors in the reciprocal space (Figure 2.1(b)). It has been widely proposed that the lattice structure determines the conducting characteristics of the carbon nanotube [22, 55, 58]. If (n - m) mod 3 = 0, the CNT is metallic; if (n - m) mod 3 $\neq$ 0, the CNT is semiconducting [55]. Both metallic and semiconducting nanotubes can be exploited as interconnect and components in circuits. Due to their nanoscale dimensions, electron transport in carbon nanotubes will take place through quantum effects and will only propagate along the axis of the tube. Because of this special transport property, carbon nanotubes are frequently referred to as one-dimensional transport.

In terms of numbers of graphene layers, carbon nanotubes can be cataloged as single-walled carbon nanotubes (SWCNTs) and multi-walled ones (MWCNTs) [2], both of which can be synthesised simultaneously under certain experimental conditions. However, the number of layers and physical features of MWCNTs are difficult to control [59]. Though researchers face a number of problems in generating separate single-walled carbon nanotubes with required characteristics [60], SWCNTs draw much academic interest due to their unique features. The conductivity and resistivity of single walled nanotubes have been measured by placing electrodes at different parts of the CNTs [61]. The resistivity of the single walled nanotubes ropes is of the order of $10^{-4}\ \Omega \cdot cm$ at room temperature. This means that single walled nanotube ropes are the most conductive carbon fibers known. The current density that can be achieved is $10^{7}\ A/cm^2$, however in theory single walled nanotube ropes should be able to sustain much higher stable current densities, as high as $10^{13}\ A/cm^2$. The prospects of mixed bundle of CNTs as low-power high-speed interconnects for future VLSI applications has been recently investigated [62]. The power dissipation and delay of CNT bundle interconnects have been examined and compared with that of copper (Cu) interconnects at the 32-nm technology. Experimental results showed that a CNT bundle consumes 1.5 to 4-fold less power than Cu for intermediate and global interconnects.

2.3.2 Electronic Properties of Different Types of Carbon Nanotubes

In the light of transport conductivity, carbon nanotubes can be catalogued as metallic or semiconducting carbon nanotubes [63], which is decided by the energy band gap between the atoms. The conductive type of the CNTs depends on its chirality [55]. Both metallic and semiconducting CNTs have been studied as potential electronic components and their electronic properties have been established.

2.3.2.1 Metallic Carbon Nanotubes

Devices made from metallic SWCNTs were first measured in 1997 [64], and have been extensively studied since that time. Conductances of two-terminal metallic SWCNTs at room temperature can vary significantly [65]. Most of this discrepancy is due to variation in contact resistance between the electrodes and the tube [66]. As techniques for making improved contacts have been developed, the conductances of CNTs have steadily improved. Additionally, optic and zone-boundary phonons [67] have the necessary momentum to backscatter electrons in nanotubes, and scattering of static disorder is also possible in metallic tubes [68].

A number of experiments have corroborated the statement that metallic CNTs have greater conductivity than conventional metals. Measurement of short tubes was made, in which $G = 4q^2/h$ was derived [69]. Meanwhile, scanned probe experiments testing the local voltage drop along the length of the nanotube were carried out, which showed that the mean-free path of metallic CNTs corresponding to a room temperature resistivity is about $10^{-6}m$, much longer than that of metals. Therefore, the conductivity of metallic nanotubes can be equal to, or even exceed, the conductivity of best metals at room temperature [70].

These long scattering lengths are in contrast to the behaviour observed in traditional metals like copper, where scattering lengths are typically of the order of tens of nanometers at room temperature, due to phonon scattering. The main difference is the significantly reduced phase space for scattering by acoustic phonons in a 1-D system [22]. At room temperature, acoustic phonons have much less momentum than the electrons

at the Fermi energy. In a traditional metal, phonons backscatter electrons through a series of small angle scattering events that eventually reverse the direction of an electron. While the mean-free path is much larger than traditional metals, conductivity is only comparable to slightly better. This is because the effective mobile charge density of states in nanotubes is much lower than in traditional metals [71].

2.3.2.2 Semiconducting Carbon Nanotubes

Semiconducting CNTs can be derived by choosing specific chirality for the nanotubes (see Section 2.3.1). The electron transport characteristics for semiconducting, single-walled CNTs with diameters ranging from small to relatively large has been calculated [72]. The Boltzmann transport equation is solved using both an iterative technique and a Monte Carlo method. The basis for the transport characteristics is provided by electronic structure calculations of a tight-binding CNT model.

The electron transport characteristics of semiconducting carbon nanotubes connected to metallic electrons have been investigated [73]. For short nanotubes, the effect of the metallisation of the semiconducting nanotube due to the metallic electrode contact is large. The electrons are transmitted through the semiconducting nanotube even at the Fermi energy due to the contact effect. With an increase in the length of the nanotube, this effect declines and a gap-like structure appears.

It has been demonstrated that the carrier mobility and mean free path of semiconducting CNTs are related to temperature and tube chirality. Both of them drop when the lattice temperature rises. The effect is more significant in CNTs with relatively larger diameters, where non-parabolic effects become dominant [74]. The band structure is approximately independent of chirality in the low-field approximation. The mobility and mean free path both decrease with increasing chiral angle, and are therefore smallest in armchair tubes (with CNT vector (n,n)) and largest in zigzag tubes (with CNT vector (n,0)).

Recently, semiconducting carbon nanotubes have been demonstrated to have potential applications in high-mobility electronic devices [75]. Researchers have found typical mobilities of 1000-10,000 $cm^2/V{\cdot}s$ for CVD-grown tubes, with occasional devices hav-

ing mobilities as high as 20,000 $cm^2/V{\cdot}s$, which is significantly higher than the values reported to date in deposited nanotubes [76]. It is also higher than the mobilities in silicon MOSFETs, indicating than SWCNTs are a remarkably high-quality semiconducting material.

Apart from mobilities, the band structure of carbon nanotubes is another significant factor affecting the electronic characteristics. Ming Zang et al. [77] suggested a curvilinear coordinate system in space and in k-space to study the energy band of single-walled carbon nanotubes wrapped at a helical angle. It is suggested that for tubes with different diameters, there is a distance between their cylindrical Brillouin zones in the radial direction. The Brillouin zone varies with the radius of the tube and the number of cells on the circumference [78]. It is also reported that mobility increases rapidly with tube diameter and increases slowly with temperature [79]. Nonparabolic corrections to the band structure are found to greatly impact transport modelling [80].

Semiconducting CNTs are proposed to be an ideal material for electronic devices. Ambipolar electrical transport has been reported in single-wall carbon nanotube field-effect transistors [81]. The carbide-nanotube junctions are abrupt and robust. In contrast to planar junctions, these contacts present low resistance for the injection of both p- and n-type carriers. The apparent barrier height of the junction is modified by the gate field. The characteristics taken with a small V_{DS} value as a function of the temperature clearly confirm that the contact barrier is small in both the hole and electron accumulation regimes. Thus semiconducting SWCNTs offer the novel possibility of ambipolar Ohmic contacts.

2.4 Carbon Nanotube Device Models

In the previous section the potential of applying semiconducting CNTs as electronic devices was discussed. The electronic characteristics of semiconducting CNTs imply the possibility of constructing semiconductor devices and circuits using this new type of material. As fundamental electronic components, carbon nanotube diodes and transistors have been studied intensively and novel theories of the physical features of the devices

have been proposed as outlined below.

2.4.1 CNT Diodes

One of the proposed CNT diode structures is based on the metal-semiconducting CNT junction [82] which performs like a Schottky barrier diode. Ineffective screening of the long-range Coulomb interaction in one-dimensional nanotube systems drastically modifies the charge transfer phenomena compared to conventional semiconductor heterostructures [83]. The length of depletion region varies sensitively over a wide range depending on the doping strength. The Schottky barrier gives rise to an asymmetry of the I-V characteristics of heterojunctions, in agreement with recent experimental results by Yao et al. [84] and Fuhrer et al [85]. Dynamic charge buildup near the junction results in a step-like growth of the current at reverse bias.

The performance of a Schottky barrier diode depends on the metal-semiconductor junction feature, which is related to the work function of metals. Electrical contacts to carbon nanotubes typically exhibit high resistance, posing a serious obstacle to their application in electronic devices. To eliminate this problem, J. Tersoff [86] suggested using a metal with a sufficiently large Fermi wave vector (or perhaps a non-armchair tube with reduced Fermi wave vector), by introducing scattering in the CNT, or by contacting the end of the CNT. In addition, the decay of electron wave functions across the van der Waals spacing between metal and CNT may also be an important factor [87].

Several experimental results confirm the operation of the proposed CNT diode model [88, 89, 90]. SWCNT Schottky diodes with titanium Schottky and platinum Ohmic contacts can be fabricated using angled evaporation of dissimilar metal contacts over a semiconducting SWCNT [90]. M. H. Yang et al. [88] demonstrated the fabrication and operation of a CNT Schottky diode by using a Pd contact (high-work-function metal) and an Al contact (low-work-function metal) at the two ends of a single-wall CNT, which shows the possibility of tuning the rectification I-V characteristics of the CNT through the use of a back gate, as illustrated in Figure 2.2.

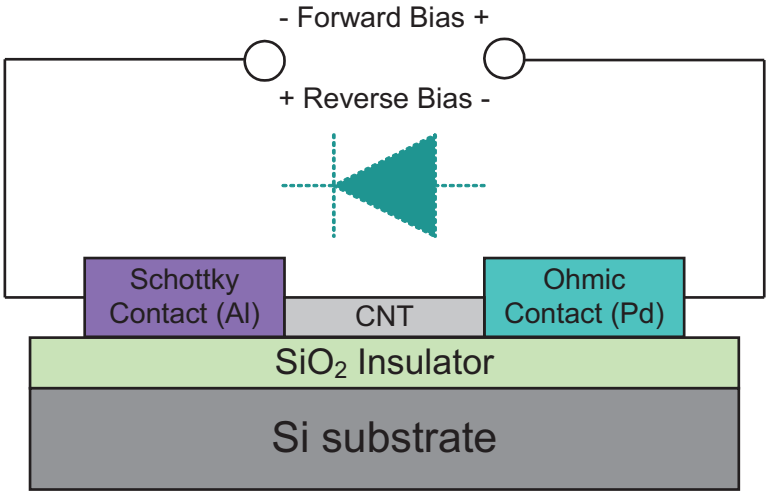

FIGURE 2.2: Carbon nanotube Schottky diode using Al/Pd contacts [88].

Apart from Schottky diodes, CNT p-n junction diodes are also proposed. J. U. Lee et al. [91] formed a structure along a single nanotube by electrostatic doping using a pair of split gate electrodes. By biasing the two gates accordingly, the device can function either as a diode or as an ambipolar field-effect transistor [92]. In 2005, General Electric Company (GE) announced the development of a carbon nanotube diode [93] formed by joining a p-type and an n-type semiconducting material using an electrostatic doping technique using two separate gates that couple to two halves of a single carbon nanotube, which operates at the "theoretical limit" [94], as shown in Figure 2.3.

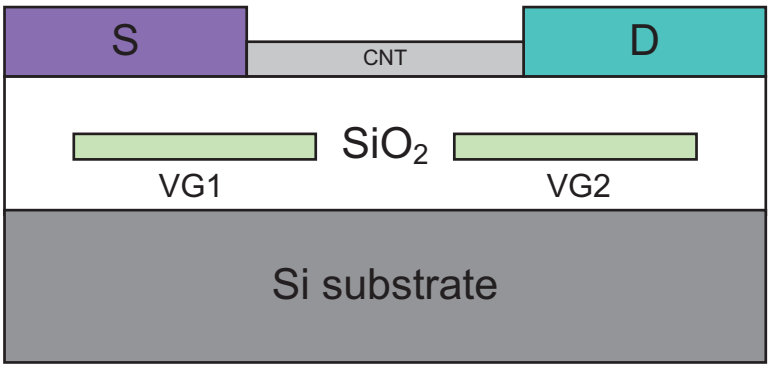

FIGURE 2.3: Schematic cross section of SWCNT p-n junction diode with split gates [91].

2.4.2 Carbon Nanotube Field-Effect Transistors (CNTFETs)

During the past decade, significant progress has been made in understanding the operation of CNTFETs. A large number of models of CNTFETs have been developed both experimentally and theoretically.

When fabricating CNT transistors, the nature of the contacts between nanotubes and metal electrodes is of significant importance. The contact between a metal and a nanotube can either be an end or side contact. In experiments, end contacts usually include strong chemical modification of the nanotube at the metal-nanotube interface. Also, it has been found that end contacts without sufficient chemical modification of the metal-nanotube interface have a large contact resistance [95]. In such a configuration, electrons are injected directly from the metal to the nanotube region between the contacts. Due to the uncertainty of the contact band structure, modelling end contacts is extremely difficult.

Critical to carbon nanotube-based transistors is the problem of constructing a good metal-nanotube contact. Ideally, nanotube-metal devices should have contact resistances in the $k\Omega$ range. In recent investigations low-resistance ohmic contacts have been achieved [96]. One of the main characteristics of the electronic response of the nanotube-metal system is a marked transfer of charge from the nanotube to the metal, which allows the valence band edge of the nanotube to align with the Fermi level of the metal electrode [97]. This charge transfer, which has also been observed for other systems in both experiments [98] and calculations [99], leads to enhanced conductivity along the tube axis and gives rise to a weak ionic bonding between the tube and the metal.

Contacting metallic single-walled carbon nanotubes using palladium (Pd) affords highly reproducible ohmic contacts and allows ballistic transport in nanotubes. The Pd ohmic contacts are more reliable than titanium (Ti) for ballistic CNT devices. In contrast, platinum (Pt) contacts provide non-ohmic contacts to metallic CNTs. For both ohmic and non-ohmic contacts, the length of the nanotube under the metal contact area is electrically turned off. Transport occurs from metal to nanotube at the edges of the

contacts. Measurements with large numbers of Pd contacted nanotube samples reveal that the mean free path for defect scattering in SWCNTs grown by chemical vapor deposition can be up to 4um. The mean free paths for acoustic phonon scattering are on the order of 500 nm at room temperature and more than $4\mu m$ at low temperatures [17].

Most proposed structures consist of a CNT channel and metal terminals as gate, source and drain [100], and the contacts may influence the performance of the devices. Reports have presented that the formation of ohmic contact between individual SWCNT and Pd electrode was achieved by applying the pulsed voltage of several volts for microseconds in the Pd electrode [101].

Novel high-κ materials make it practical to model nano-scale transistors, which promises to push the performance limit for molecular electronics. SWCNT transistors with integrated ZrO_2 high-κ dielectrics have been reported [102]. Additionally, high performance enhancement mode CNT transistors have been obtained using high-κ HfO_2 films as gate insulators [103, 104], in which excellent OFF states to nanotube FETs under aggressive vertical scaling can be derived. Polymer electrolytes have also been demonstrated as gate media to construct CNT transistors showing high on-state conductance, carrier mobilities and on-off ratios [105].

As an alternative to exploiting new material, researchers have demonstrated that gate structure is related to performance. Different from conventional top-gated transistors [106, 107], back-gated [97, 108] and dual-gated CNTFETs [109] have recently been proposed. It has also been revealed that the overlaps between gate, drain and source may considerably affect the transport situation. A dual-gate CNTFET, with a pair of metallic SWCNT bundles as the top gates and a heavily doped silicon substrate as its back gate, has been systematically studied [110]. Through adjusting the electrostatic potential of the channel by tuning the back gate and SWCNT top gate voltages, single-electron and single-hole charging with the Coulomb blockade effect are clearly observed at 100K or below.

The prospect of realising nanoscale transistors using individual semiconducting carbon nanotubes offers potential as an alternative to silicon technology beyond conventional

scaling limits. A significant challenge is the realisation of low-voltage nanotube transistors with individually addressable gate electrodes that display large transconductance, steep subthreshold swing, and large on/off ratio [111]. Their integration into circuits with large signal gain and good stability still needs to be demonstrated. It has recently been demonstrated [111] that these important goals can be achieved with the help of a bottom-gate device structure that combines patterned metal gates with a thin gate dielectric based on a molecular self-assembled monolayer. The obtained transistors operate with a gate-source voltage of $1V$ and have a transconductance of $5\mu S$, a subthreshold swing of $68mV/decade$, and an on/off ratio of 10^7. It has also been verified that the device structure can be applied to implement unipolar logic circuits with good switching performance [111].

The work of M. Pourfath et al. [112, 113] shows that, by carefully choosing the gate-source and gate-drain layouts, both the static and dynamic response of ohmic contact CNTFETs can be improved. However, device geometry is not applicable to conventional MOSFETs, since the mechanisms in controlling the flow current are different. As for the capacitances of CNTFETs, researchers have focused on the electrostatic capacitance [114, 115] and the quantum capacitance [116]. It has been suggested by Sayed Hasan et al. [117] that at high frequencies the quantum capacitance will dominate and the gate bias may also exert significant effects on the performance of the transistor.

One important metric that determines transistor performance is the current of the device at ON state I_{on}. For Schottky barrier CNT transistors, a wide range of ON-currents between $10^{-5}A$ and $10^{-9}A$ have been reported by different groups for devices with various nanotube diameters and contact metals. This ON-current is dependent on the SB height Φ_{SB-h} for hole carriers at the nanotube/metal interface, i.e. the line-up of the metal Fermi level and the valence band of the nanotube. By comparing the diameter and I_{on} distribution of devices for each contact metal, the diameter dependence of I_{on} of Pd-, Ti-, Al-contacted CNT transistors are summarised [18]. For any nanotube diameter, Pd-contacted CNT transistors deliver the largest I_{on} while Al-contacted devices have the smallest I_{on}. This is because Pd has the highest work function, which forms a small Φ_{SB-h} to the valence band of the nanotube. Since the nanotube band gap E_G is

inversely proportional to the nanotube diameter, a smaller Φ_{SB-h} is achieved for a larger diameter nanotube, leading to a monotonic increase of I_{on} with increasing nanotube diameter. One important trend observed in experiments is that I_{on} exhibits a stronger diameter dependence for small nanotubes than for large diameter nanotubes [18].

K. S. Kim et al. [118] investigated a modification of electronic structures of a carbon nanotube by exposing carbon nanotubes to atomic hydrogen which was generated by a hot tungsten filament in the vacuum chamber, and the results predicted a strong chemisorption with the band gap widening upon hydrogenation.

Single-hole CNT transistors operating at room temperature were recently derived [119]. To obtain large charging energy, a 25nm-long CNT channel was formed via evaporation to achieve small gate capacitance and an insulator was inserted between the CNT channel and electrodes to minimise tunnel capacitances. A small gate capacitance ($\sim 0.06aF$) and a small tunnel capacitance ($\sim 0.3aF$) were obtained, which are much smaller than those of conventional MOSFETs. Drain current oscillation as a function of gate voltage was obtained for the device without insulator. These results imply that the small tunnel capacitance is of importance for single-charge CNT transistors working at room temperature.

By taking advantage of silicon-on-insulator technology and in situ CNT growth, new local silicon-gate CNTFETs have been implemented [120]. An approach to integrating the CNTFET onto the silicon MOS platform has been proposed. Individual device operation, batch fabrication, low parasitic capacitance, and better compatibility with the CMOS process were realised. The scaling effect, Schottky barrier effect, and ambipolar conductance of the proposed transistor were analysed.

Efforts have been made on growing carbon nanotube as channel using position controlling under certain conditions [121]. With appropriate temperature in CH_4 environment, single electron transistors can be fabricated by controlling the position of the CNT using the patterned chemical catalyst. By using the CNT as a device element, an electron device with the feature size of 1-2nm could be easily fulfilled using only the conventional photolithography process [121].

2.5 Existing Carbon Nanotube Transistor Models

Circuit-level CNT transistor models have recently emerged to describe the macroscopical characteristics of CNTFETs [122, 123]. Researchers at Stanford University [9] have implemented a circuit-compatible SPICE model for enhancement mode CNTFET with real time dynamic response. Anisur Rahman et al. at Purdue University [16] set up a MATLAB model which helps to derive the performance of CNTFETs such as the I-V relationship.

An equivalent circuit model of a ballistic one-dimension CNTFET has been introduced for circuit simulation, as illustrated in Figure 2.4 [124]. This model indicates the relationships between device characteristics and applied terminal voltages, such as I-V characteristics. For small bias conditions, the performance of this model matches closely that of the physical model. However, this model only employs basic ballistic approximation and when the bias is large its performance will degrade significantly. Another circuit compatible model is shown in Figure 2.5 [9]. It brings in the gate-substrate coupling capacitance C_{GB}, three trans-capacitance pairs, the small magnetic inductance L_{MS} and the large quantum inductance L_{KS} which affects high frequency performance. This model suggests that, in the light of both fabrication availability and device characteristics, enhancement mode CNTFETs should be appropriate for circuit applications.

The density of states and band structure of CNTs has also been investigated by researchers. Finite integrations [125], Newton-Raphson iteration approach [11, 126] and non-equilibrium Green's function [127] are employed in recent reports. It has been illustrated that the energy band of CNTFETs is to some extent dependent on external terminal voltages. Currently, researchers are working on simplifying the numerical calculation of the channel current of CNT transistors [11, 126].

Recently, analytical modelling equations describing the current transport in carbon nanotube field effect transistors have been developed from physical electronics, which have strong dependence on the chiral vector and device geometries [128]. The solution of these model equations for the CNTFETs has been compared with available experimental data and then used to generate voltage transfer characteristics of basic logic devices based on

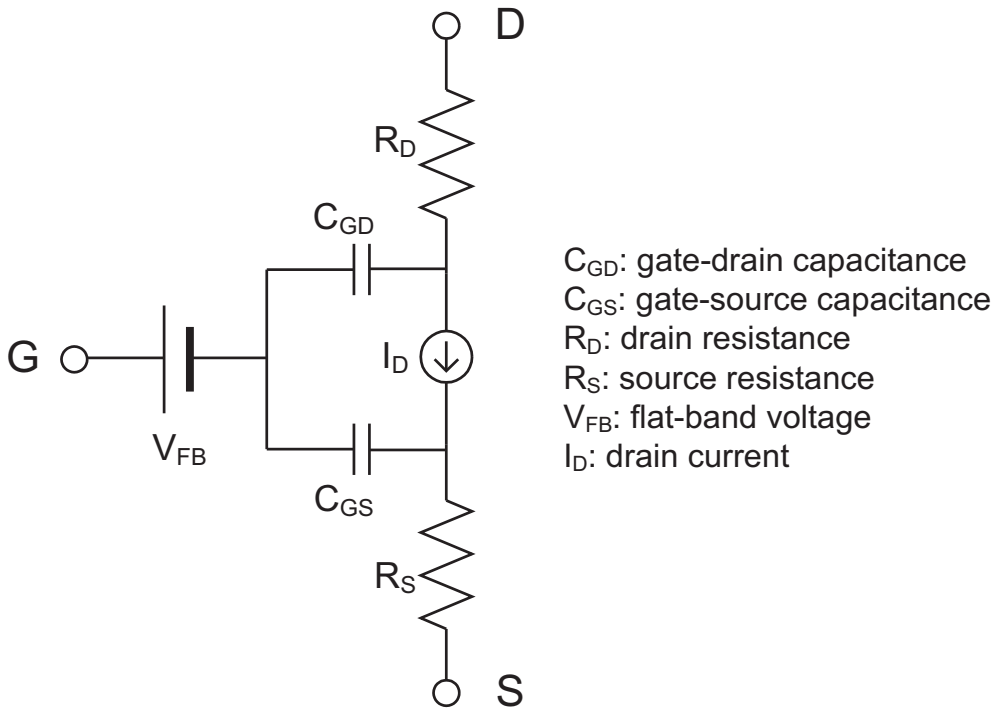

FIGURE 2.4: A MOS-like model of CNT transistor [124].

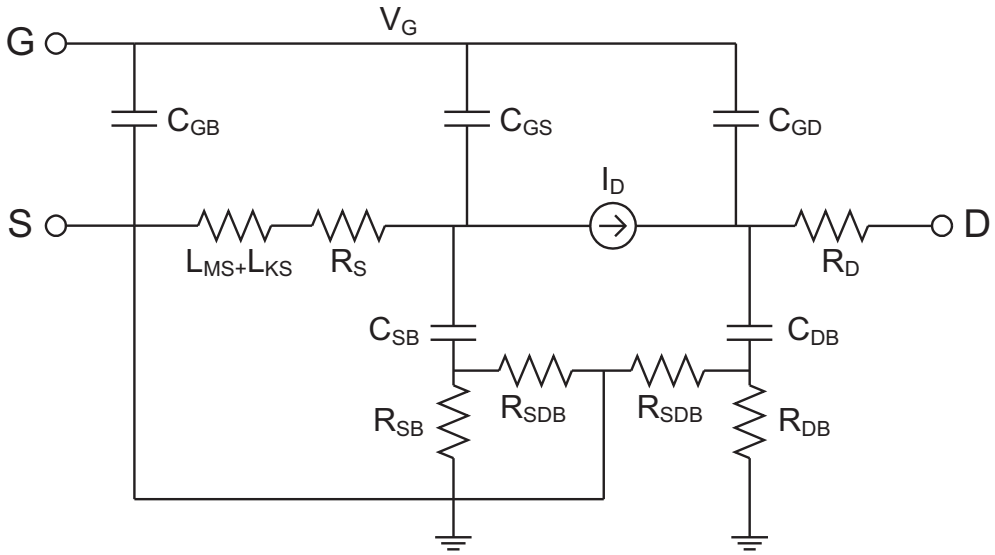

FIGURE 2.5: One circuit compatible model of CNT transistor [9].

complementary CNTFETs. The voltage transfer characteristics exhibit characteristics similar to the voltage transfer characteristics of standard CMOS logic devices. A novel modelling approach that has recently emerged can predict the characteristics of a CNT transistor with a number of parameters, including diameter, chirality, gate dielectrics, and terminal bias voltages [129]. J. Appenzeller et al. [130] compared three possible

models, Schottky barrier-, conventional- and tunnelling-CNTFETs, and they suggested that the tunnelling-CNTFET can be beneficial for overall device performance in terms of switching speed and power consumption. Furthermore, a compact analytical model for the I-V characteristics of tunnel current in a Schottky barrier CNTFET which features the main physical effects governing the operation of this device has recently been developed [131].

Recent studies have shown interest in eliminating the effects of metallic CNTs from modelling semiconducting CNT devices [132, 133]. A technique based on the physical design of CNT devices demonstrates that single metallic CNT defects can be modelled and detected by a single stuck-at fault method [132]. A mathematical algorithm using both the diameter and chirality angle of the CNTs has also been demonstrated to be effective in distinguishing metallic and semiconducting CNTs [133]. Temperature is another critical parameter in CNTFET modelling, for the energy band will be different if the temperature changes [134]. The density of carriers within the channel can also be tuned by temperature [135].

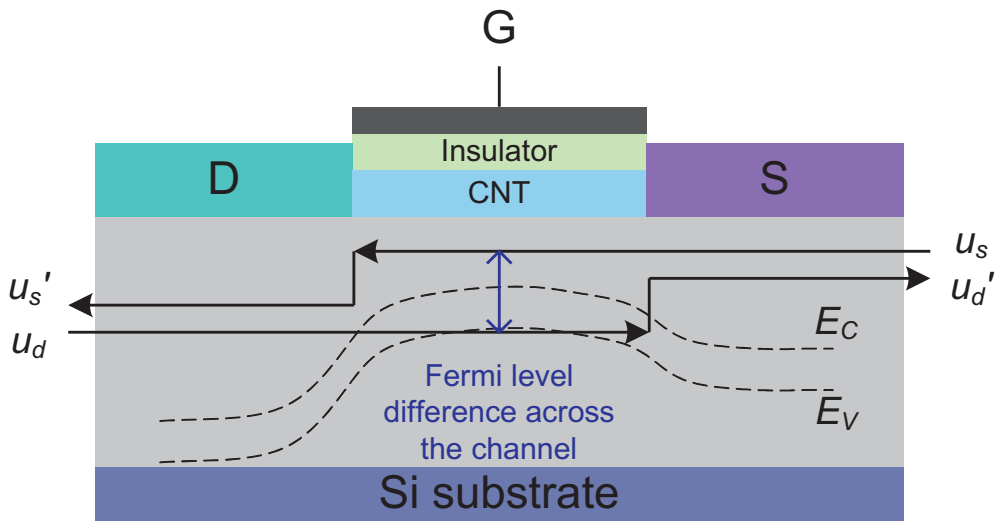

FIGURE 2.6: Ideal CNTFET with ballistic channel. Superposed are the Fermi level profiles (solid arrows) from source to drain and the energy band diagram (dashed lines) with bias V_{DS}. All the node potentials are referred to the input source Fermi level [13].

Recently, research on non-ballistic transport in CNT transistors has emerged. A circuit-compatible compact model of the intrinsic channel region of MOSFET-like SW-CNTFETs including some channel region non-idealities has been developed [13, 14, 136]. The Fermi level profiles and the energy-band diagram in the channel region with a ballistic trans-

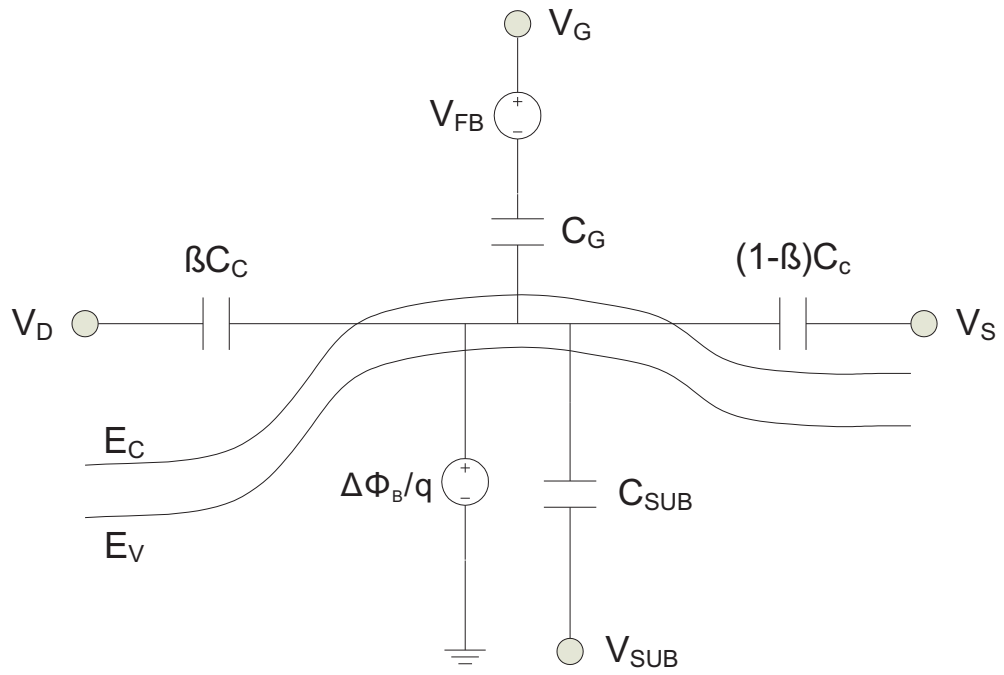

FIGURE 2.7: Electrostatic capacitor model used to calculate the channel surface-potential change before and after gate/source/drain/substrate bias. All the node potentials are referred to the input source Fermi level. C_C and β are fitting parameters [13].

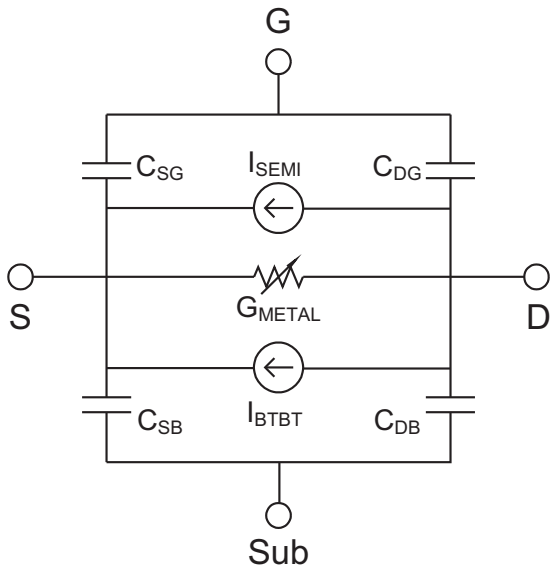

FIGURE 2.8: Equivalent circuit model for the intrinsic channel region of CNTFET [13].

port are shown in Figures 2.6 and 2.7 [13]. An analytical model to calculate the gate capacitance of the device with high-κ gate dielectric material and multiple cylindrical conducting channels including the screening effect has also been developed [137]. This model is valid for CNTFETs with a wide range of chiralities and diameters, which makes

the proposed modelling methodology generally applicable to other 1-D devices [13]. The equivalent circuit model for the intrinsic channel region of the proposed CNTFET model is illustrated in Figure 2.8. Furthermore, a universal model including some device non-idealities is proposed [14]. The performance of this model is compared with that of the proposed CNT transistor models of this research in Chapter 6.

2.6 Theoretical Ballistic CNT Transistor Model

Another ballistic nanotransistor model concentrates on two-dimensional electrostatic effects and self-consistent potential [12]. This model demonstrates that the self-consistent potential at the gate region determines the transport status of carriers in CNTFET. Figure 2.9 illustrates the relationship between the states at the top of the gate barrier and the $\overrightarrow{k}$ vector within a simple band structure. The positive velocity states are populated according to the Fermi level of the source and the negative velocity states by the Fermi level of the drain.

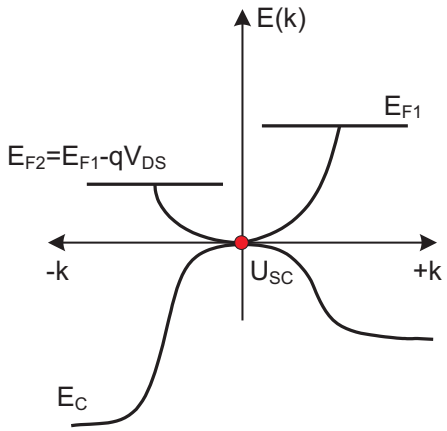

FIGURE 2.9: The k-states at the top of the energy barrier [12].

The proposed theoretical ballistic CNT transistor model [12] is based on two transport features that provide mathematical information on its operation. One is the non-equilibrium Green's function (NEGF) formalism for quantum transport [20], and the other one is the numerical solution of the Boltzmann equation [19]. A 2-D model for the ballistic MOSFET is shown in Figure 2.10 [12]. It consists of four capacitors, which represent the effect of the four terminals on the potential at the top of the barrier. As

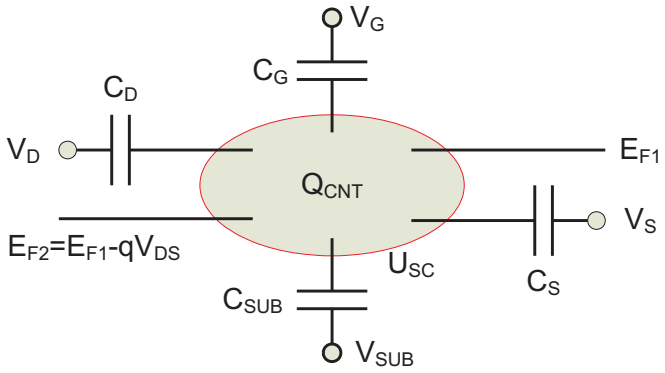

FIGURE 2.10: Two-dimensional model for ballistic CNT transistors [12].

indicated by the shaded region in Figure 2.10, a mobile charge can be placed at the top of the barrier. The mobile charge is determined by the local density of states at the top of the barrier, the location of the source and drain Fermi levels E_{F1} and E_{F2}, and by the self-consistent potential at the top of the barrier U_{SC} [20].

When an electric field is applied between the drain and the source of a CNT transistor, a non-equilibrium mobile charge is induced in the nanotube [12, 21, 22]. V_{SC} is the self-consistent voltage, a recently introduced concept [12] which illustrates that the CNT energy band is affected by external terminal voltages. The self-consistent voltage V_{SC} is implicitly related to the device terminal voltages and charges at terminal capacitances as shown in the following non-linear algebraic equation [11, 12]:

$$V_{SC} = \frac{-Q_t + qN_S(V_{SC}) + qN_D(V_{SC}) - qN_0}{C_\Sigma} \tag{2.1}$$

where Q_t represents the charge stored in terminal capacitances, q is the electronic charge, N_S is the density of positive charges filled by the source, N_D is the density of negative charges filled by the drain, N_0 is the equilibrium electron density, and C_Σ represents the total terminal capacitance of the CNT transistor. The conventional approach to the solution of Eq. 2.1 is to use the Newton-Raphson iterative method and in each iteration obtain the state densities N_S and N_D. Based on theoretical equations, this method can represent the accurate ballistic transport characteristics of a CNT transistor. However, the iterative calculation limits the speed of the modelling process and thus affects the efficiency of this approach. As a reference theoretical model, the algorithm of FETToy

will be discussed in Section 3.1.2. The performance of FETToy [16] will also be compared with that of models developed in this research in Chapters 3 and 4.

2.7 CNT Transistor Model Based on Symbolic Approximation of Charge Densities

Though the theoretical modelling approach introduced in Section 2.6 can accurately describe the ballistic transport property of ideal CNT transistors, the Newton-Raphson iteration in the equation is time-consuming and affects modelling efficiency. To derive faster modelling approaches without sacrificing much accuracy, models based on the approximation of the mobile charge density of CNT transistors, including numerical and symbolic ones, which can replace the iterative calculation with faster algorithms, have been proposed.

Recently a symbolic piece-wise linear approximation for mobile charge densities of CNTFETs in the ballistic regime has been presented [11]. This approach permits a fast and accurate calculation of the charge densities and self-consistent voltage as well as the source-drain current of the CNTFET [23]. The proposed symbolic model presents a closed-form solution of the self-consistent voltage in a CNTFET as a function of parameters including temperature, device terminal voltages, Fermi level, and CNT diameter.

This model is based on the mathematical piece-wise linear approximation of the source and drain charge densities. This process involves finding one point and the slope of three line pieces for each charge density [126]. They obtain the slopes by first differentiating the charge density curves and then calculating the limits using L'Hopital's rule. The simplified results of source and drain mobile charge densities can be presented using the following equations (Eq. 2.2 and Eq. 2.3):

$$N_S(U_{SCF}) \approx \begin{cases} m_1^2 U_{SCF} + n_1^2, & \text{if } U_{SCF} \leq E_F + 2k_B T ln(\varepsilon) \\ m_1^1 U_{SCF} + n_1^1, & \text{if } E_F + 2k_B T ln(\varepsilon) < U_{SCF} \leq -\frac{n_1^1}{m_1^1} \\ 0, & \text{if } U_{SCF} > -\frac{n_1^1}{m_1^1} \end{cases} \tag{2.2}$$

$$N_D(U_{SCF}) \approx \begin{cases} m_2^2 U_{SCF} + n_2^2, & \text{if } U_{SCF} \leq E_F - qV_{DS} + 2k_B T ln(\varepsilon) \\ m_2^1 U_{SCF} + n_2^1, & \text{if } E_F - qV_{DS} + 2k_B T ln(\varepsilon) < U_{SCF} \leq -\frac{n_2^1}{m_2^1} \\ 0, & \text{if } U_{SCF} > -\frac{n_2^1}{m_2^1} \end{cases} \tag{2.3}$$

where N_S and N_D refer to the charge densities at source and drain respectively. The coefficients m_1^1, m_1^2, n_1^2, n_1^2, m_2^1, m_2^2, n_2^1 and n_2^2 can be derived from the parameters given for the CNT transistor model. Thus a full characterisation of the source and drain charge densities shown in Equations 2.2 and 2.3 using the piece-wise linear approximation have been obtained. The calculation is straightforward and does not require a numerical integration method or curve fitting for charge densities. Moreover, the model is symbolic, which implies that it can readily incorporate any change in the parameter values in the charge densities.

The proposed symbolic model, using linear approximation of charge densities of ballistic CNT transistors, brings in mathematical simplification to eliminate the iterative process of the calculation of self-consistent potential, which significantly saves computing time and raises modelling efficiency. However, the symbolic model is not accurate enough and the introduced coefficients require some estimations, which may affect the performance of the model.

2.8 Logic Circuits Based on CNTs

The topic of composing logic gates using CNT transistors has attracted interest from researchers [10, 138, 139]. Circuits that exhibit a range of digital logic circuits including logic inverters, NOR and NAND gates, a static random-access memory cell, and multi-valued logic gates have recently been demonstrated [138]. The shift of the flat band potential makes it possible to employ CNT transistors in logic gates [139]. In this section some CNT transistor based logic circuits are described.

Inverters

Research from IBM has introduced a simple process involving the annealing in vacuum of a p-type CNTFET to convert it to an n-type CNTFET. This conversion is reversible, and re-exposure to oxygen leads to a p-type CNTFET [10]. Having complementary CNTFETs allows the building of logic gates, for example, an inverter. IBM recently fabricated a logic inverter which was implemented by bonding together two CNTFETs stable in air [140]. An offset voltage (V_{shift}) between the isolated transistor back-gates allows adjustment of the threshold of the n- and p-type CNTFET characteristics and the inversion performance is optimised.

NAND and NOR Gates

In recent work, high-performance back-gated p-type and n-type CNT transistors based on transferred aligned carbon nanotubes were fabricated [141]. These transistors were further utilised to demonstrate various logic gates, including complementary metal-oxide-CNT NAND and NOR gates. Both of them employ a $20M\Omega$ resistive load in the pull-down network, while two p-type aligned nanotube transistors are connected using external wires to serve as the pull-up network. The value of the resistive load is chosen between the on-state resistance and the off-state resistance of the transistors. The NAND and NOR circuits are both operated with a supply voltage of $1V$.

Memory Cells

Recently, a flip-flop memory element that was constructed from two inverters was implemented [138]. When the output of each inverter is connected to the input of the other inverter, two different stable states are possible: the outputs can take on the values (1,0) or (0,1). A logical 1 is written into memory by forcing the circuit into the (0,1) state and a logical 0 is written by forcing the circuit into the (1,0) state. Tests have been made to demonstrate the stable memory function of this duo-CNT-transistor memory unit. The electrical characteristics of Carbon Nanotube Field Effect Transistor SRAMs have also been investigated [142]. Research shows that in 32nm technology node CNTFET

SRAM spends much less standby power and is more stable in read operation as compared with its Si-MOSFET SRAM counterpart. However, write Static Noise Margin (SNM) in CNTFET SRAM is very low so two SRAM designs based on backgate voltage and diameters of CNTFET have been proposed to improve write SNM in CNTFET SRAMs. This research also demonstrates that access time for a 128 column-256 row SRAM array based on CNTFET is improved over its Si-MOSFET counterpart.

Multi-Valued Logic Gates

Recently, a multi-valued logic in a single quantum well has been proposed [143]. There are three dominant parameters for implementing various levels of logic units: the well width (via the width of the inner gate electrode), the barrier height (via the tunable gate voltage), and the Fermi energy level (via doping). A novel technique for multiple-valued logic gate design using CNT transistors has been developed [144, 145, 146]. This methodology is based on the feature that CNTFETs provide an opportunity to obtain two distinct threshold voltages (V_T) by using a pair of CNTs with different tube diameters. Any other technique that allows usage of two reliable threshold voltages can also be used for realising logic cells. The geometry-dependent threshold voltage of CNTFETs has been effectively used to design a ternary logic family. Figure 2.11 shows the structure of the multiple-valued logic unit. This figure illustrates that with different diameters (or other parameters), the conduction status of CNT transistors may vary, which can be applied in multi-valued logic circuits. The working status of this unit is briefly shown in Figure 2.12. When the input voltage increases, the two CNT transistors turn on successively at their own threshold voltages, leading to a step-shaped output.

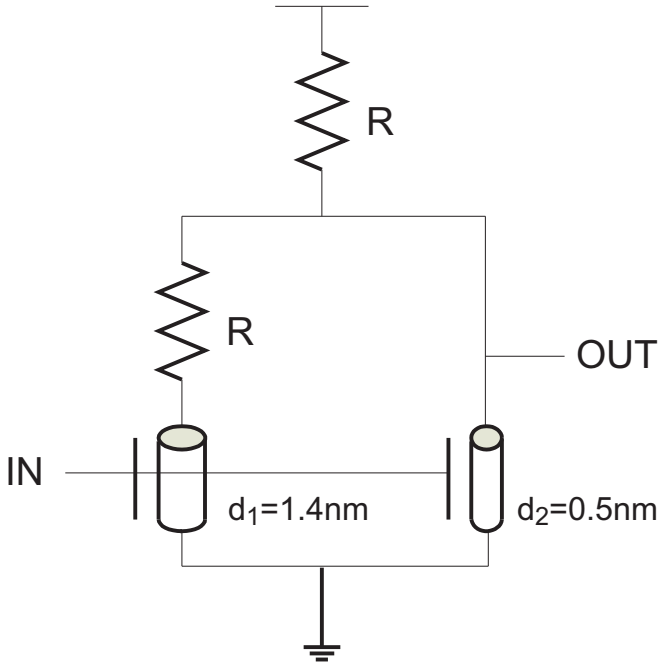

FIGURE 2.11: Schematic of a multi-valued logic gate [138].

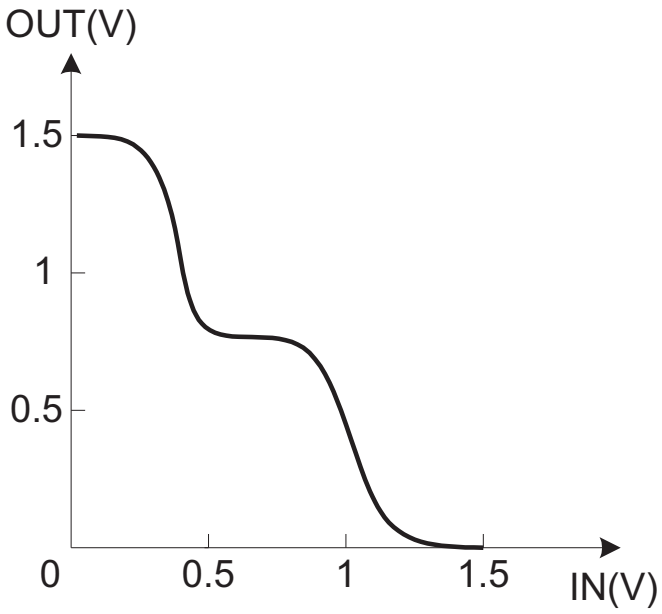

FIGURE 2.12: Performance of the multi-valued invertor gate [138].

2.9 Variation Analysis for CNT Transistors

It has been demonstrated that parameter variation can affect the performance of CNT transistor models [26, 27]. Recent research has shown that disorder in the orientation of the nanotube may change the transport characteristics of the device [147]. With

different chiralities, the resistance of CNTs may vary within a range from as small as about $6k\Omega$ to several megaohms [65], which will cause failure to CNT based devices.

It has also been reported that diameter variation may widen or narrow the band gap of CNTs and thus change the transport strength of the nanotube [148]. Considering that current fabrication techniques face difficulties in controlling the CNT diameter, diameter variation is widespread and its effect on the transport characteristics of CNTs should be analysed in CNT device modelling. Recent experiments also show that temperature variation leads to band gap diversity and therefore affects the transport property of CNT transistors [149].

Additionally, Fermi level variation caused by defects, vacancies and charged impurities has also been examined in altering nanotube transistor characteristics [150]. The threshold voltage of a CNT transistor may shift as the Fermi level changes. A single vacancy can cause drive current reduction by approximately 28%, independent of the location of the vacancy in the channel, for the device considered. While a single negatively charged impurity near the channel also decreases the drive current by a similar amount, it leads to a much larger threshold voltage shift, comparable to $40mV$, 10% of the power supply.

2.10 Concluding Remarks

This chapter has provided a literature review of the research in carbon nanotube device characterisation, fabrication, modelling and simulation. Firstly, considerable understanding of the physical properties of CNTs was gained. Through the surveyed literature on the transport characteristics of CNTs, it was proposed that semiconducting carbon nanotubes have the potential of working as high-performance active electronic devices. Furthermore, progress has been made in CNT device modelling. Both numerical and symbolic modelling techniques have been developed to describe the ballistic transport characteristics of CNT transistors, while CNT based devices have been implemented in experiments. Also, CNT logic circuits including inverters, NOR and NAND gates, SRAM, and multi-valued logic gates have been developed and their performance were compared with that of MOS devices. These results look encouraging and merit further

research. However, through the summary of carbon nanotube device modelling efforts, this chapter has also revealed the strengths and weaknesses of current CNT device modelling techniques and identified the need for further development of them. All reported modelling techniques suffer from high CPU time consumption and lack of analysis of non-ballistic CNT transport characteristics. These form the foundations for Chapters 3, 4 and 5. Additionally, numerical or symbolic models are not suitable for circuit-level simulation. This aspect is addressed in Chapter 6, in which the implementation of SPICE-compatible CNT transistor models and CNT based logic circuits is described.

Chapter 3

Ballistic CNT Transistor Model Based on Piece-Wise Approximation

This chapter presents a numerical technique to efficiently analyse the ballistic transport characteristics of CNT transistors. As outlined in Section 2.6, Chapter 2, significant progress has been made in the development of CNT transistor modelling techniques. However, new and more efficient models are required, since some of the currently proposed CNT transistor models suffer from significant numerical complexities. This includes models that rely on numerical evaluation of integrals or internal Newton-Raphson iterations to find solutions of non-linear dependencies or both [9, 12]. This chapter introduces a technique which eliminates the need for costly Newton-Raphson iterations and numerical integration when calculating the charge densities of CNT transistor characteristics through the use of piece-wise approximation. This technique is based on the effective employment of linear and polynomial approximation of the charge densities to accelerate simulation speed when evaluating the source-drain current of CNT transistors.

This chapter is organised as follows. Section 3.1 presents the theoretical analysis of ballistic CNT transport and explains the complexity of solving the non-linear source-drain current equation. Section 3.2 describes the implementation of a model that uses

a piece-wise linear approximation to mathematically simplify the solution of the non-linear equation, while Section 3.3 proposes an alternative model based on quadratic approximation of mobile charge density which can obtain higher simulation accuracy than the linear approximation based model. Finally, Section 3.4 gives conclusions from this work.

3.1 Numerical Analysis of Ballistic Transport Characteristics of CNT Transistors

Theoretical analysis of transport characteristics of CNT transistors has been the focus of many published papers [12, 21, 22, 97, 106, 107, 108]. Models and software tools like FETToy [16] have been developed. Equations numerically describing the general transport mechanism of CNTs have also been derived from the physical properties of CNTs. The following section explains the theories supporting existing techniques of CNT transistor modelling and introduces the motivation behind this work to develop numerically efficient CNT transistor models.

3.1.1 Non-Equilibrium Mobile Charge of CNT Transistors

Existing theories [12, 21, 22] suggest that when an electric field is applied between the drain and the source of a CNT transistor, a non-equilibrium mobile charge is induced in the carbon nanotube channel:

$$\Delta Q = q(N_S + N_D - N_0) \tag{3.1}$$

where N_S is the density of positive charges filled by the source, N_D is the density of negative charges filled by the drain and N_0 is the equilibrium charge density. These densities are determined by the Fermi-Dirac probability distribution as shown in Equations 3.2, 3.3 and 3.4:

$$N_S = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E - U_{SF})dE \tag{3.2}$$

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E - U_{DF})dE \tag{3.3}$$

$$N_0 = \int_{-\infty}^{+\infty} D(E)f(E - E_F)dE \tag{3.4}$$

where $D(E)$ represents the density of states (DoS) contributed by the lowest subband of a CNT, E_F is the Fermi level, f is the Fermi probability distribution, q is the electronic charge, E represents the energy levels per nanotube unit length, while U_{SF} and U_{DF} are source and drain potentials related to the Fermi level and terminal voltages (V_D, V_S and V_G). It can be seen from Equations 3.2 - 3.4 that N_S and N_D are determined by the potential levels at the source and the drain, while N_0 is related to the Fermi level of CNTs and independent of terminal voltages. As the diameter of a nanotube is within the nanometer range and is much smaller than its length, generally a CNT is treated as a one-dimensional nanowire. The one-dimensional density of states for the semiconducting band of CNT is shown in Eq. 3.5 [11]:

$$D(E) = D_0 \frac{|E|}{\sqrt{E^2 - (E_G/2)^2}} \Theta(|E| - E_G/2) \tag{3.5}$$

where $D_0 = \frac{8}{3\pi a_{cc} V_{cc}}$ is the constant metallic band DoS of CNTs, $\Theta(x)$ is the step function which equals 1 for x $>$ 0 and 0 otherwise, and E_G is the band gap of the CNT which can be represented using Eq. 3.6:

$$E_G = \frac{2a_{cc}\,|V_{cc}|}{d} \tag{3.6}$$

where $a_{cc} \approx 1.44\overset{o}{A}$ is the nearest neighbour C-C bonding distance and $V_{cc} \approx -3.0eV$ is the neighbour C-C bonding energy [12].

For the purpose of modelling an equivalent circuit of the CNT transistor, equal parts of

the equilibrium mobile charge density N_0 are proposed to apportion to the drain and source, and the corresponding non-equilibrium mobile charges Q_S (Eq. 3.7) and Q_D (Eq. 3.8) are introduced as follows.

$$Q_S = q\left(N_S - \frac{1}{2}N_0\right) \tag{3.7}$$

$$Q_D = q\left(N_D - \frac{1}{2}N_0\right) \tag{3.8}$$

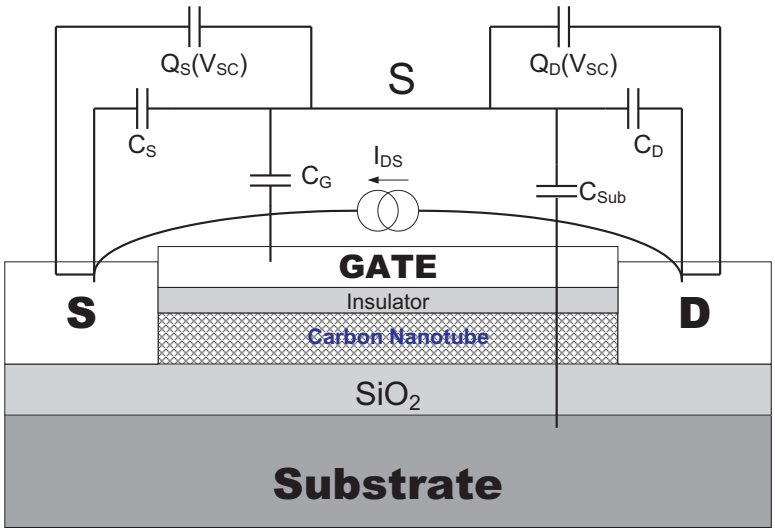

FIGURE 3.1: Schematic of a top-gated CNT transistor showing its equivalent circuit.

Figure 3.1 shows the schematic of a top-gated CNT transistor model. In the schematic, C_G, C_S, C_D and C_{Sub} represent the capacitances between the CNT channel and the gate, the source, the drain and the substrate of the transistor respectively. Since the non-equilibrium mobile charges are induced by terminal voltages, here Q_S and Q_D are introduced in the form of a pair of capacitors, which implies the relationship between the mobile charge and the voltage. Furthermore, the ballistic source-drain current is treated as a DC current source I_{DS}.

The existence of non-equilibrium charges determines that the transport mechanism of CNTs is different from that of traditional semiconductor materials like silicon. The remainder of this section will numerically analyse the relation between non-equilibrium charges and supply voltages and finally describe the algorithm to calculate the current

within the CNT channel.

3.1.2 Self-Consistent Voltage

U_{SF} and U_{DF} mentioned above in Equations 3.2 and 3.3 are potentials induced by terminal voltages at the source and drain of the CNT transistor, which are defined in Eq. 3.9 and Eq. 3.10 respectively:

$$U_{SF} = E_F - qV_{SC} \tag{3.9}$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS} \tag{3.10}$$

where V_{SC} is the self-consistent voltage, a recently introduced concept [12] which illustrates that the mobile charge potential of CNT transistors can be tuned by terminal voltages.

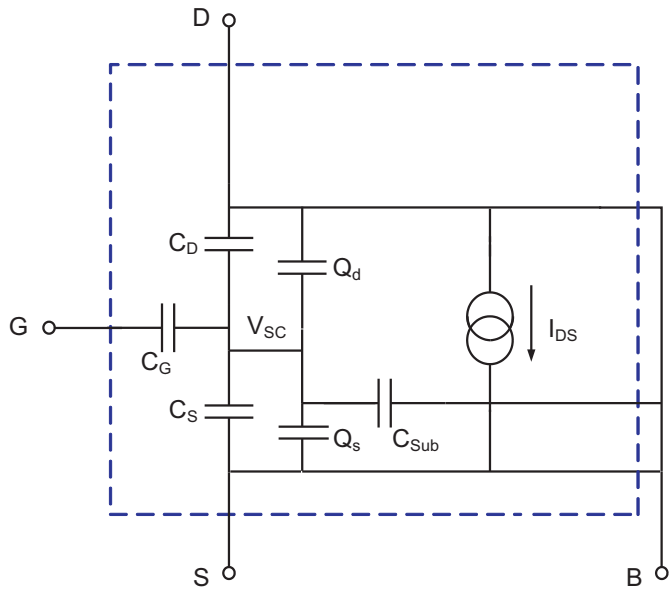

FIGURE 3.2: Equivalent circuit of the proposed CNT transistor model

To clarify the concept of V_{SC}, an equivalent circuit of a CNT transistor is shown in Figure 3.2. The figure illustrates that the self-consistent voltage locates at a hypothetical point within the channel which combines all the CNT terminal capacitances (C_G, C_S, C_D and

C_{Sub}) and potentials (Q_S and Q_D) induced from the source and the drain. Therefore, the self-consistent voltage V_{SC} is implicitly related to the device terminal voltages and charges at terminal capacitances, which is represented by Eq. 3.11 [11, 12]:

$$V_{SC} = \frac{-Q_t + Q_S + Q_D}{C_\Sigma} \tag{3.11}$$

where Q_t represents the charge stored in terminal capacitances and is defined in Eq. 3.12:

$$Q_t = V_G C_G + V_D C_D + V_S C_S \tag{3.12}$$

where C_G, C_D, C_S are the gate, drain, and source capacitances correspondingly and the total terminal capacitance C_Σ is represented by Eq. 3.13.

$$C_\Sigma = C_G + C_D + C_S \tag{3.13}$$

According to Equations 3.2, 3.3, 3.7, 3.8, 3.9 and 3.10, Q_S and Q_D can be described as functions of V_{SC}. Regarding this, Eq. 3.11 can be transformed into Eq. 3.14 which forms a non-linear algebraic equation of V_{SC}.

$$V_{SC} = \frac{-Q_t + qN_S(V_{SC}) + qN_D(V_{SC}) - qN_0}{C_\Sigma} \tag{3.14}$$

According to the ballistic CNT transport theory [12, 16], the drain current induced by the transport of the non-equilibrium charge across the nanotube can be calculated using the Fermi-Dirac statistics represented by Eq. 3.15:

$$I_{DS} = \frac{2qkT}{\pi\hbar}\left[\mathcal{F}_0(\frac{U_{SF}}{kT}) - \mathcal{F}_0(\frac{U_{DF}}{kT})\right] \tag{3.15}$$

where $\mathcal{F}_0$ represents the Fermi-Dirac integral of order 0, k is Boltzmann's constant, T is the temperature and $\hbar$ is reduced Planck's constant.

If the self-consistent voltage V_{SC} is known, the evaluation of the drain current poses no numerical difficulty since energy levels U_{SF}, U_{DF} can be found instantly from Equations 3.9 and 3.10 respectively, while I_{DS} is calculated directly using the closed-form analytical solution of the Fermi-Dirac integral of order 0 (Eq. 3.16) [151].

$$\mathcal{F}_0(\eta) = log(1 + e^{\eta}) \tag{3.16}$$

Algorithm 3.1: Implementation of the numerical FETToy model

Input: terminal voltages V_G,V_D,V_S, Fermi level E_F, CNT diameter d, and Temperature T

Output: drain current I_{DS}

```
set constants and compute V_SC related parameters;
for vg = 0 : +0.1 : V_G do
    i = 0, which is the index of output current value as V_DS sweeps;
    I_DS = 0;
    V_DS = V_D − V_S;
    for vd = 0 : 0.01 : V_DS do
        apply Newton-Raphson method to iteratively solve Eq. 3.14 and derive the
        value of V_SC;
        compute the drain current I from the I − V_SC relationship using Eq. 3.15;
        i = i + 1;
        I_DS(i) = I;
    end
end
return I_DS;
```

Based on the theory given above, as long as the value of V_{SC} is computed, the DC transport current can be obtained from a straightforward closed-form expression. However, traditional methods [11, 16] to solve the non-linear algebraic equation for V_{SC} are inefficient and need improvement. In the existing modelling approaches of CNT transistors [12, 16], evaluation of the self-consistent voltage from Eq. 3.14 involves a time consuming Newton-Raphson iterative process, which has been described in Algorithm 3.1. Each Newton-Raphson iteration in turn requires evaluations of integrals to obtain state densities $N_S(V_{SC})$ and $N_D(V_{SC})$. Due to the iteration process, these approaches are not efficient (consuming circa 10 seconds for a single transistor simulation, which will be shown in detail in Section 3.2). To accelerate the solution of Eq. 3.14 and thus improve the efficiency of CNT transistor modelling, piece-wise approximation techniques that eliminate the iteration process while maintaining a high modelling accuracy are

developed in the following sections.

3.2 Numerical Model Based on Piece-Wise Linear Approximation of Mobile Charge Density

The typical dependence of non-equilibrium mobile charge density at the source, calculated from Equations 3.2, 3.7 and 3.9, is illustrated in Figure 3.3. From Equations 3.9 and 3.10 it can be concluded that the difference between U_{SF} and U_{DF} is determined only by V_{DS}. The corresponding graph of the drain charge density has a similar shape as the source one with a V_{SC}-axis shift of $-V_{DS}$. As explained in Section 3.1.2, the conventional technique which directly substitutes this relationship into Eq. 3.14 leads to an iterative calculation and becomes inefficient. Unlike the modelling approach proposed in [11], in which a piece-wise approximation of the state densities relies on symbolic calculations of slopes and intersection points from CNT parameters, the technique developed in this section is not to link the slopes and intersection points to CNT parameters directly but rather to use an arbitrary number of them and adjust their slopes and intersection points to maximise the overall drain current characteristic accuracy. A piece-wise linear approximation that generates a polyline fitting the density of states curve has been employed in the modelling, which is explained in detail in Section 3.2.1. The approximation dramatically simplifies the computational complexity and reduces the CPU time by up to almost three orders of magnitude compared with FETToy, a popular existing theoretical model [16] introduced in Section 2.6. This section will describe the implementation of the piece-wise linear approximation based modelling technique and show the performance of the proposed model.

3.2.1 MATLAB Implementation of the CNT Transistor Model Based on Piece-Wise Linear Approximation

It has been confirmed that the numerical relationship between mobile charge density and self-consistent voltage is the key factor in calculating the channel current I_{DS} of the CNT transistor in Section 3.1.2. Therefore, this research aims to implement the piece-

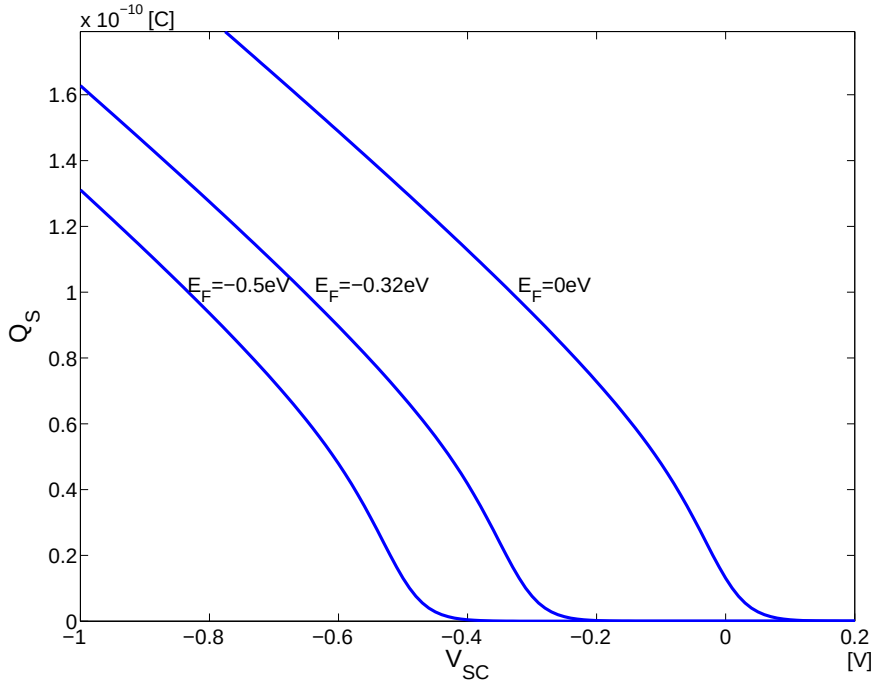

FIGURE 3.3: The theoretical source mobile charge Q_S at different Fermi levels.

wise linear approximation of mobile charge densities of CNT transistors in MATLAB and compare the new technique with the computationally inefficient solving process for Eq. 3.14 in conventional modelling techniques [11, 12].

It is necessary to explain the functional structure of the implementation of the piece-wise linear approximation based model using MATLAB. Terminal voltages of the CNT transistor can be set at the input stage and then parameters will be evaluated for the calculation at the next stages. An example of MATLAB pseudo code describing the piece-wise linear approximation of the developed model is shown in Algorithm 3.2. The inputs are defined first, where terminal voltages, Fermi-levels, CNT diameters, and the temperature are selected. Parameters and constants used in the calculation of the I-V characteristics including electronic charge, vacuum permittivity and tight-binding potential are defined in line 1 of Algorithm 3.2, while a number of parameters which can affect the self-consistent voltage, including terminal capacitances and band gap, are computed in line 2.

Algorithm 3.2 provides details of the approximation fitting process and I_{DS} calculation. To implement the piece-wise linear approximation of the mobile charge, the intervals

and boundaries are determined by the fitting process. Usually, a limited V_{SC} range ($\sim 0.5V$) around the typical E_F value is scanned by a small scale ($\sim 0.01V$, depending on the precision required) each time the terminal voltages are changed and the errors of all corresponding linear pieces will be compared with theoretical results. The ones with least deviation are chosen for the the piece-wise linear approximated curve and the linear equation set will be derived.

The fitting algorithm of the piece-wise linear approximation is described in lines 8-22 of Algorithm 3.2. This algorithm has been implemented as a self-adjusting process within a specified range. With different terminal voltages (V_G, V_D and V_S), a series of boundaries on the proposed V_{SC} region is selected. Then for each boundary, the corresponding value of $Q_S(V_{SC})$ can be derived using Eq. 3.2 and linear equations can be built between each two neighbour boundaries. Therefore the non-linear Eq. 3.14 will be simply represented using a set of linear equations. According to Eq. 3.9 and 3.10, the $Q_D(V_{SC})$ curve can be reflected as a horizontal shift of $Q_S(V_{SC})$ by the distance of V_{DS}. Therefore, the piece-wise linear approximation algorithm can work on $Q_D(V_{SC})$ in a similar way. The approximated results will then be compared with the theoretical $Q_S(V_{SC})$ value and the boundaries with the smallest difference will be chosen as the appropriate fitting conditions. In this research the concept of normalised RMS error which is expressed in Eq. 3.17 is applied to represent the difference.

$$normalised\ RMSE = \frac{\sqrt{\frac{\sum_{i=1}^{n}(a_i - b_i)^2}{n}}}{max(a_i, b_i) - min(a_i, b_i)} \tag{3.17}$$

In the RMSE equation, a_i and b_i represent the theoretical $Q_S(V_{SC})$ value and that calculated from the linear approximation respectively. As long as the matching boundaries that have the smallest RMSE are obtained, the approximated linear equations of $Q_S(V_{SC})$ and $Q_D(V_{SC})$ can be used to replace the complicated non-linear ones in the calculation of V_{SC}. Eq. 3.18 shows an example of the expressions used for a 3-piece linear approximation mode, and the resulting $Q_S(V_{SC})$ is compared with theoretical curves in Figure 3.4. Here the diameter of the CNT is $1nm$ and the Fermi level is $-0.32eV$ at $T = 300K$.

Algorithm 3.2: Piece-wise Linear Approximation of the Density of States

Input: terminal voltages V_G,V_D,V_S, Fermi level E_F, CNT diameter d, Temperature T and plot intervals n

Output: drain current I_{DS}

set constants: electronic charge q, dielectric constant of top gate dielectric material k, vacuum permittivity $e0$, length of CNT region L, atom-to-atom distance for tight-binding CNTs acc, tight-binding potential Vcc and Planck constant h;
compute V_{SC} related parameters: flat band mobile charge density $N0$, terminal capacitances Cge, Cde, Cse and CNT band gap Eg;
for $vg = 0 : +0.1 : V_G$ **do**
    $i = 0$, which is the index of output current value as V_{DS} sweeps;
    $I_{DS} = 0$;
    $V_{DS} = V_D - V_S$;
    for $vd = 0 : n : V_{DS}$ **do**
        $j = 1$, which is the index of the linear equation set and RMSE;
        for $V_{pwl} = 0 : -0.01 : -0.5$ **do**
            shift the boundary at a specific V_{SC} interval ($0.01V$) within a limited range (0 to $-0.5V$) around the given E_F value ($-0.32eV$ here for example);
            each time the boundary shifts, it will divide the Q_S curve into m pieces with different scales;
            then form linearised equation set (LES_j) representing the m-piece linear approximation of the Q_S curve in the form of $Q_S(V_{SC})_k \approx a_k V_{SC} + b_k$ (where $k = 1, ..., m$);
            LES_j indicates the linearly approximated $Q_S(V_{SC})$ relationship instead of the theoretical one;
            compute the discrepancy between LES_j and theoretical $Q_S(V_{SC})$ from Eq. 3.2 by calculating the root-mean square error;
            return all $RMSE_j$;
            $j = j + 1$;
        end
        compare all $RMSE_j$ values and select the smallest one and return its index j;
        the corresponding LES_j fits the theoretical $Q_S(V_{SC})$ best;
        calculate V_{SC} by invoking LES_j in Eq. 3.14;
        calculate drain source current I using Eq. 3.19;
        $i = i + 1$;
        $I_{DS}(i) = I$;
    end
end
return I_{DS};
plot output results;

$$Q_S(V_{SC}) \approx \begin{cases} 0, & (V_{SC} - E_F/q > 0.05) \\ (-3.0594 \cdot V_{SC} - 0.8260) \times 1e - 10, & (-0.15 \leq V_{SC} - E_F/q \leq 0.05) \\ (-2.0278 \cdot V_{SC} - 0.3412) \times 1e - 10, & (V_{SC} - E_F/q < -0.15) \end{cases} \tag{3.18}$$

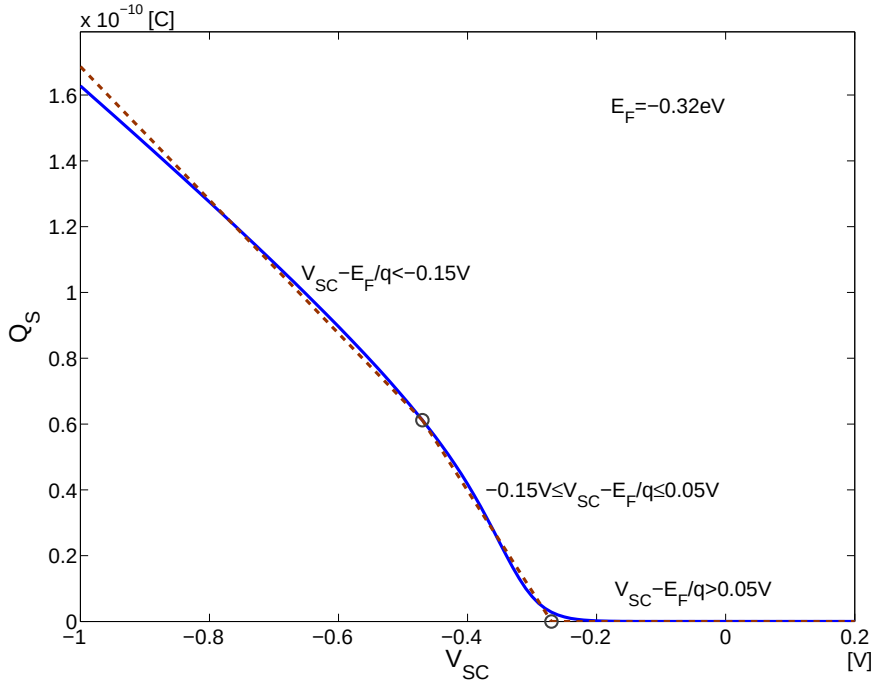

FIGURE 3.4: Example of a 3-piece linear approximation of the source mobile charge Q_S.

Solving the linear equation set Eq. 3.18 is much faster than the Newton-Raphson iterative solution of Eq. 3.14 in conventional approaches. Once the self-consistent voltage V_{SC} is calculated from the closed-form solution of Eq. 3.14 which after invoking the linear approximation in Eq. 3.18 represents only linear equations, the total drain current can be directly obtained from Eq. 3.19 [11].

$$I_{DS} = \frac{2qkT}{\pi\hbar}\left[ln(1 + e^{\frac{E_F - qV_{SC}}{kT}}) - ln(1 + e^{\frac{E_F - q(V_{SC}+V_{DS})}{kT}})\right] \tag{3.19}$$

3.2.2 Performance of the CNT Transistor Model Based on Piece-Wise Linear Approximation

Substituting the linear approximation of mobile charge densities into Eq. 3.14, the piece-wise linear approximation based model can be simulated. Figure 3.5 shows an example of the I-V characteristics of the n-type CNT transistor model with 3-piece linear approximation. Typical values of the Fermi level (-0.32eV) and temperature (300K) have been used [12, 16, 21, 22]. In Figure 3.5, the simulated drain current of the developed n-type CNT transistor model (dashed lines) has been compared with that of FETToy [16] (solid lines), while there is a close correlation between these two simulated CNT transistor models.

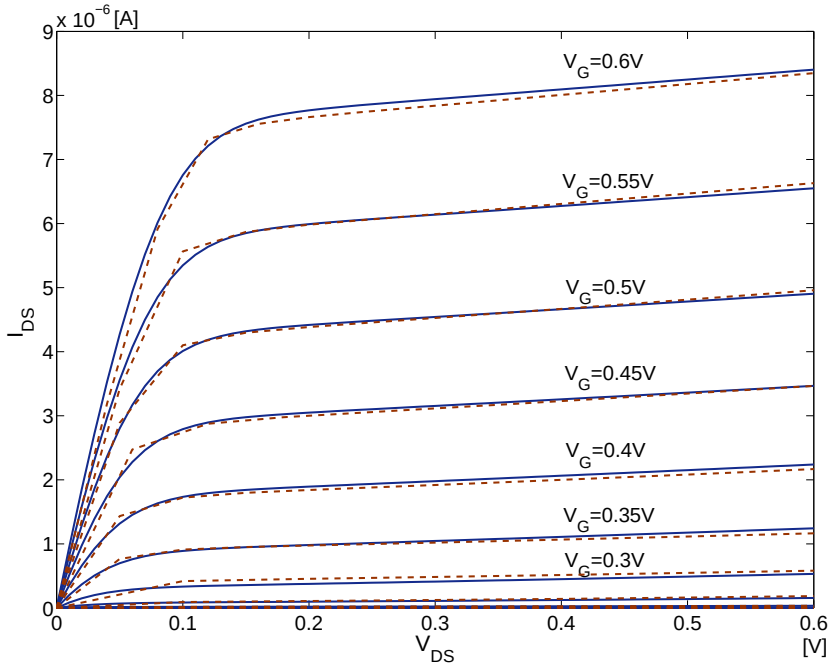

FIGURE 3.5: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece linear approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 300K$.

Figures 3.6 and 3.7 show the simulated drain current of the proposed n-type CNT transistor model with different Fermi levels. As the Fermi level rises from -0.5eV to 0, the threshold voltage of a CNT transistor gets lower [12]. Furthermore, the drain current of the transistor also increases with higher Fermi levels.

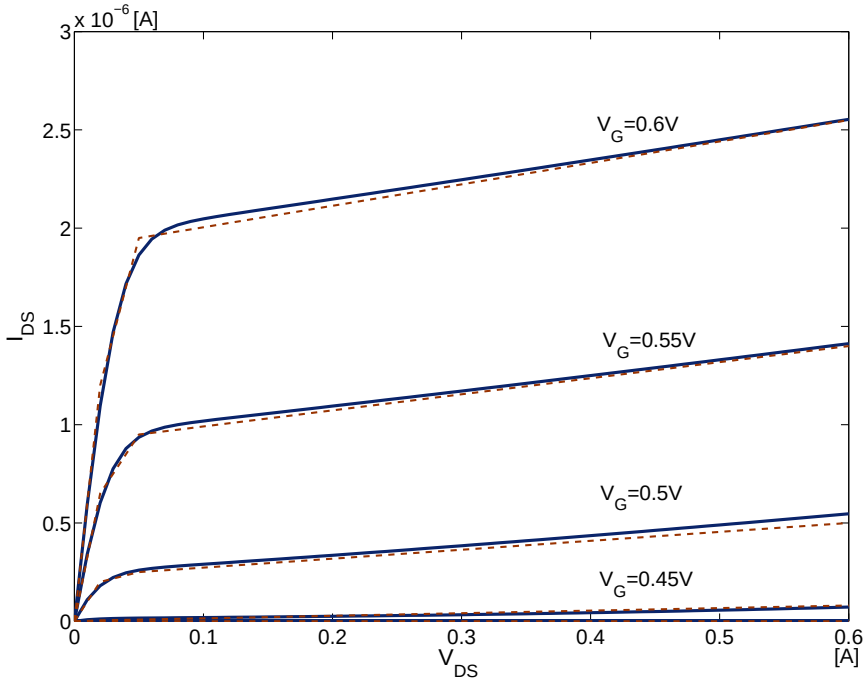

FIGURE 3.6: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece linear approximation with $E_F = -0.5eV$, $d = 1nm$ and $T = 300K$.

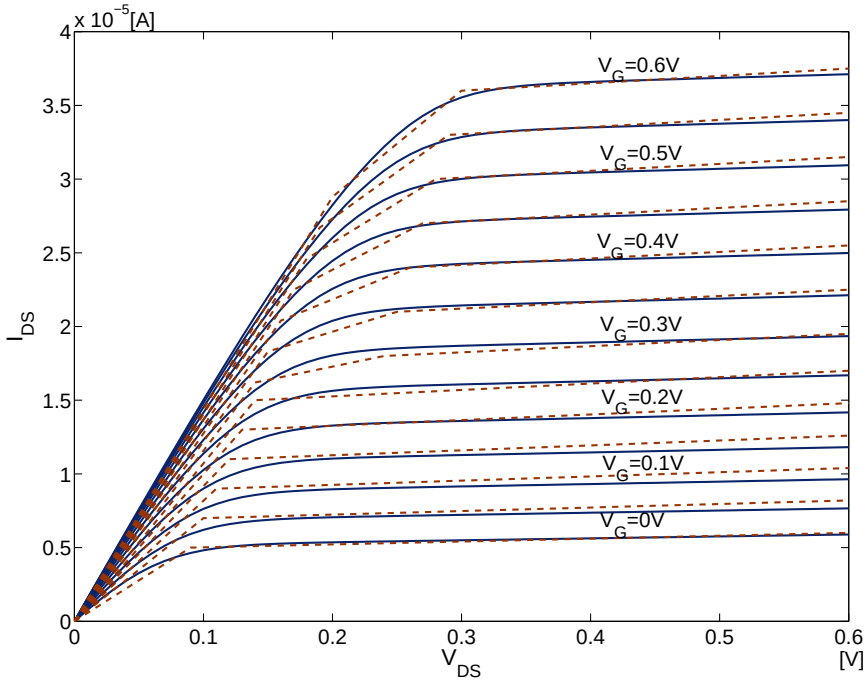

FIGURE 3.7: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece linear approximation with $E_F = 0eV$, $d = 1nm$ and $T = 300K$.

Additionally, Figures 3.8 and 3.9 show the drain current characteristics of the proposed model when the temperature changes. The drain current of the CNT transistor increases when the temperature goes up from $150K$ to $450K$, which matches the theoretical prediction [12, 22]. With higher temperatures, the mobility of carriers within the CNT channel increases, and thus results in higher current.

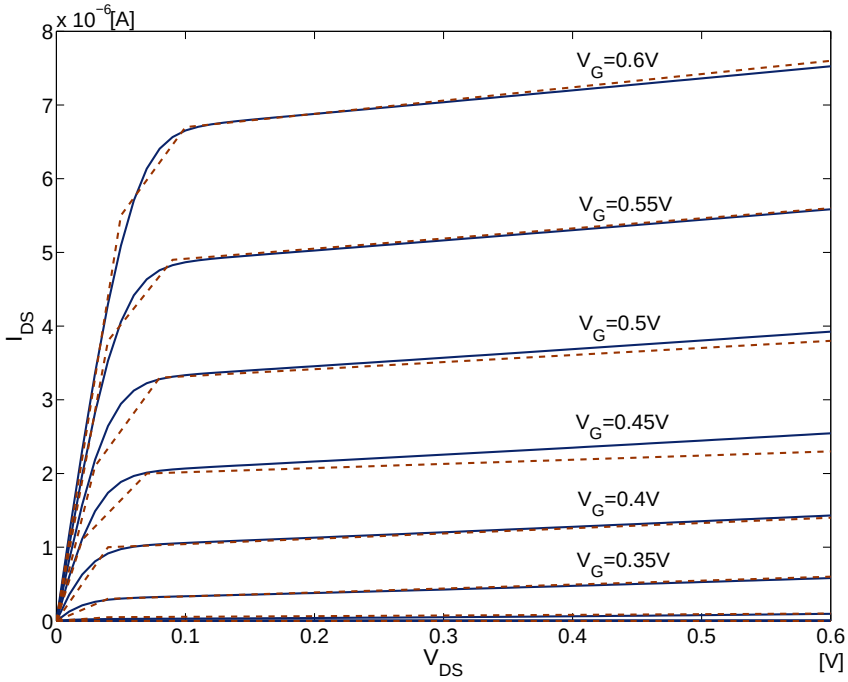

FIGURE 3.8: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece linear approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 150K$.

As can be seen from the simulated drain current characteristics, the developed CNT transistor model based on numerical piece-wise linear approximation can generally describe the ballistic transport characteristics of CNT transistors. However, the simulated I-V current curves are not smooth enough and have some inflexion points between the piece-wise linear regions. In this section, the number of approximation pieces used in the simulation is set to three. More pieces can be used to achieve higher approximation accuracy, but more simulation time will be required.

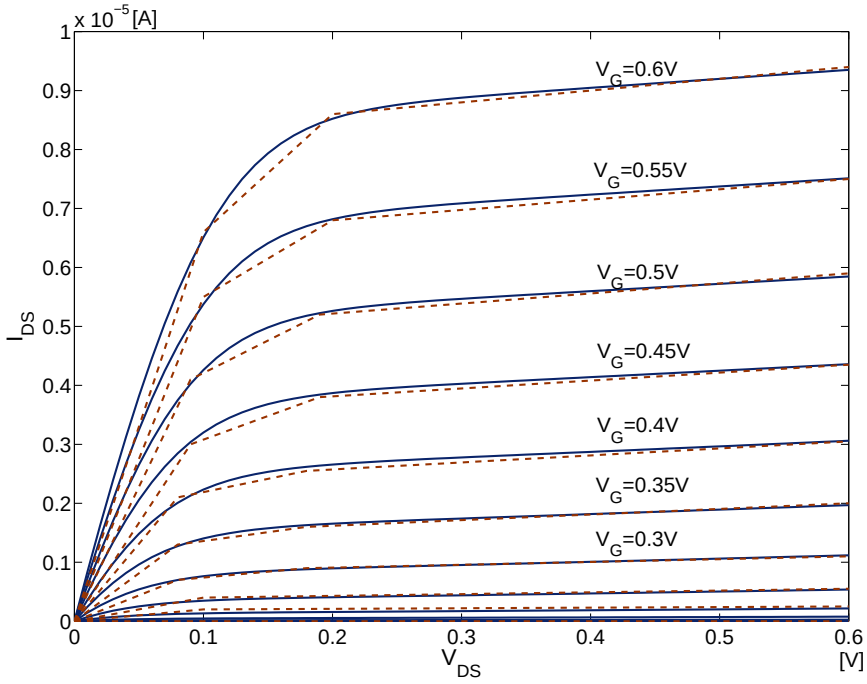

FIGURE 3.9: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece linear approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 450K$.

To identify the computational efficiency of the proposed piece-wise linear approximation based model, the CPU time of the model has been measured and compared with that of FETToy [16], which uses the conventional iterative method to implement the model. As the FETToy MATLAB script is freely available on line, it has been employed in this research by replacing FETToy's I_{DS} code with the proposed piece-wise algorithm for the fast model as outlined above. In this way equal conditions for the purpose of the performance evaluation in both models are maintained, including the same CNT parameter values as in the original FETToy script, as well as identical set up and output code. Results in Table 3.1 show that a speed-up of almost three-hundred times has been achieved by the proposed piece-wise linear approximation based model. To obtain accurate measurement results, an extra outermost loop was added to run both algorithms 100 times. In the measurement, the code to generate output plots in the original FETToy model might cost extra simulation time and thus was switched off for the purpose of the CPU time comparison.

TABLE 3.1: Average CPU Time Comparison between FETToy and the proposed model based on piece-wise linear approximation

Loops	**FETToy**	**3-Piece Linear Approximation Based Model**
5	64.43s	0.017s
10	128.78s	0.031s
50	642.44s	0.177s
100	1287.45s	0.359s

Tables 3.2, 3.3 and 3.4 list the root mean square errors (RMSEs) of the developed piece-wise linear approximation based model compared with theoretical results from FETToy [16]. As can be seen from the tables, the average discrepancy of the numerical model is larger than 10%, which shows that the accuracy of the proposed model needs to be improved.

TABLE 3.2: Average RMS errors of I_{DS} of the proposed model based on 3-piece linear approximation with $E_F = -0.32eV$.

$V_G[V]$	150K	300K	450K
0.1	13.0%	11.2%	10.3%
0.2	11.6%	10.6%	10.9%
0.3	10.5%	10.7%	9.9%
0.4	10.8%	9.9%	9.3%
0.5	9.7%	10.3%	9.5%
0.6	10.9%	10.2%	9.8%

TABLE 3.3: Average RMS errors of I_{DS} of the proposed model based on 3-piece linear approximation with $E_F = -0.5eV$.

$V_G[V]$	150K	300K	450K
0.1	11.6%	10.9%	10.1%
0.2	11.3%	10.4%	9.7%
0.3	11.0%	10.1%	9.4%
0.4	10.6%	9.7%	10.0%
0.5	10.4%	10.6%	9.8%
0.6	9.7%	9.8%	9.6%

TABLE 3.4: Average RMS errors of I_{DS} of the proposed model based on 3-piece linear approximation with $E_F = 0eV$.

$V_G[V]$	150K	300K	450K
0.1	14.1%	13.2%	12.8%
0.2	13.5%	12.8%	12.4%
0.3	13.3%	12.6%	12.0%
0.4	13.0%	12.4%	11.8%
0.5	12.7%	12.5%	11.7%
0.6	12.9%	11.7%	11.1%

The piece-wise linear approximation of the density of states can simplify Eq. 3.14 and dramatically reduce the calculation time of V_{SC}. However, the existence of inflexion points limits the accuracy of the piece-wise linear approximation, and it needs to be improved. For this purpose, a new technique based on quadratic polynomial approximation is developed and introduced in Section 3.3.

3.3 CNT Transistor Model Based on Quadratic Polynomial Approximation of Mobile Charge Density

After obtaining the piece-wise linear approximation based model of the CNT transistor, there is still room to improve the performance of the technique. The quadratic polynomial piece-wise approximation was chosen as it can describe the non-linear relationship between the charge density and the self-consistent voltage more accurately than the linear approximation while keeping the calculation's simplicity.

3.3.1 MATLAB Implementation of the CNT Transistor Model Based on Quadratic Approximation

Although the piece-wise linear approximation dramatically accelerates the calculation, it obviously compromises much of the accuracy of the model. Similarly to the implementation of the piece-wise linear approximation based CNT transistor model, the modelling of the proposed quadratic polynomial based model employs an input stage, a fitting

process, and an output stage. The input stage of the polynomial based CNT transistor model in MATLAB is similar to that of the piece-wise linear approximation model, which contains the definitions of input ports, default parameter values and equations to calculate internal parameters. Terminal voltages of the CNT transistor can be set at the input stage and then parameters will be evaluated for the calculation at the next stage.

Algorithm 3.3: Quadratic Polynomial Approximation of the Density of States

Input: V_G,V_D,V_S,E_F,d,T and n
Output: I_{DS}

set constants and compute V_{SC} related parameters;
for $vg = 0 : +0.1 : V_G$ **do**
    $i = 0$, which is the index of output current value as V_{DS} sweeps;
    $I_{DS} = 0$;
    $V_{DS} = V_D - V_S$;
    for $vd = 0 : n : V_{DS}$ **do**
        $k = 1$, which is the index of the linear equation set and RMSE;
        for $V_{pwl} = 0 : -0.01 : -0.5$ **do**
            shift the boundary at a specific V_{SC} interval ($0.01V$) within a limited range (0 to $-0.5V$) around the given E_F value ($-0.32eV$ for instance);
            as the boundary shifts, it will divide the Q_S curve into m pieces with different scales;
            then form quadratic equation set (QES_k) representing the m-piece linear approximation of the Q_S curve in the form of $Q_S(V_{SC})_p \approx a_p V_{SC}^2 + b_p V_{SC} + c_p$ (where $p = 1, ..., m$);
            QES_k describes the quadratic piece-wise approximation of $Q_S(V_{SC})$ instead of the theoretical one;
            compute the discrepancy between QES_k and theoretical $Q_S(V_{SC})$ from Eq. 3.2 by calculating the root-mean square error ($RMSE_k$) between them;
            return $RMSE_k$;
            $k = k + 1$;
        end
        compare all $RMSE_k$ values and select the smallest one and return its index k;
        the corresponding QES_k matches the theoretical $Q_S(V_{SC})$ most closely;
        calculate V_{SC} by invoking QES_k in Eq. 3.14;
        calculate drain source current I using Eq. 3.19;
        $i = i + 1$;
        $I_{DS}(i) = I$;
    end
end
return I_{DS} and plot results;

The functional structure of the quadratic polynomial approximation is shown in Algorithm 3.3, which is similar to that of the piece-wise linear approximation in Algorithm 3.2 outlined in Section 3.2.1. However, it requires a 2^{nd} order non-linear adjusting process other than a linear one in the piece-wise linear approximation based model introduced

in Section 3.2. The aim of this technique is to simplify the strongly non-linear $Q_S\,(V_{SC})$ and $Q_S\,(V_{SC})$ equations into quadratic polynomial equation sets so that they can be solved without numerical complication thus saving simulation time. Compared with the piece-wise linear approximation model, the quadratic approximation based model may consume more time for the polynomial fitting process, but its accuracy will exceed that of the linear approximation.

Similarly to the fitting process introduced in Section 3.2.1, when applying the approximation to the charge density, the boundaries of each piece are initially estimated within certain ranges and then computed. A limited range is scanned by a small scale (~ 0.01, depending on the precision required) each time the terminal voltages are changed and the errors of all corresponding polynomial pieces are calculated and compared. The ones with least deviation were chosen to divide the piece-wise approximated curve. Polynomial equations are then obtained according to the similar rule. The approximation results are compared with the theoretical curves calculated from Equations 3.2, 3.7 (Q_S) and 3.3, 3.8 (Q_D) correspondingly. Model A, illustrated in Figure 3.10, uses three piece-wise regions: 1) linear, when $V_{SC} \leq \frac{E_F}{q} - 0.08V$, 2) quadratic, when $\frac{E_F}{q} - 0.08V < V_{SC} < \frac{E_F}{q} + 0.08V$ and 3) zero, when $V_{SC} \geq \frac{E_F}{q} + 0.08V$. The more accurate Model B uses four piece-wise regions as shown in Figure 3.11: 1) linear, when $V_{SC} \leq \frac{E_F}{q} - 0.28V$, 2) quadratic, when $\frac{E_F}{q} - 0.28V < V_{SC} \leq \frac{E_F}{q} - 0.03V$, 3) quadratic, when $\frac{E_F}{q} - 0.03V < V_{SC} \leq \frac{E_F}{q} + 0.12V$ and 3) zero, when $V_{SC} > \frac{E_F}{q} + 0.12V$. The polynomial parameters have been optimised for fitting accuracy, while assuring the continuity of the first derivative, over the temperature range $150K \leq T \leq 450K$, Fermi level range $-0.5eV \leq E_F \leq 0V$ and assuming the carbon nanotube diameter of $1nm$.

Equations 3.20 and 3.21 show two examples of the polynomial equation sets used for 3-piece and 4-piece quadratic approximation modes respectively. For these two examples, the CNT diameter is set to a typical value of $1nm$, with $E_F = -0.32eV$ at $T = 300K$, which is comparable with the theoretical instance stated above. It can be seen that only quadratic and linear equations are used to represent the approximation value of Q_S and thus the numerical calculation is simplified.

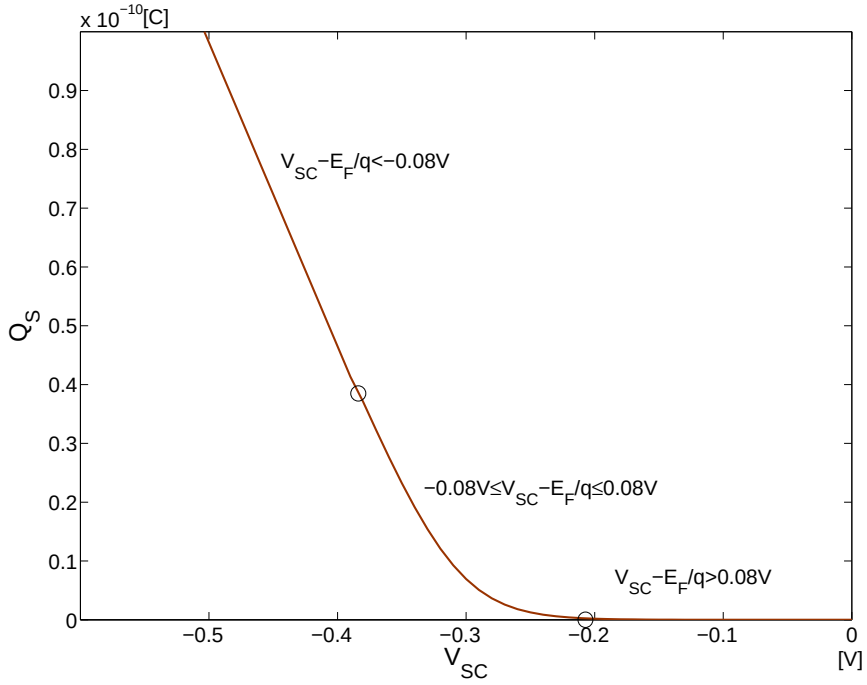

FIGURE 3.10: Model A: three-piece quadratic approximation of source mobile charge of CNT transistor.

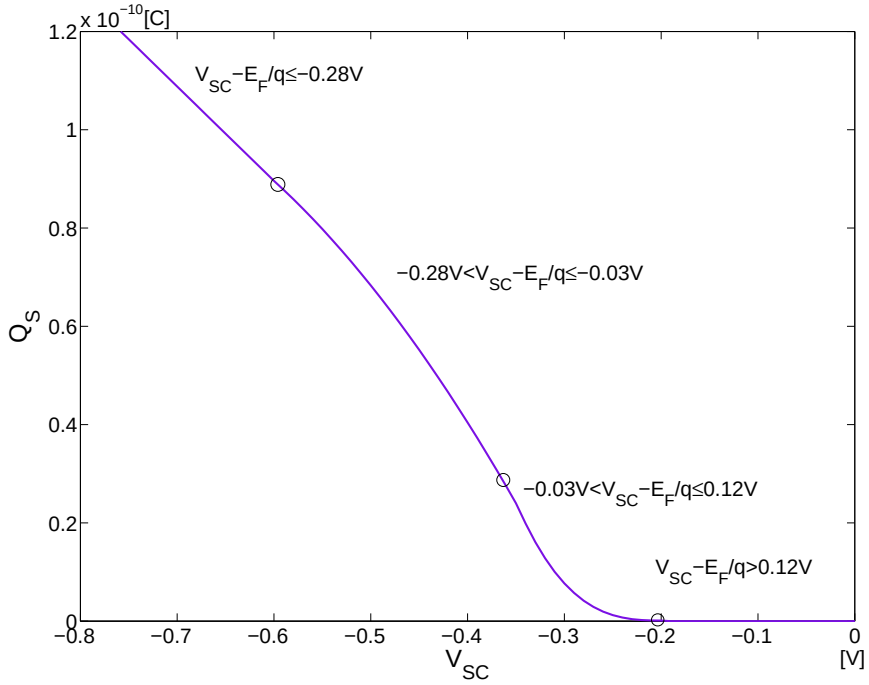

FIGURE 3.11: Model B: more accurate four-piece non-linear approximation of source mobile charge of CNT transistor.

$$Q_S(V_{SC}) \approx \begin{cases} 0, & (V_{SC} - E_F/q > 0.08) \\ (16.3136 \cdot V_{SC}^2 + 7.8305 \cdot V_{SC} + 0.9397) \times 1e - 10, & (-0.08 \le V_{SC} - E_F/q \le 0.08) \\ (-5.2203 \cdot V_{SC} - 1.6705) \times 1e - 10, & (V_{SC} - E_F/q < -0.08) \end{cases} \tag{3.20}$$

$$Q_S(V_{SC}) \approx \begin{cases} 0, & (V_{SC} - E_F/q > 0.12) \\ (10.6136 \cdot V_{SC}^2 + 4.2454 \cdot V_{SC} + 0.4245) \times 1e - 10, & (-0.03 \leq V_{SC} - E_F/q \leq 0.12) \\ (-2.2187 \cdot V_{SC}^2 - 4.7372 \cdot V_{SC} - 1.1474) \times 1e - 10, & (-0.28 \leq V_{SC} - E_F/q \leq -0.03) \\ (-2.0748 \cdot V_{SC} - 0.3487) \times 1e - 10, & (V_{SC} - E_F/q < -0.28) \end{cases} \tag{3.21}$$

The quadratic polynomial approximations of the drain and source mobile charge densities calculated using Model A (3-piece approximation) for the typical temperature and Fermi level values of $T = 300K$ and $E_F = -0.32eV$ correspondingly are illustrated and compared with the theoretical graphs in Figure 3.12. A similar illustration and comparison for Model B (4-piece approximation) is shown in Figure 3.13. The numerical equations representing the approximation $Q_S(V_{SC})$ curves are shown in Eq. 3.20 and 3.21. As can be seen from these two figures, Model B reflects more accurately the mobile charge especially in the ranges representing larger values of the charge.

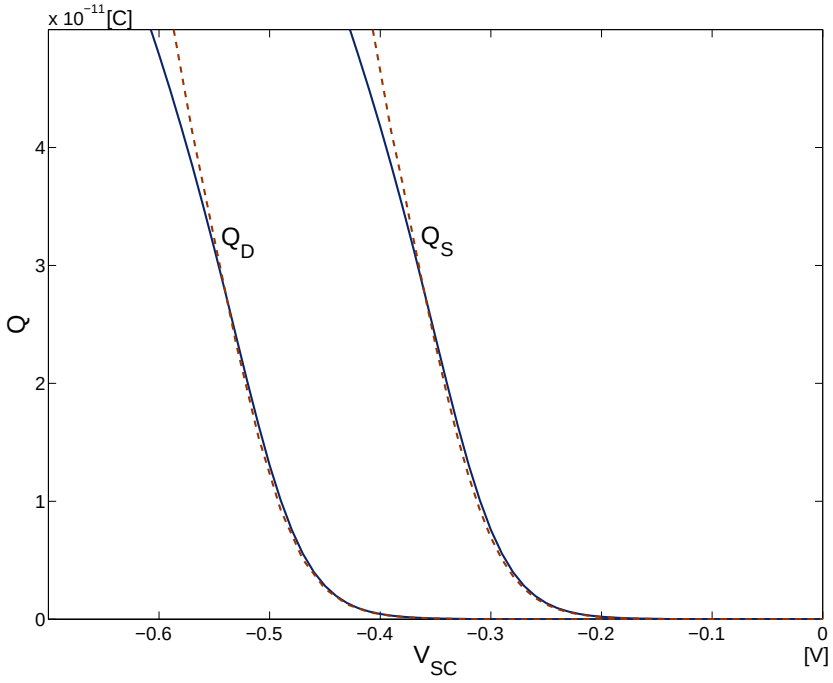

FIGURE 3.12: Mobile charges at drain and source for $T = 300K$, $d = 1nm$ and $E_F = -0.32eV$ (solid lines) and their piece-wise approximation using Model A (dashed lines).

Both models use polynomials of order no greater than 2 and hence allow a closed-form

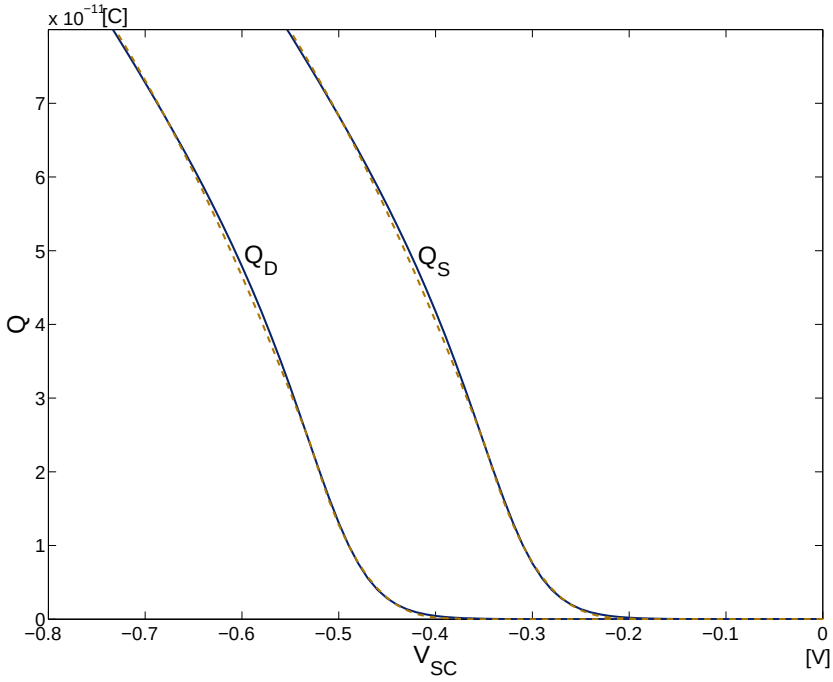

FIGURE 3.13: Mobile charges at drain and source for $T = 300K$, $d = 1nm$ and $E_F = -0.32eV$ (solid lines) and their piece-wise approximation using Model B (dashed lines).

solution of the self-consistent voltage equation (Eq. 3.14), which eliminates the need for Newton-Raphson iterations. More non-linear pieces of the approximation result in higher accuracy but require more simulation time as a trade-off. In the following part of this section, the performance of the quadratic approximation based CNT transistor model is analysed and compared with that of existing models like FETToy [16].

3.3.2 Performance of the CNT Transistor Model Based on Quadratic Polynomial Approximation

Once the self-consistent voltage V_{SC} is calculated from the solutions of Eq. 3.14 which after the approximation represents only linear, quadratic or 3^{rd} order polynomial equations, the total drain current can be directly obtained from Eq. 3.19. These calculations are fast, as Newton-Raphson iterations and integration of the Fermi-Dirac probability distribution are eliminated.

Figures 3.14 and 3.15 show the simulated drain current of Model A (with 3-piece quadratic approximation) and Model B (with 4-piece approximation) respectively. The

TABLE 3.5: Average RMS errors of I_{DS} of Model A and Model B when $E_F = -0.32eV$.

	150K		300K		450K	
$V_G[V]$	Model A	Model B	Model A	Model B	Model A	Model B
0.1	4.0%	2.7%	4.4%	3.0%	4.6%	3.3%
0.2	3.2%	2.3%	3.6%	2.7%	3.7%	2.9%
0.3	2.5%	2.0%	2.7%	2.4%	2.9%	2.6%
0.4	2.8%	2.7%	2.9%	2.0%	2.3%	2.3%
0.5	2.5%	2.4%	2.6%	2.2%	3.6%	2.5%
0.6	2.9%	2.8%	3.2%	2.6%	2.7%	2.4%

performance of the proposed quadratic approximation based model is evaluated by comparing the simulated I_{DS} with that of FETToy [16]. Both models maintain a high accuracy in terms of the average RMS error as shown in Table 3.5. As expected, with more approximation pieces, Model B is more accurate than Model A with errors not exceeding 4% throughout the typical ranges of drain voltages V_{DS} and gate bias V_G (0-0.6V).

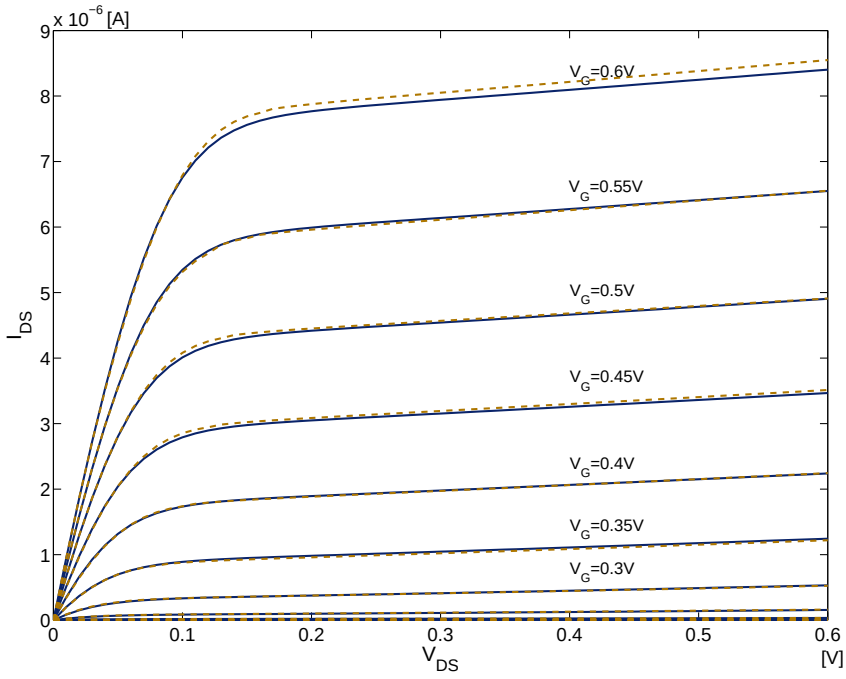

FIGURE 3.14: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece quadratic approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 300K$.

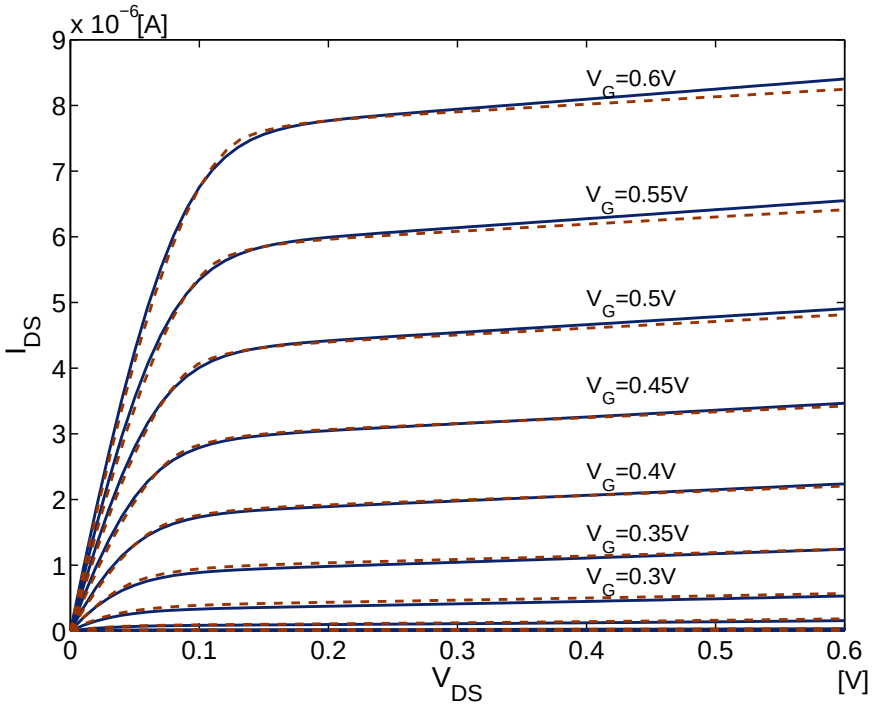

FIGURE 3.15: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 4-piece quadratic approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 300K$.

Table 3.6 shows the average CPU time of both Model A and Model B together with that of FETToy. For accurate measurement, several experiments were carried out by invoking all models 5, 10, 50 and 100 times. Furthermore, the MATLAB function to generate graphic output plots was switched off for the purpose of the CPU time comparison. The simulation results showed that both models are more than three orders of magnitude faster than FETToy: Model A is about 3400 times faster and Model B more than 1100 times.

TABLE 3.6: Average CPU time comparison between theoretical and the proposed quadratic based model

Loops	**FETToy**	**Model A**	**Model B**
5	64.43s	0.02s	0.06s
10	128.78s	0.04s	0.12s
50	642.44s	0.19s	0.56s
100	1287.45s	0.38s	1.12s

The performance of the proposed model has been analysed when parameters are changed. Figures 3.16 and 3.17 show the drain current characteristics of the proposed quadratic based model with different Fermi levels. As the Fermi level rises from -0.5eV to 0, the

threshold voltage of the CNT transistor drops and the drain current increases.

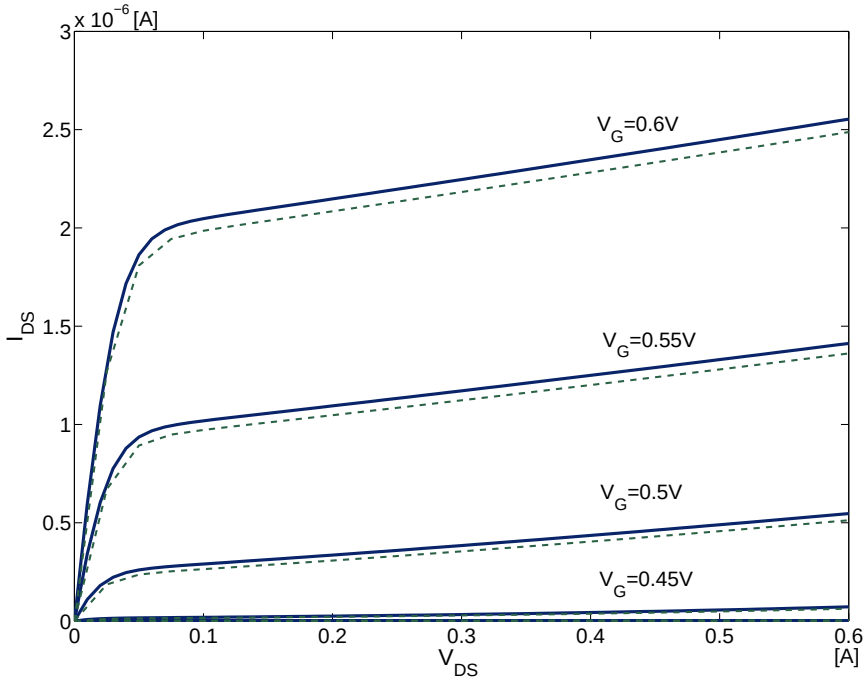

FIGURE 3.16: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece quadratic approximation with $E_F = -0.5eV$, $d = 1nm$ and $T = 300K$.

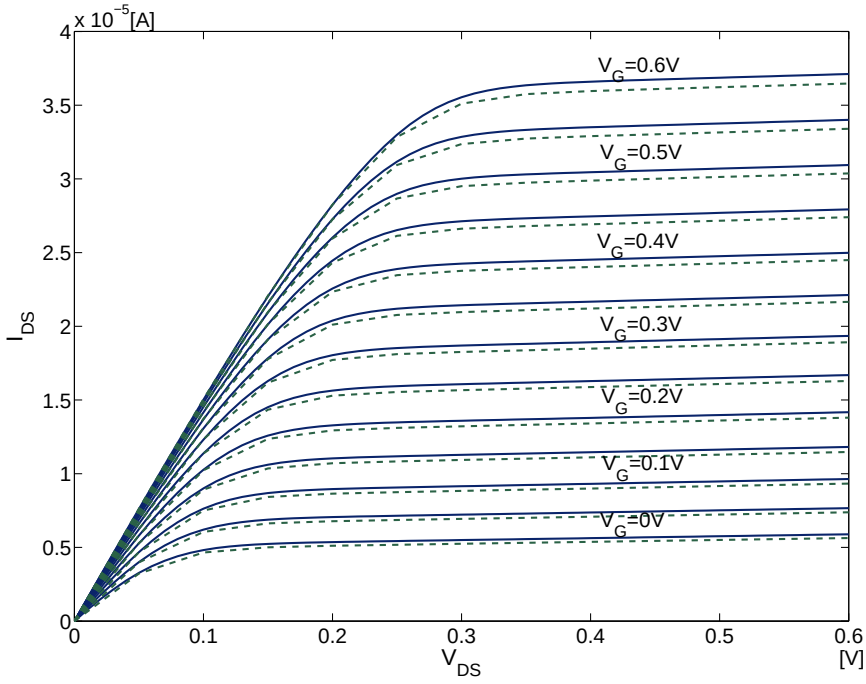

FIGURE 3.17: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece quadratic approximation with $E_F = 0eV$, $d = 1nm$ and $T = 300K$.

The drain current of the proposed model has also been simulated with different temperatures. Figures 3.18 and 3.19 show that the drain current of the CNT transistor increases when the temperature goes up from $150K$ to $450K$, which matches the theoretical prediction [12, 22] and the simulation results of the piece-wise linear approximation based model introduced in Section 3.2.2.

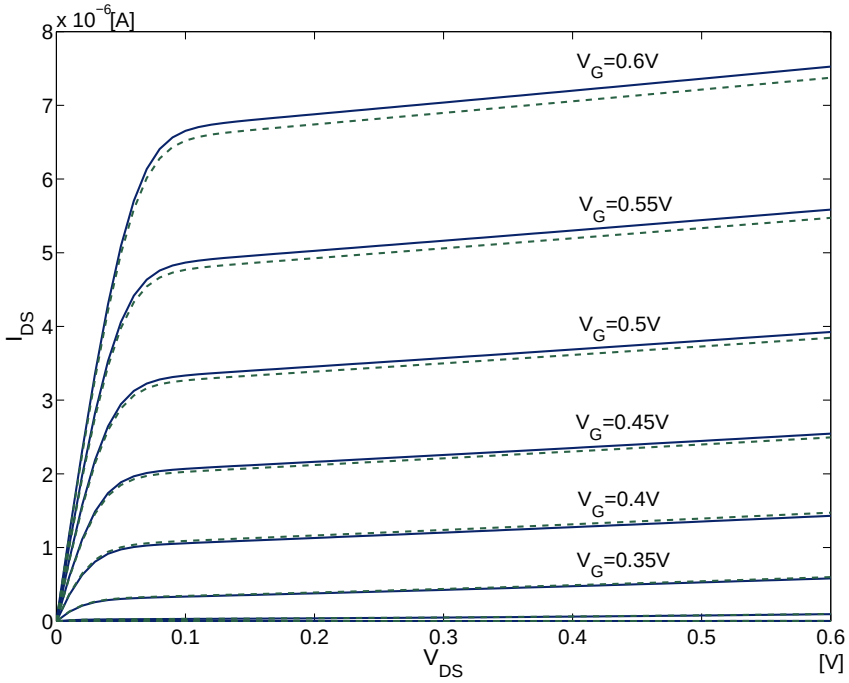

FIGURE 3.18: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece quadratic approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 150K$.

The drain current performance of the proposed quadratic based model were also compared for accuracy with that of the theoretical ballistic CNT transistor FETToy [16] model with specific temperature and Fermi level values. Tables 3.5, 3.7 and 3.8 show average RMS errors for both models with different temperatures ($T = 150K, 300K, 450K$) and Fermi levels ($E_F = -0.5eV, -0.32eV, 0eV$). The comparisons show that the numerical approximation used in the quadratic based model causes a slight loss of accuracy, not exceeding 5%, which is better than the results obtained from the developed model based on piece-wise linear approximation introduced in Section 3.2.

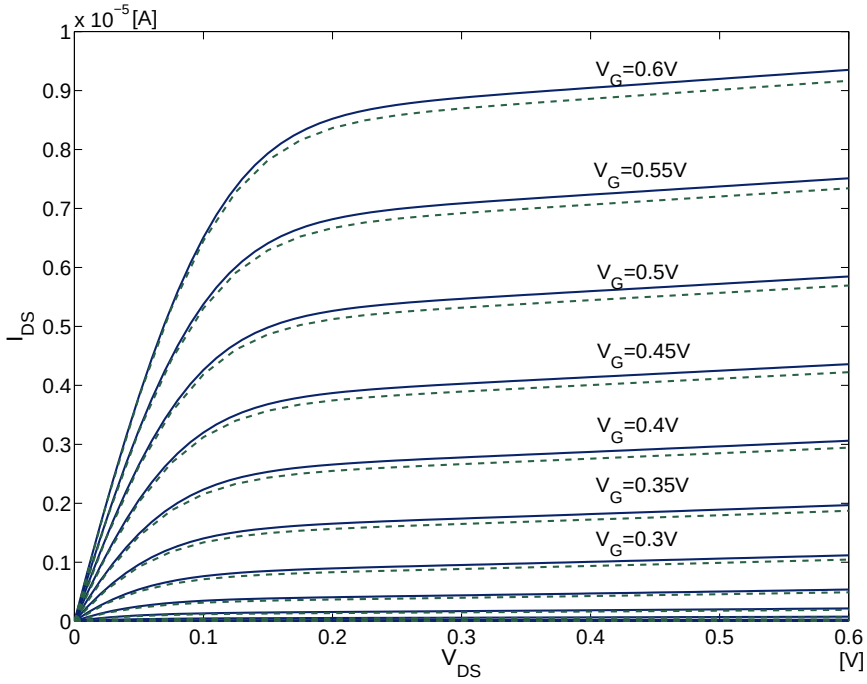

FIGURE 3.19: Drain current characteristics of FETToy (solid lines) and the CNT transistor model (dashed lines) based on 3-piece quadratic approximation with $E_F = -0.32eV$, $d = 1nm$ and $T = 450K$.

TABLE 3.7: Average RMS errors of I_{DS} of Model A and Model B when $E_F = -0.5eV$.

	150K		300K		450K	
$V_G[V]$	Model A	Model B	Model A	Model B	Model A	Model B
0.1	4.4%	3.1%	4.7%	3.3%	4.8%	3.9%
0.2	4.0%	2.5%	4.2%	2.8%	4.3%	3.4%
0.3	3.1%	2.2%	3.3%	2.6%	3.5%	3.0%
0.4	2.2%	2.0%	2.9%	2.4%	2.7%	2.8%
0.5	1.8%	1.7%	2.6%	2.5%	3.5%	2.7%
0.6	2.4%	1.9%	3.3%	2.8%	4.1%	3.1%

TABLE 3.8: Average RMS errors of I_{DS} of Model A and Model B when $E_F = 0eV$.

	150K		300K		450K	
$V_G[V]$	Model A	Model B	Model A	Model B	Model A	Model B
0.1	3.9%	2.6%	3.4%	2.9%	4.0%	3.1%
0.2	3.1%	2.3%	2.6%	2.4%	3.2%	2.7%
0.3	2.6%	2.0%	2.5%	2.1%	2.6%	2.4%
0.4	2.3%	1.6%	1.8%	1.7%	2.7%	2.0%
0.5	2.2%	1.4%	2.3%	1.6%	2.1%	1.8%
0.6	2.5%	1.7%	2.0%	1.8%	3.1%	2.0%

Additionally, CNT transistor models with different diameters have also been simulated. Figure 3.20 shows the ballistic DC transport characteristics of an n-type CNT transistor with CNT diameter $2nm$. The figure shows that the DC performance of the model matches the theoretical calculation from FETToy [16] well, which implies that the quadratic based model can predict the performance of CNT transistors with various channel diameters. Compared with the simulation result of transistor models with CNT diameter $1nm$ shown in Figure 3.14, CNT transistors with larger channel diameters can deliver higher saturation current.

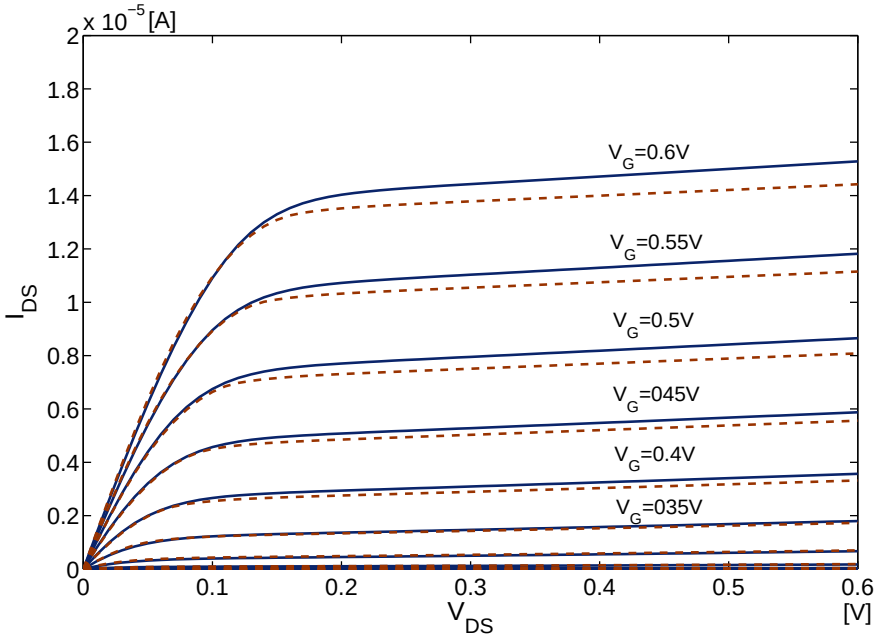

FIGURE 3.20: Drain current characteristics of a CNT transistor with $2nm$ CNT diameter, $T = 300K$ and $E_F = -0.32eV$ using FETToy (solid lines) and 3-piece quadratic approximation (dashed lines).

3.4 Concluding Remarks

This chapter has firstly reviewed the theoretical analysis of the ballistic CNT transport mechanism and the limitation of conventional modelling approaches. In this context, the concept of self-consistent voltage [12] and its application in conventional CNT transistor modelling attempts were introduced and new computationally efficient modelling methods were presented. The chapter proposed new, fast CNT transistor modelling techniques based on numerical approximation of the charge densities of the transistor.

Results were shown to provide further evidence to support the recent suggestion [11] to avoid the use of numerical integration when calculating charge densities in the CNT transistor model, leading to a significant speed-up in the model simulation. It has been demonstrated that although the two techniques proposed in this chapter have similar modelling processes, the quadratic polynomial approximation smooths the inflexion points at the piece-wise boundaries and is more accurate than the linear one, while consuming more CPU time. When compared with FETToy [16], a reference ballistic CNT transistor model, both proposed approximation techniques lead to a computational time saving of more than three orders of magnitude with RMS errors of less than 15%.

Chapter 4

Ballistic CNT Transistor Model Based on Cubic Spline Approximation

It has been stated in Section 3.1 that the conventional approach to the solution of the self-consistent voltage V_{SC} of CNT transistors which uses the Newton-Raphson iterative technique to evaluate solutions of Equations 3.2 and 3.3 [11, 16] requires high simulation time due to iterative computations and repeated integrations and thus is unsuitable for circuit simulation [29]. To accelerate the modelling process, numerical piece-wise approximation techniques that eliminate the need for the iterative calculation were developed in Chapter 3. These techniques suggested calculating the charge densities and self-consistent voltage by dividing the continuous density function into a number of linear and non-linear pieces which together form a fitting approximation of the original charge density curve. Then the V_{SC} equation 3.14 is simplified to a set of linear and quadratic equations, which can be solved efficiently. This has been explained in detail in Chapter 3.

Although the piece-wise approximation techniques have shown lower simulation time than theoretical models [16], their weakness is that they both require accurate fitting process when deciding on the number of linear and non-linear approximation pieces and

intervals of the ranges, which costs simulation time and reduces the accuracy of the model. To improve the performance of the model, a new modelling technique that can automatically generate matching approximation is desirable. For this purpose, a cubic spline approximation of the charge density is proposed in this chapter to overcome the drawbacks of the piece-wise approximation outlined in Chapter 3.

This chapter is organised as follows. Section 4.1 introduces the cubic spline algorithm and its application in the charge density approximation. Section 4.2 describes the MATLAB implementation of the new numerical model based on the cubic spline approximation. In Section 4.3, simulated DC characteristics of the developed spline approximation based CNT transistor model are described. To demonstrate the performance of the developed model for behavioural-level analysis, VHDL-AMS implementation is carried out in Section 4.4. Section 4.5 summarises the conclusion of this chapter.

4.1 Cubic Spline Approximation of the Density of States

A cubic spline is a spline constructed of piecewise third-order polynomials which pass through a set of discrete points. The second derivative of each polynomial is commonly set to zero at the endpoints, since this provides a boundary condition that completes the system of equations. This produces a so-called *natural* cubic spline and leads to a simple tridiagonal system which can be solved easily to give the coefficients of the polynomials. This feature of the cubic spline algorithm can be exploited to automatically generate piece-wise approximation that fits the CNT density of states curves expressed in Equations 3.2 and 3.3 of Chapter 3.

For a set of n ($n \geq 3$) discrete points (x_0, y_0), (x_1, y_1), ..., (x_{i+1}, y_{i+1}) ($i = 0, 1, ..., n-2$), cubic splines can be constructed in the form of Eq. 4.1 [152]:

$$y = Ay_i + By_{i+1} + C\ddot{y}_i + D\ddot{y}_{i+1} \tag{4.1}$$

where A,B,C and D are the coefficients for each pieces of the cubic spline. For simple demonstration here, the horizontal interval between every two neighbour points is equal

to h, then we have $x_1 - x_0 = x_2 - x_1 = ... = x_{i+1} - x_i = h$. Therefore, the cubic spline coefficients can be expressed as functions of x using Equations 4.2, 4.3, 4.4 and 4.5:

$$A \equiv \frac{x_{i+1} - x}{x_{i+1} - x_i} = \frac{x_{i+1} - x}{h} \tag{4.2}$$

$$B \equiv 1 - A = \frac{x - x_i}{x_{i+1} - x_i} = \frac{x - x_i}{h} \tag{4.3}$$

$$C \equiv \frac{1}{6}(A^3 - A)(x_{i+1} - x_i)^2 \tag{4.4}$$

$$D \equiv \frac{1}{6}(B^3 - B)(x_{i+1} - x_i)^2 \tag{4.5}$$

These equations show that A and B are linearly dependent on x, while C and D are cubic functions of x. To derive an expression for $y(x)$, the second-order derivatives of y have to be computed from the following tridiagonal set of linear equations (Eq. 4.6).

$$\begin{bmatrix} 1 & 4 & 1 & & \\ & 1 & 4 & 1 & \\ & & \cdots & & \\ & & 1 & 4 & 1 \end{bmatrix} \begin{bmatrix} \ddot{y}_0 \\ \ddot{y}_1 \\ \cdots \\ \ddot{y}_n \end{bmatrix} = \frac{6}{h^2} \begin{bmatrix} y_2 - 2y_1 + y_0 \\ y_3 - 2y_2 + y_1 \\ \cdots \\ y_n - 2y_{n-1} + y_{n-2} \end{bmatrix} \tag{4.6}$$

After obtaining cubic spline coefficients and second derivatives, the coefficients of each spline a_i, b_i, c_i and d_i can be obtained using Equations 4.2, 4.3, 4.4, 4.5 and 4.6. Therefore, each spline can be represented in the form of Eq. 4.7.

$$y_i = a_i x^3 + b_i x^2 + c_i x + d_i, \ (i = 0, 1, ..., n-2) \tag{4.7}$$

The two linear regions that extend the cubic splines on both sides can be described in Eq. 4.8 and 4.9:

$$y = y_n, \ (x > x_n) \tag{4.8}$$

$$y = a_l x + b_l, \ (x < x_0) \tag{4.9}$$

where $a_l = \ddot{y}_0 = 3a_0x_0^2 + 2b_0x_0 + c_0$ and $b_l = y_0 - a_l x_0$. For example the density of states at the source $N_S(V_{SC})$ can be accurately approximated by choosing a number of V_{SC} points at the range around the given Fermi level of the CNT. The cubic spline approximation of the V_{SC} curve can be calculated based on the equations described above (Equations 4.1 - 4.9) in the form of Eq. 4.10.

$$N_S(V_{SC}) \approx \begin{cases} a_l V_{SC} + b_l, & (V_{SC} \leq V_{SC(0)}) \\ a_i V_{SC}^3 + b_i V_{SC}^2 + c_i V_{SC} + d_i, & (V_{SC(i)} < V_{SC} \leq V_{SC(i+1)}, i = 0, 1, ..., n-2) \\ b_n, & (V_{SC} > V_{SC(n-1)}) \end{cases} \tag{4.10}$$

4.2 MATLAB Implementation of the CNT Transistor Model Based on Cubic Spline Approximation

Following the analysis of the feasibility of applying cubic splines in the approximation of the CNT density of states, a numerical implementation has been developed in MATLAB. An example model representing the relationship between the density of states and the self-consistent voltage, which uses three cubic splines, four interval points ($n = 4$), and two linear pieces at the ends, has been compared with the theoretical $N_S(V_{SC})$ curve calculated from Eq. 3.2 as shown in Figure 4.1. For this implementation the Fermi level of the CNT was set to be a typical value $-0.32eV$ at room temperature and the diameter was $1nm$.

When applying the cubic spline approximation to the density of states, the first step is to set the boundary of the cubic spline region and the number of cubic spline pieces.

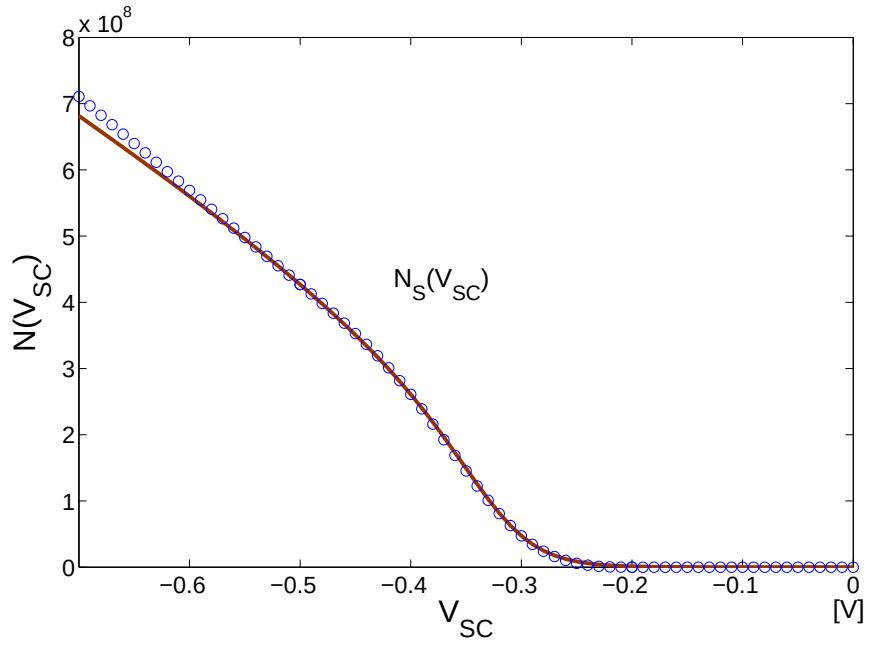

FIGURE 4.1: Piece-wise cubic spline approximation with $n = 4$(circlet line) of source mobile charge density of CNT transistor compared with the theoretical result (solid line).

According to Eq. 4.10, for the $n = 4$ cubic spline proposed in Figure 4.1, the approximation $N_S(V_{SC})$ curve can be represented using a set of polynomial and linear equations. Eq. 4.11 represents an example of such equation set for the $n = 4$ cubic spline approximation with typical CNT parameters, namely $d = 1nm$, $E_F = -0.32eV$ and $T = 300K$. The cubic spline boundaries for this example are $xmax = -0.2$ and $xmin = -0.5$. To solve the resulting 3^{rd} order polynomial equations, Cardano's method [153] is applied to determine the appropriate root which represents the correct value of V_{SC}. According to Eq. 3.10, in the expression for $N_D(V_{SC})$, V_{SC} in Eq. 4.11 should be replaced by $V_{SC} - V_{DS}$.

$$N_S(V_{SC}) \approx \begin{cases} (-0.1420V_{SC} + -0.0283) \cdot 1e10, & (V_{SC} \leq -0.5) \\ (-2.3841V_{SC}^3 - 3.5761V_{SC}^2 - 1.9301V_{SC} - 0.3263) \cdot 1e10, & (-0.5 < V_{SC} \leq -0.4) \\ (7.1377V_{SC}^3 + 7.8500V_{SC}^2 + 2.6404V_{SC} + 0.2831) \cdot 1e10, & (-0.4 < V_{SC} \leq -0.3) \\ (-4.7536V_{SC}^3 - 2.8521V_{SC}^2 - 0.5703V_{SC} - 0.0380) \cdot 1e10, & (-0.3 < V_{SC} \leq -0.2) \\ 0, & (V_{SC} > -0.2) \end{cases} \tag{4.11}$$

A number of functions have been developed in MATLAB to implement the CNT transistor model based on the cubic spline approximation. The MATLAB function files and their descriptions used to implement the spline approximation based model are listed in Table B.4 in Appendix B.1.1. They can either be applied together as a whole model to analyse the drain current of the CNT transistor, or be used separately to check performance of interior parameters, for example, V_{SC} and the density of states, of the model.

Algorithm 4.1: Numerical Implementation of Cubic Spline Approximation

Input: terminal voltages V_G,V_D,V_S, Fermi level E_F, CNT diameter d, Temperature T, number of cubic spline interval points n and cubic spline boundaries $xmax$, $xmin$

Output: drain current I_{DS}

```
set constants and compute V_SC related parameters;
calculate cubic spline coefficients and form the set of equations 4.10;
for vg = 0 : +0.1 : V_G do
    i = 0;
    I_DS = 0;
    V_DS = V_D − V_S;
    for vd = 0 : 0.01 : V_DS do
        calculate cubic spline coefficients and divide the N_S(V_SC) curve into n − 1
        pieces of 3^rd order splines;
        obtain 3^rd order polynomial and linear equation set from these splines in the
        form of Eq. 4.10;
        every time the terminal voltages (V_G,V_D and V_S) change, compute the voltage
        range in which V_SC belongs to and choose the corresponding spline piece;
        calculate V_SC by invoking the chosen spline equation into Eq. 3.14 and
        compute the drain current I using Eq. 3.19;
        i = i + 1;
        I_DS(i) = I;
    end
end
return I_DS and plot results;
```

The pseudo code describing the implementation of the cubic spline approximaton based model is shown in Algorithm 4.1. The inputs have 9 parameters, including terminal voltages, Fermi levels, CNT diameters, plotting intervals, proposed boundaries of the cubic spline approximation and temperature. Equations representing other parameters used in the calculation of the I-V characteristics are declared, while terminal capacitances C_G, C_D and C_S which can affect the self-consistent voltage are computed. The algorithm then invokes the function to compute the cubic spline coefficients in Eq. 4.7

and calculates the equilibrium mobile charge density of the CNT channel. When all the required parameters are derived, the *For* loops implement the cubic spline algorithm and solve the value of the self-consistent voltage. As long as V_{SC} is calculated, the current through the channel can be computed using Eq. 3.19.

It can be seen from Algorithm 4.1 that the automatic fitting process employed in the piece-wise approximation based models introduced in Chapter 3 has been eliminated. Instead, the more accurate cubic spline approximation is applied. The accuracy of the cubic spline can be adjusted by choosing a different number of interval points. More intervals lead to higher accuracy, but will consume more simulation time. Another advantage of the cubic spline is that the second derivatives of the spline polynomials are set equal to zero at the endpoints of the interval of interpolation, which implies that the inflexion points can be eliminated and the approximation curve is smooth.

4.3 Performance of the Cubic Spline Based Model

Since the self-consistent voltage V_{SC} is calculated from the spline approximation, the evaluation of the drain current poses no numerical difficulty as energy levels U_{SF}, U_{DF} can be found quickly using Eq. 3.19 from Section 3.2.1, Chapter 3. These calculations are direct and therefore considerably fast, as there are no Newton-Raphson iterations or integrations of the Fermi-Dirac probability distribution. For performance comparison, both 3-piece ($n = 4$) and 4-piece ($n = 5$) cubic spline based models were simulated. The model with 4-piece spline approximation was expected to be more accurate but slower than the 3-piece spline based one. Figure 4.2 shows the I_{DS} characteristics of the proposed model with 3-piece spline approximation and FETToy. Table 4.1 shows the average CPU times for both models and those from FETToy [16] and previously reported piece-wise approximation based models [29], while Table 4.2 compares the accuracy of both numerical model types. As can be seen from Tables 4.1 and 4.2, although the proposed spline based model has higher simulation time than the quadratic based model [29], it is still more than two orders of magnitude faster than FETToy [16]. it also achieves better accuracy than the quadratic approximation based model. The

extent to which the modelling accuracy was compromised by numerical approximation was measured by calculating average RMS errors in the simulation, and the results are shown in Table 4.2. As expected, the model based on cubic spline approximation is more accurate than the quadratic based model with errors not exceeding 3% at $T = 300K$ and $E_F = -0.32eV$ throughout the typical ranges of drain voltages V_{DS} and gate bias V_G.

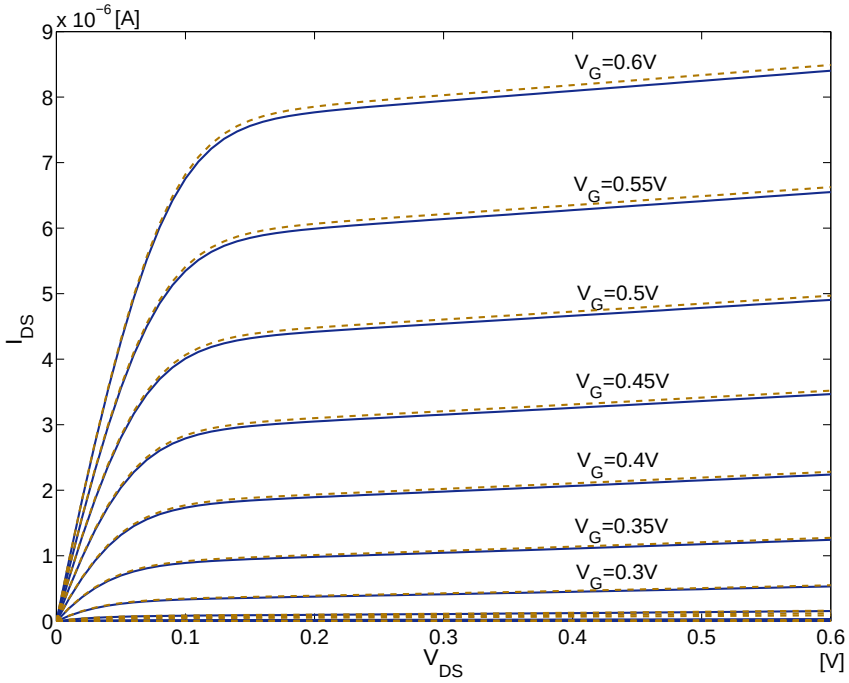

FIGURE 4.2: Drain current characteristics of FETToy [16] (solid lines) and 3-piece cubic spline approximation based model (dashed lines) with $T = 300K$ and $E_F = -0.32eV$.

TABLE 4.1: Average CPU time comparison between FETToy, 3-piece and 4-piece quadratic approximation based models, and spline based models with $n = 4$ and $n = 5$.

Loops	**FETToy**	**3-piece Quadratic Based Model**	**4-piece Quadratic Based Model**	**Spline Based Model n=4**	**Spline Based Model n=5**
5	64.43s	0.02s	0.06s	0.57s	0.95s
10	128.78s	0.04s	0.12s	1.15s	1.91s
50	642.44s	0.19s	0.56s	5.82s	9.59s
100	1287.45s	0.38s	1.12s	11.69s	19.33s

TABLE 4.2: Average RMS errors of I_{DS} of proposed models based on quadratic and cubic spline approximation with $E_F = -0.32eV$ and $T = 300K$.

$V_G[V]$	**3-piece Quadratic Based Model**	**4-piece Quadratic Based Model**	**Spline Based Model n=4**	**Spline Based Model n=5**
0.1	4.4%	3.0%	2.3%	1.9%
0.2	3.6%	2.7%	2.0%	1.8%
0.3	2.7%	2.4%	1.8%	1.6%
0.4	2.9%	2.0%	1.6%	1.5%
0.5	2.6%	2.2%	1.9%	1.7%
0.6	3.2%	2.6%	2.1%	2.0%

Changing temperatures and Fermi levels, the performance of the proposed cubic spline approximation based model under various conditions can be derived. Simulated drain current characteristics of the proposed model at different Fermi levels and temperatures are shown and compared with those of FETToy [16] in Figures 4.3 and 4.4. In both figures dashed lines represent the spline based model and solid lines indicate results obtained from FETToy. The simulation results showed that the drain current increases as the Fermi level and temperature rises, which matches the results of the piece-wise approximation based model developed in Chapter 3.

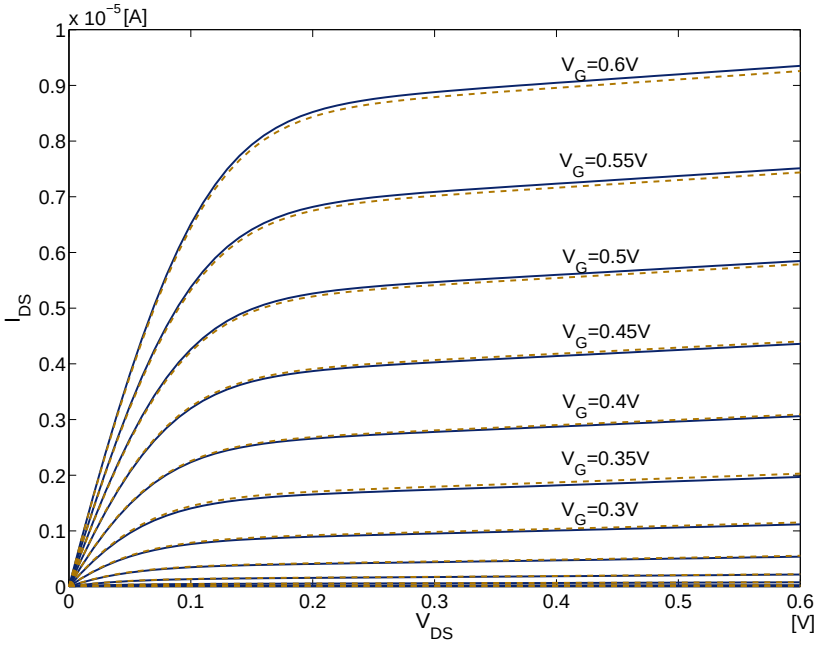

FIGURE 4.3: Drain current characteristics of FETToy [16] (solid lines) and 3-piece cubic spline approximation based model (dashed lines) with $T = 450K$ and $E_F = -0.32eV$.

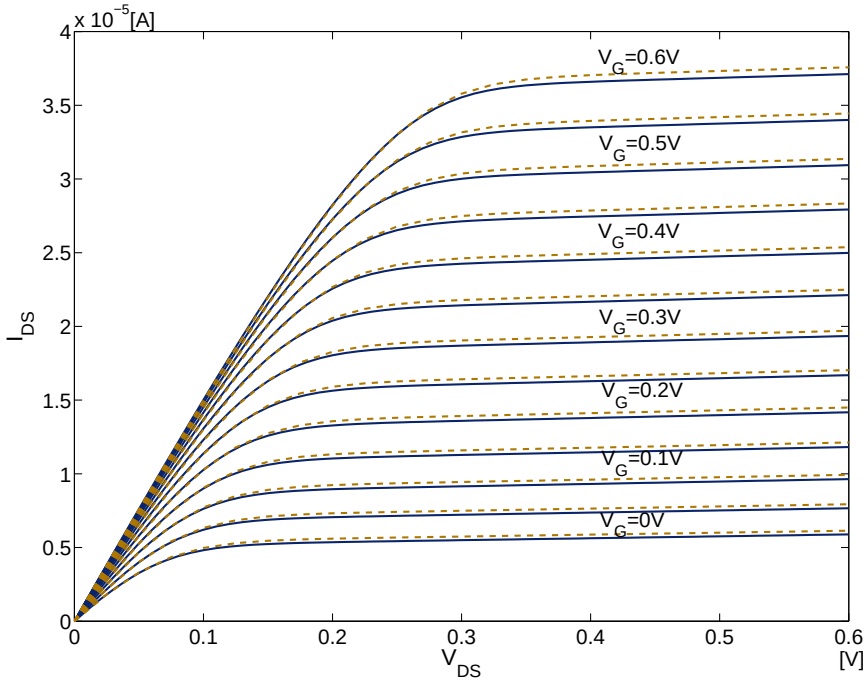

FIGURE 4.4: Drain current characteristics of FETToy [16] (solid lines) and 3-piece cubic spline approximation based model (dashed lines) with $T = 300K$ and $E_F = 0eV$.

The output drain source current characteristics have also been derived and compared for accuracy with the theoretical results generated by FETToy for specific temperature and Fermi level values. Tables 4.3, 4.4 and 4.5 show average RMS errors for both models with different temperatures ($T = 150K, 300K, 450K$) and Fermi levels ($E_F = -0.5eV, -0.32eV, 0eV$). The comparisons show that the numerical approximation used in the fast model causes a slight loss of accuracy, not exceeding 3%.

The performance of the proposed cubic spline based model can be affected by the values of E_F, T, d and terminal voltages V_G,V_D and V_S. The choice of the number of cubic

TABLE 4.3: Average RMS errors of I_{DS} of proposed models based on 3-piece cubic spline approximation with $E_F = -0.32eV$.

$V_G[V]$	150K	300K	450K
0.1	2.5%	2.3%	2.4%
0.2	2.6%	2.0%	1.7%
0.3	2.3%	1.8%	1.9%
0.4	2.1%	1.6%	1.9%
0.5	1.8%	1.9%	2.1%
0.6	2.2%	2.1%	2.3%

TABLE 4.4: Average RMS errors of I_{DS} of proposed models based on 3-piece cubic spline approximation with $E_F = -0.5eV$.

$V_G[V]$	150K	300K	450K
0.1	2.7%	2.5%	2.5%
0.2	2.5%	2.8%	2.4%
0.3	2.2%	2.6%	2.2%
0.4	2.2%	2.4%	2.0%
0.5	2.7%	2.3%	2.5%
0.6	2.9%	2.2%	2.1%

TABLE 4.5: Average RMS errors of I_{DS} of proposed models based on 3-piece cubic spline approximation with $E_F = 0eV$.

$V_G[V]$	150K	300K	450K
0.1	2.6%	2.2%	2.1%
0.2	2.3%	2.0%	1.7%
0.3	2.2%	2.1%	1.9%
0.4	1.9%	1.8%	1.9%
0.5	2.0%	2.1%	1.8%
0.6	2.2%	1.8%	1.6%

spline approximation pieces is a clear trade-off between speed and accuracy as more operations need to be performed with more pieces while the shape of the mobile charge curve is reflected more accurately. From simulation results of this research, it is suggested that 3-piece cubic spline ($n = 4$) is a balanced choice for the spline based model, for the approximated splines can match the theoretical $N_S(V_{SC})$ curve very closely and the simulation speed with 3-piece approximation is fairly high. With more pieces of splines, more simulation time will be required, but the increase of accuracy is limited, which means a large number of spline pieces is not necessary for the proposed spline based model.

4.4 VHDL-AMS Implementation and Simulation of the Cubic Spline Based Model

So far, the implementation of the proposed ballistic CNT transistor models based on piece-wise and cubic spline approximation has been carried out using numerical methods.

To verify the performance of the models in circuit design, behavioural-level implementation is preferred. The VHDL-AMS standard was created to enable designers of mixed signal systems and integrated circuits to create and use modules that encapsulate high-level behavioural descriptions [52].

The numerical cubic spline algorithm has been used to implement both n-type and p-type CNT transistor models in VHDL-AMS and to simulate CNT based logic circuits. A number of functions in VHDL-AMS were created to implement the proposed CNT transistor model. Table B.4 in Appendix B.2 lists the functions and their descriptions used in the model. This model has been verified using Mentor Graphics SystemVision Professional 4.4 and 5.5.

Algorithm 4.2 indicates the functional relations of the VHDL-AMS files. It can be seen that the top function *CNTTransistor.vhd* invokes relevant functions to fulfill the cubic spline algorithm.

Algorithm 4.2: VHDL-AMS Implementation of the Proposed Cubic Spline Based CNT Transistor Model

Input: V_G,V_D,V_S,E_F,d,n and T
Output: I_{DS}

1 define I/O ports of the proposed model in the top level function module;
2 set parameters, including the cubic spline range and the number of intervals;
3 apply the cubic spline method and divide the $N_S(V_{SC})$ curve into $n-1$ pieces of 3^{rd} order splines, then obtain 3^{rd} order polynomial equation set from these splines in the form of Eq. 4.10;
4 for different V_G,V_D and V_S, compute the range in which V_{SC} belongs to and choose the corresponding spline piece;
5 calculate V_{SC} by invoking the chosen spline equation into Eq. 3.14 and compute the drain current I_{DS} using Eq. 3.19;
6 return I_{DS};

To use the VHDL-AMS model properly, the coefficient list file (coefficient.vhd) has to be generated first from $Fsy.m$ in MATLAB (see Appendix B.2). When running simulation, each subordinate function should be loaded using the following statement.

```
library work;
use work.SolveVscEquation_pack.all;
use work.FindQRange_pack.all;
use work.coeff_pack.all;
```

In the top level function *CNTtransistor.vhd* of the developed VHDL-AMS model, the port definitions of drain, gate, source, and bulk are the same as for a typical MOS transistor model, which is shown in Listing 4.1. In this listing, the libraries and loaded function packages are included in lines 1-6. The generic and I/O ports of the developed model are defined in lines 8-17. Lines 21-33 define the properties of the I/O parameters of the model.

```
1   library IEEE;
2   use IEEE.math_real.all;
3   use IEEE.electrical_systems.all;
4
5   library work;
6   use work.cntcurrent.all;
7
8   entity CNTTransistor is
9     generic( -- model parameters
10        T : real := 300.0;
11            dcnt: real := 1.0E-9;
12            Ef_i: real := -0.32*1.6E-19
13           );
14
15    port (terminal drain, gate, source,
16          bulk: electrical
17         );
18
19  end entity CNTTransistor;
20
21  architecture Characteristic of CNTTransistor is
22
23  --terminal voltages and drain current
24  quantity Vdi across drain to bulk;
25  quantity Vgi across gate to bulk;
26  quantity Vsi across source to bulk;
27  quantity Ids through drain to source;
28
29  begin
30
31  Ids == Fcnt(Vgi, Vsi, Vdi, Ef_i, T, dcnt);
32
33  end architecture Characteristic;
```

LISTING 4.1: Top level module of the proposed cubic spline based CNT transistor model in VHDL-AMS

In the developed behavioural-level CNT transistor model based on the cubic spline approximation, the bulk voltage was considered to take into account the effects of the charge densities generated by the substrate voltage. This is especially important for the p-type transistor, because the bulk usually links to the source terminal voltage. Figure 4.5 shows I_{DS} characteristics of the n-type transistor implemented in VHDL-AMS which closely match the MATLAB simulation result shown in Figure 4.2.

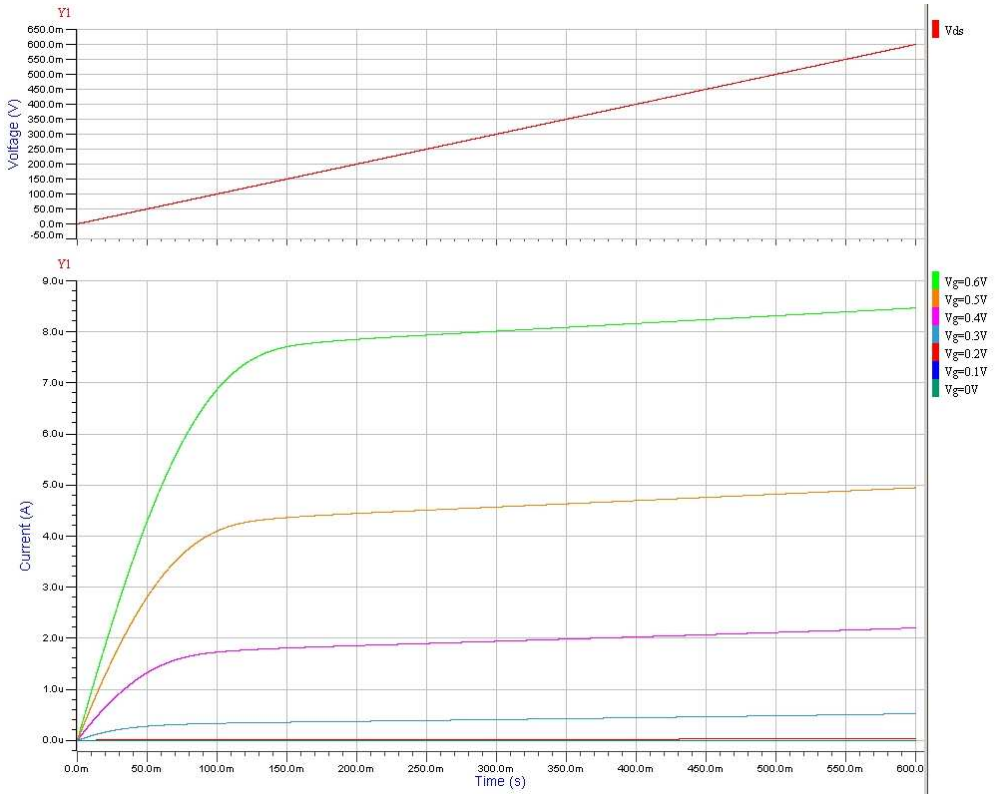

FIGURE 4.5: Simulated drain current of the proposed VHDL-AMS CNT transistor model based on 3-piece cubic spline approximation of mobile charge densities with $T = 300K$, $d = 1nm$ and $E_F = -0.32eV$.

To develop a complementary logic inverter model, both n-type and p-type CNT transistors were employed. The schematic of the inverter is shown in Figure 4.6. The VHDL-AMS testbench code of the inverter based on the developed CNT transistor model is given in Listing 4.2. The testbench invokes the two transistors (lines 18-24) as well as a ramp voltage source (lines 16-17) and a constant voltage source (lines 14-15). The constant source provides the supply voltage V_{CC} for the gate, while the ramp source is used to produce the output characteristic of the inverter. Lines 25-27 describe a capacitor as the load of the inverter. The simulation result is shown in Figure 4.7. Considering that the transport characteristics of both transistors are not the same, it is worth noting that

the inverter output is not symmetrical at $V_{CC}/2$ due to the stronger n-type transistor.

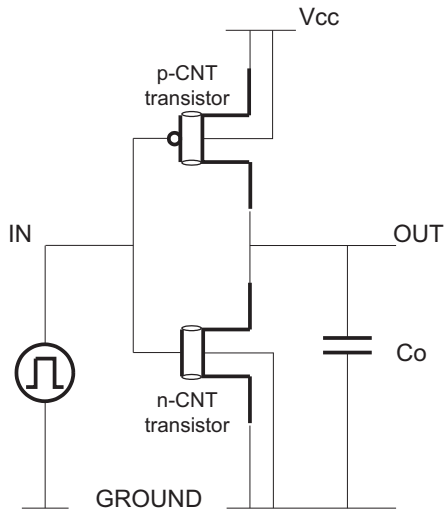

FIGURE 4.6: Schematic of the simulated CNT based inverter in VHDL-AMS.

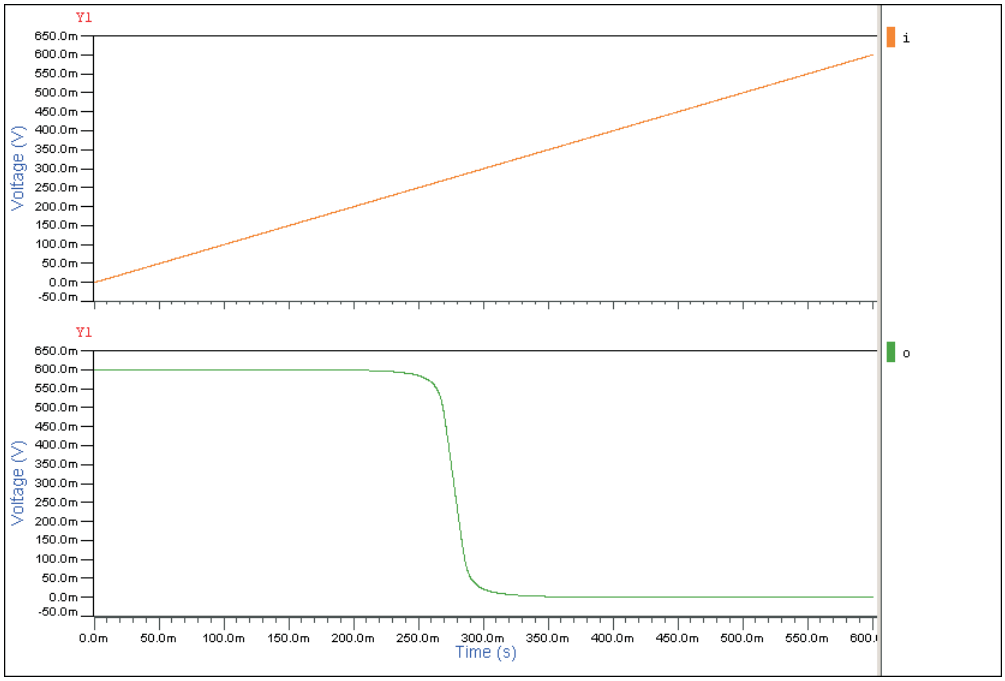

FIGURE 4.7: CNT based inverter simulation result: input ramps from $0V$ to $0.6V$.

```
-- Inverter Testbench

1  library IEEE;
2  use IEEE.math_real.all;
3  use IEEE.electrical_systems.all;
4
5  entity test_CNTTransistor is
6  end entity test_CNTTransistor;
7
8  architecture test of test_CNTTransistor is
9    terminal g,i,o: electrical;
10   alias ground is ELECTRICAL_REF;
11
12 begin
13
14 vc: entity v_source generic map (lv=>0.6)
15                     port map (po=>g, ne=>ground);
16 vi: entity v_pulse  generic map (pulse=>1.0,tchange=>1sec)
17                     port map(po=>i,ne=>ground);
18 ntransitor: entity CNTTransistor
19           generic map (Ef_i=>0.32*1.6E-19)
20           port map (drain=>o,gate=>i,source=>g,bulk=>g);
21 ptransistor: entity CNTTransistor
22         generic map (Ef_i=>-0.32*1.6E-19)
23         port map (drain=>o,gate=>i,source=>ground,
24                   bulk=>ground);
25 Co: entity capacitor
26     generic map(1.0E-6) -- 1uF
27     port map(o,ground);
28
29 end architecture test;
```

LISTING 4.2: Testbench of a logic inverter using the proposed cubic spline based CNT transistor model in VHDL-AMS

More complex logic circuits using the developed CNT transistor model have been constructed and simulated. A typical full adder with the circuit schematic as shown in Figure 4.8 has been implemented in VHDL-AMS and simulated using SystemVision 4.4. Sum and carry functions of the adder are represented in Equations 4.12 and 4.13.

$$S = (A \bigoplus B) \bigoplus C_{in} \tag{4.12}$$

$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \bigoplus B)) \tag{4.13}$$

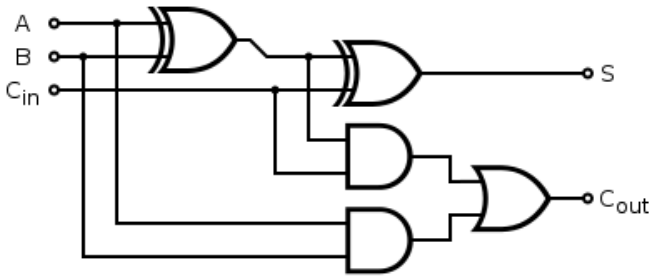

FIGURE 4.8: Schematic of 1-bit full adder.

A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting C_{in} to the other input and OR the two carry outputs. Figure 4.9 shows the simulated logic performance of the 1-bit full adder based on the cubic spline CNT transistor models. As can be seen from this figure, the 1-bit adder functions correctly as the Equations 4.12 and 4.13 predict.

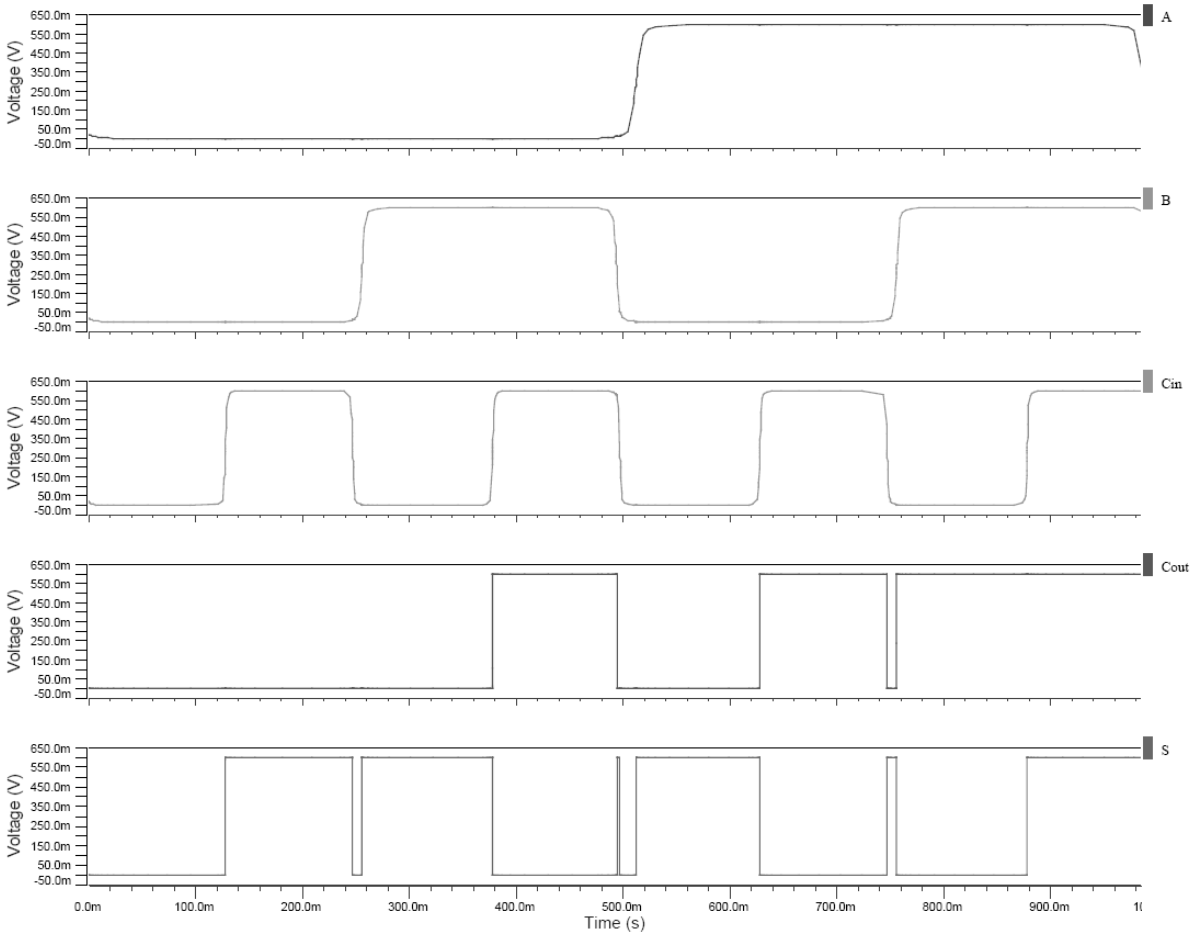

FIGURE 4.9: Simulation results of the CNT based 1-bit full adder in VHDL-AMS.

4.5 Concluding Remarks

The aim of this chapter was to develop a new technique to automatically generate the numerical approximation of the mobile charge density of CNT transistors, which overcame the fitting process disadvantage existing in the numerical piece-wise approximation techniques developed in Chapter 3. This chapter explained the cubic spline algorithm and how it can be employed in the approximation of the CNT charge density. Furthermore, the chapter described the numerical implementation of the cubic spline approximation based CNT transistor model and emphasised that the cubic spline approximation could fulfill the fitting process automatically. DC simulation results showed that the developed spline based model can achieve a simulation speed-up of up to two orders of magnitude compared with FETToy [16] with RMS errors of less than 3%. To verify the feasibility of the developed spline approximation based model at behavioural level, VHDL-AMS implementation for both n-type and p-type transistors was obtained and used to simulate their I_{DS} characteristics. Logic circuits including inverters and adders based on the bahavioural-level CNT transistor model functioned correctly in simulation.

Chapter 5

Modelling of Non-ballistic Transport Effects of CNT Transistors

In Chapters 3 and 4, it was demonstrated that numerical piece-wise and cubic spline approximation of mobile charge densities leads to efficient solutions of ballistic transport of CNT transistors. Ballistic CNT transistor models were developed using MATLAB and VHDL-AMS, and simulation results of the implemented models match the theoretical prediction [16] well. However, the transport mechanism of CNT transistors is complicated and the existence of non-idealities may result in non-ballistic transport characteristics. In this chapter, a number of transport mechanisms that lead to non-ballistic behaviour will be discussed and the implementation of these effects will be described.

In Section 5.1, four non-ballistic transport effects will be described. Equations representing these effects will be shown and the influence of each effect will be illustrated in simulation. In addition, FETToy models with non-ballistic transport which contain these non-ballistic effects will be introduced in this section. Section 5.2 describes the numerical implementation of the model with non-ballistic effects, named *FETToy+*. Also, simulation results obtained from the extended FETToy model with non-ballistic effects and *FETToy+* will be compared. The proposed non-ballistic CNT transistor model is

compared with experimental results in Section 5.3. Section 5.4 provides a conclusion to this chapter.

5.1 Non-ballistic Transport of CNT Transistors and FET-Toy with Non-Ballistic Effects

Research into non-ballistic transport in carbon nanotubes has recently yielded results and some new theories have been reported. The transport type in carbon nanotubes, ballistic or non-ballistic, depends on the energy region. For a CNT transistor with length smaller than the carrier mean free path but larger than the Coulomb blockade length, ballistic transport will dominate. The charging and discharging decides the maximum differential conductance through single transport channels, and the energy of the hole in a nanotube E is directly determined by the terminal voltage V_{DS}. In contrast, for non-ballistic CNT transistors, this transmission coefficient fluctuation could be caused by mobility fluctuation. Under the effects of scattering, E can become much smaller than qV_{DS} in the case. It has also been shown that a mismatch of helicity between adjacent shells may result in a short mean free path [154]. The band gap may also be tuned due to the strain on the nanotube [155]. Furthermore, defects including vacancies, contamination, contact with the substrate, and adsorbed molecules may cause non-ballistic transport [154]. In the light of these results, the non-ballistic transport of CNT transistors is likely to attract more research attention in the near future. Four non-ballistic effects, including elastic scattering, strain effect, tunnelling effect and phonon scattering, are outlined and implemented in spline based CNT transistor models.

5.1.1 Elastic Scattering

The elastic scattering mechanism in the CNT channel region affects the channel resistance and therefore causes a potential drop in the channel voltage. Assuming that the mean free path (MFP) l_{eff} is proportional to the diameter of the nanotube [156, 157], which is $l_{eff} = d/(d_0)\lambda_{eff}$, where d_0 is the reference diameter when λ_{eff} is the elastic-scattering mean free path [14], the transmission probability in the elastic-scattering

channel region can be expressed using $T_{eff} = l_{eff}/(L + l_{eff})$, where d is the CNT diameter, $\lambda_{eff} \approx 200nm$ [158] and L is the channel length. The channel potential drop can hereby be derived from Eq. 5.1.

$$V_{DSeff} = \frac{L}{L + \frac{d}{d_0} \cdot \lambda_{eff}} V_{DS} \tag{5.1}$$

The contribution to the device current characteristics can be computed directly from the variable voltage V_{DSeff} due to the elastic scattering instead of the channel resistance, which efficiently simplifies the calculation [14]. Figure 5.1 illustrates how the drain current changes when the elastic scattering effect relating to the channel length is considered.

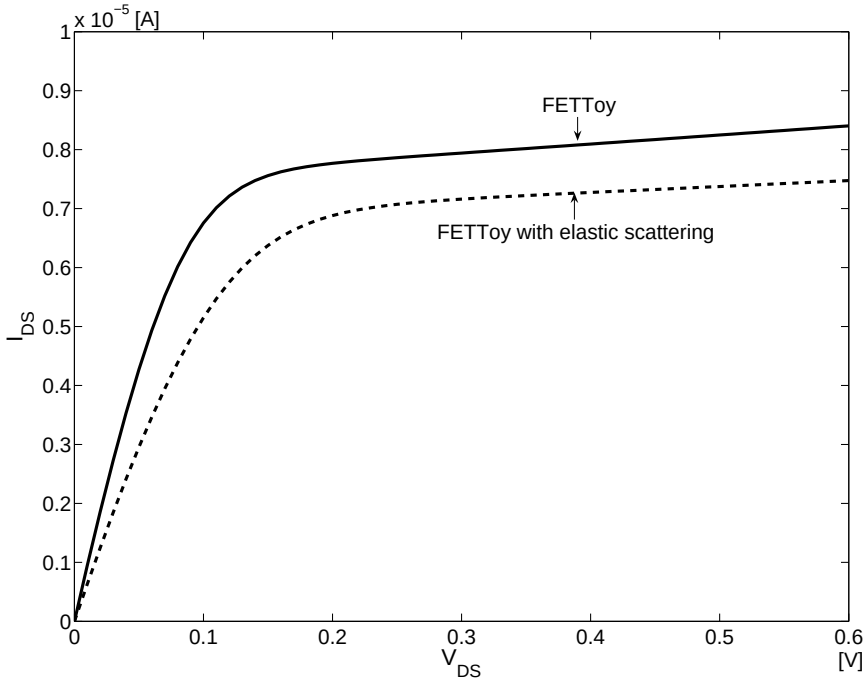

FIGURE 5.1: Comparison of the drain current between models with and without the elastic scattering effect with $V_G = 0.6V, T = 300K$, $E_F = -0.32eV$ and $L = 300nm$: the extended FETToy model (dashed line) with elastic scattering described in Section 5.1.5 and ballistic FETToy model [16] (solid line).

5.1.2 Band Gap Tuning with Strain

It has been demonstrated that the transport properties of a CNT can vary under strain [155, 159]. Experimental measurement has shown that the strain exerted onto a nanotube can change the band gap and thus affect the transport characteristics. The shape distortion formed by the strain can be treated as a key factor when calculating the extra band gap caused by the effect. Eq. 5.2 indicates the influence of the strain effect on the band gap of CNTs:

$$E_{geff} = E_g + \frac{dE_{gstrain}}{d\chi}\chi \tag{5.2}$$

where E_{geff} is the effective band gap under strain, $dE_{gstrain}$ is the gap shift due to the strain and χ is defined as the distortion factor under strain. It has also been indicated that the change rate of the band gap $\frac{dE_{gstrain}}{d\chi}$ in the light of strain is chirality dependent, which can be computed using Eq. 5.3.

$$\frac{dE_{gstrain}}{d\chi} = 3\sigma(1+r_0)sign(2p+1)cos(3\phi) \tag{5.3}$$

In this equation, σ is the overlap integral of the tight-binding C-C model, with a value of circa $2.7eV$, $r_0 \approx 0.2$ is the Poisson's ratio, ϕ is the chiral angle of the nanotube and p comes from the CNT chirality: for a CNT with the chirality (m, n), $m - n = 3l + p$, where l and p are both integrals [155]. It is indicated that the chirality and strain can both influence the band gap of a CNT and the total gap E_{geff} could be either larger or less than the ideal diameter-based calculation E_g, which might cause the transport to decrease or increase respectively. Figure 5.2 illustrates that when under certain strain conditions ($\chi = 0.1$, $p = 1$ and $\phi = 20^o$) the drain current is reduced due to the band gap variation.

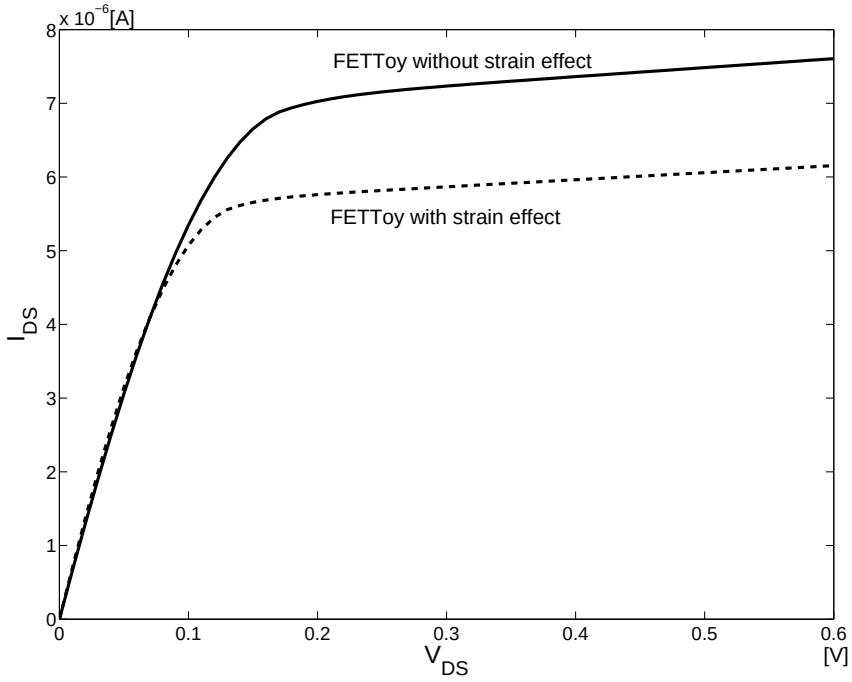

FIGURE 5.2: Comparison of the drain current between models with and without strain effect with $V_G = 0.6V, T = 300K$, $E_F = -0.32eV$ and $L = 300nm$: the extended FETToy model (dashed line) with strain effect and ballistic FETToy model [16] (solid line).

5.1.3 Tunnelling Effect

The tunnelling effect is inevitable in the subthreshold region, which may lower the self-consistence potential and thereby worsen the threshold characteristics of the transistor. One simplified method to describe the tunnelling effect is to introduce a parameter T_t, called the tunnelling probability [13, 160], which is calculated using Eq. 5.4:

$$T_t \approx \frac{\pi^2}{9} e^{-\frac{\pi\sqrt{m^* E_g^3}}{\sqrt{8}q\hbar F}} \tag{5.4}$$

where F is a parameter which triggers the tunnelling under high electrical field and m^* is the effective electron mass [13]. The tunnelling current then can be obtained by T_t timing the maximum possible tunnelling current as represented in Eq. 5.5.

$$I_t = \frac{4qkT}{h} T_t \sum_{m=1}^{M} [ln(1 + e^{(qV_{DSeff} - E_{geff}/2 - E_F)/kT}) - ln(1 + e^{(qV_{DSeff} - E_F)/kT})] \frac{max(qV_{DSeff} - E_{geff}, 0)}{qV_{DSeff} - E_{geff}} \tag{5.5}$$

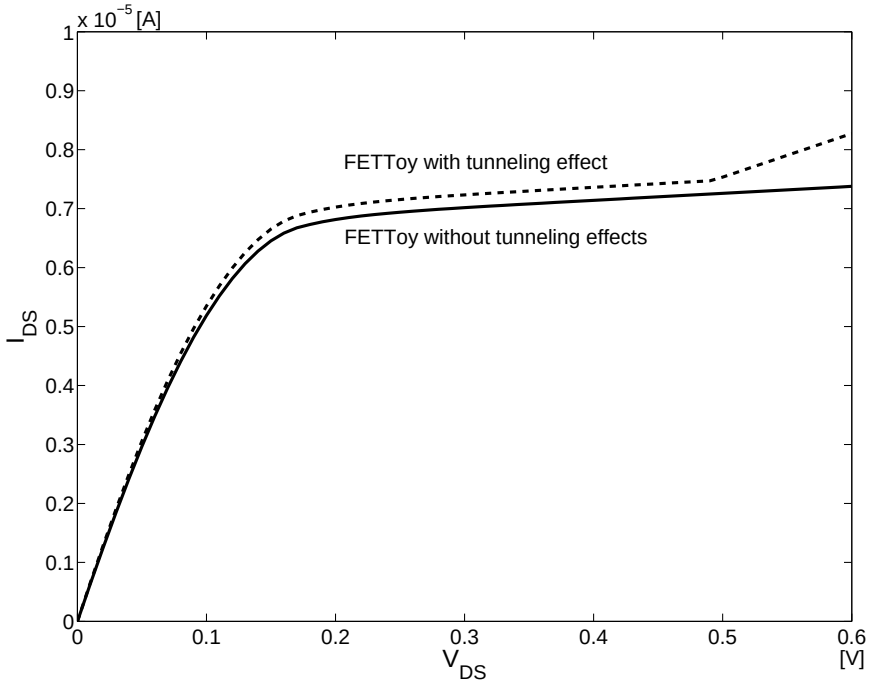

FIGURE 5.3: Comparison of the drain current between models with and without tunnelling effect with $V_G = 0.6V, T = 300K$, $E_F = -0.32eV$ and $L = 300nm$: the extended FETToy model (dashed line) with tunnelling effect and ballistic FETToy model [16] (solid line).

It can be noticed from Figure 5.3 that the tunnelling current has increased the total drain current throughout the V_{DS} range, but the effect becomes significant when the channel voltage exceeds a certain turning point depending on the CNT transistor coefficients including V_{DSeff} and E_{geff} in Eq. 5.5.

5.1.4 Phonon Scattering

For semiconducting carbon nanotubes, scattering effects are related to the band energy. The effective phonon scattering mean free path in a semiconducting nanotube can be computed by Eq. 5.6:

$$\begin{aligned}\frac{1}{l_{sc}(V_x)} = \frac{1}{l_{ap}}\left[1 - \frac{1}{1+e^{(E_F - qV_{SC} + qV_x)/kT}}\right] \\ + \frac{1}{l_{op}}\left[1 - \frac{1}{1+e^{(E_F - qV_{SC} - \hbar\omega_{op} + qV_x)/kT}}\right]\end{aligned} \tag{5.6}$$

where $l_{ap} = 500nm$ is a typical acoustic phonon scattering MFP value while $l_{op} = 15nm$ is a typical optical phonon scattering MFP, and $\hbar\omega_{op} \approx 0.16eV$ is a typical OP energy [129, 161, 162]. It can be noticed that at low carrier energy (e.g. $< 0.15eV$), the acoustic scattering dominates, while the optical scattering is more important at high kinetic energy.

$$T_S = \frac{l_{sc}(0)}{l_{sc}(0) + L} \tag{5.7}$$

$$T_D = \frac{l_{sc}(V_{DSeff})}{l_{sc}(V_{DSeff}) + L} \tag{5.8}$$

$$\begin{aligned}I_{DS_p} = \frac{2qkT}{\pi\hbar}[T_S ln(1 + e^{\frac{E_F - qV_{SC}}{kT}}) \\ - T_D ln(1 + e^{\frac{E_F - q(V_{SC} + V_{DSeff})}{kT}})]\end{aligned} \tag{5.9}$$

Equations 5.7, 5.8 and 5.9 describe the scattering effects on the I-V characteristics. Figure 5.4 illustrates that the phonon scattering effects may limit the transport capability of carriers in the channel and hence restrain the drain current. Different from Eq. 3.15, the scattering coefficients T_S and T_D are introduced in Eq. 5.9 which indicates the effects of the phonon scattering. The modelling of the scattering processes is of importance for circuit design, since neglecting the scattering leads to an overestimation of more than 70% of the main figures of merit [162].

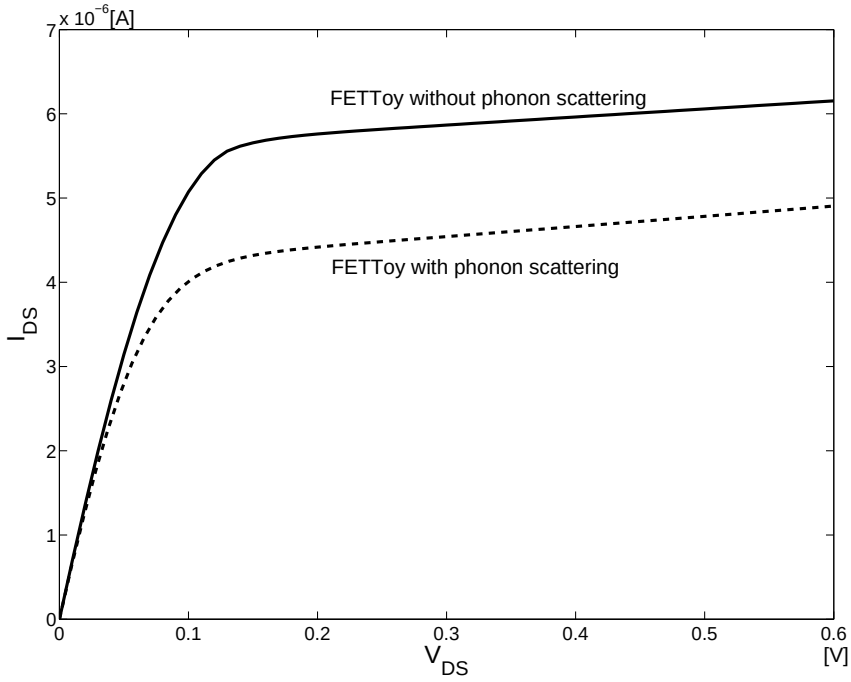

FIGURE 5.4: Comparison of the drain current between models with and without phonon scattering with $V_G = 0.6V, T = 300K$, $E_F = -0.32eV$ and $L = 300nm$: the extended FETToy model (dashed line) with phonon scattering and ballistic FETToy model [16] (solid line).

5.1.5 Implementation of FETToy with Non-Ballistic Transport Effects

As described in Sections 5.1.1-5.1.4, non-ballistic transport mechanisms are widespread in CNT transistors. For the purpose of predicting the performance of a CNT transistor with non-ballistic transport characteristics, a model is developed based on the ballistic FETToy [16] model. FETToy is based on theoretical equations derived from physical phenomena, and thus its performance is accurate. However, solving the theoretical equations is slow process.

To develop a non-ballistic CNT transistor model based on theoretical analysis, the initial FETToy model is modified by adding numerical expressions of non-ballistic effects. Algorithm 5.2 indicates the implementation of the extended FETToy model which is capable of describing the non-ballistic transport performance of CNT transistors. The extended FETToy incorporates the following non-ballistic effects: elastic scattering, band gap tuning with strain, tunnelling effect and phonon scattering.

Functional files to numerically implement the FETToy model with non-ballistic trans-

Algorithm 5.1: Numerical Implementation of FETToy with non-ballistic effects

Input: Initial Voltage V_I, Final Voltage V_F, number of bias points NV, Fermi level E_F, CNT diameter d, Temperature T, insulator thickness t, Channel Length L and CNT chiral angle ϕ

Output: drain current I_{DS}

1 set physical constants and compute V_{SC} related parameters;
2 define parameters for non-ballistic effects introduced in Sections 5.1.1-5.1.4;
3 add non-ballistics effects by numerically implementing Equations 5.1-5.9 in the model, which will affect V_{SC} and I_{DS};
4 for different terminal voltages, apply the Newton-Raphson method and integral to compute calculate V_{SC} from Eq. 3.14 and compute the drain current I_{DS} using Eq. 3.19;
5 return I_{DS} and plot results;

port effects in MATLAB have been listed in Appendix B.1.2 with instructions. With the traditional iterative calculation of V_{SC}, FETToy with non-ballistic effects suffers from CPU time inefficiency since it relies on the solution algorithm implemented in the original FETToy. The main purpose of developing this enhanced FETToy model is to obtain reference results for the model named $FETToy+$, which is a non-ballistic CNT transistor model based on cubic spline approximation of mobile charge densities of CNT transistors. $FETToy+$ is introduced in the following section.

5.2 Non-Ballistic Effects in Cubic Spline Approximation Based CNT Transistor Model (*FETToy+*)

It was stated earlier that the extended FETToy model with non-ballistic effects is similar to the original ballistic FETToy model and employs iterative computation when calculating the transport current within the CNT channel, and thus is slow. Following the development of a fast numerical ballistic CNT transistor model based on cubic spline approximation of mobile charge densities in Chapter 4, this spline approximation based model is extended by adding non-ballistic transport effects. The developed model, named $FETToy+$, is capable of predicting both the ballistic and the non-ballistic performance of a CNT transistor, while maintaining fast simulation time and high accuracy by taking advantage of the cubic spline algorithm. Considering that non-ballistic effects are modelled by adding numerical equations which are straightforward and can be solved

quickly, the extension of non-ballistic transport effects does not increase significantly the CPU cost of the model.

5.2.1 MATLAB Implementation of *FETToy+*

For an ideal model with no non-ballistic effects, once the self-consistent voltage V_{SC} is calculated from the closed-form solutions of Eq. 3.14 in Chapter 3 after the approximation which yields only linear, quadratic or 3^{rd} order polynomial relations, the total drain current can be directly obtained from equations 3.9, 3.10 and 3.15. However, when non-ballistic transport features are considered, a more complicated model which includes additional coefficients and equations is needed. To clarify the effects of non-ballistic transport characteristics, separate simulations were carried out for both ideal and non-ballistic scenarios and their results were compared.

The implementation of the numerical non-ballistic CNT transistor model in MATLAB is similar to that of the ballistic model introduced in Chapter 4. Both models are based on the cubic spline approximation of the mobile charge densities. However, the new model takes into account non-ballistic transport effects in CNT channels and generally it can be implemented by adding the non-ballistic effects described in Section 5.1 into the ballistic spline approximation based model introduced in Chapter 4.

Algorithm 5.2 shows the functional structure of the numerical implementation of the developed CNT transistor model with non-ballistic effects. As described in lines 12-13, the non-ballistic transport effects mentioned in Sections 5.1.1-5.1.4 are changed into numerical equations and added into the new model. For example, the elastic effect has been implemented using the following expressions:

```
VDS=VD-VS;
Leff= d0/1.5e-9*L0;
Vch=L/(L+Leff)*VDS;
```

Adding Equations 5.1, 5.2, 5.5 and 5.9 to the cubic spline based CNT transistor model, the extended non-ballistic CNT transistor model *FETToy+* [163] which includes the

Algorithm 5.2: Numerical Implementation of *FETToy+* Model with Non-Ballistic Effects

Input: terminal voltages V_G,V_D,V_S, Fermi level E_F, CNT diameter d, Temperature T, number of cubic spline approximation pieces n, cubic spline boundaries $xmax$, $xmin$, Channel Length L and CNT chiral angle ϕ

Output: drain current I_{DS}

```
set constants and compute V_SC related parameters;
define parameters for non-ballistic effects introduced in Section 5.1;
calculate cubic spline coefficients and form the set of equations 4.10;
for vg = 0 : +0.1 : V_G do
    i = 0;
    I_DS = 0;
    V_DS = V_D − V_S;
    for vd = 0 : 0.01 : V_DS do
        calculate cubic spline coefficients and divide the N_S(V_SC) curve into n pieces of 3^rd order splines;
        obtain 3^rd order polynomial equation set from these splines in the form of Eq. 4.10;
        for various terminal voltages V_G,V_D and V_S, compute the range in which V_SC belongs to and choose the corresponding spline piece;
        numerically implement the non-ballistic effects described by Equations 5.1-5.9;
        add these equations into the numerical model, which will affect the V_SC and thus the drain current I_DS;
        calculate V_SC by invoking the chosen spline equation into Eq. 3.14 and compute the drain current I_DS using Eq. 3.19;
    end
end
return I_DS and plot results;
```

following four non-ballistic effects, elastic scattering, strain effect, tunnelling effect, and phonon scattering, has been developed. Figure 5.5 shows the comparison of drain current between ballistic FETToy [16], extended FETToy with non-ballistic effects introduced in Section 5.1.5, and the proposed *FETToy+* with the four non-ballistic transport effects. As can be seen in Figure 5.5, there is close agreement between the DC performance of *FETToy+* and that of FETToy extended with non-ballistic transport effects. MATLAB functional files to numerically implement the *FETToy+* model are listed in Appendix B.1.3 with instructions.

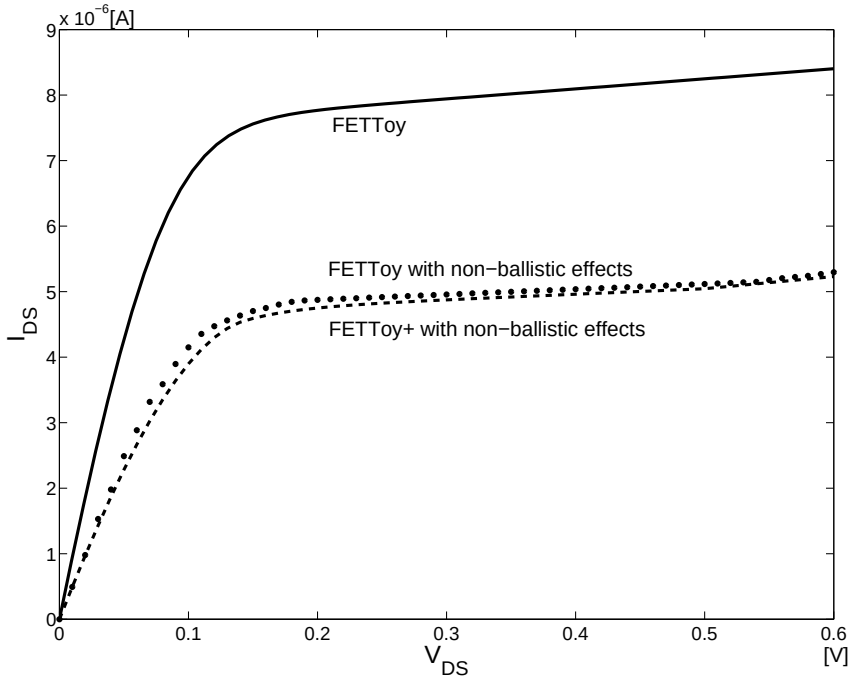

FIGURE 5.5: Comparison of the drain currents between ballistic FETToy (solid line), FETToy with non-ballistic effects (dotted line) and *FETToy+* (dashed line) models with $L = 300nm$, $dcnt = 1nm$, $E_F = -0.32eV$ and $T = 300K$ at $V_G = 0.6V$.

5.2.2 Performance of *FETToy+*

When taking into account the four non-ballistic effects, including elastic scattering, strain effect, tunnelling effect, and phonon scattering, described in sections 5.1.1, 5.1.2, 5.1.3 and 5.1.4, the original cubic spline based CNT transistor model, which implements the purely ballistic transport theory as introduced in Chapter 4, cannot be used as a reference for accuracy and speed analysis. However, by adding Equations 5.1, 5.2, 5.5 and 5.9 to the MATLAB scripts of the developed ballistic CNT transistor model based on spline approximation, an extended model named *FETToy+* [163] which is capable of analysing both the ballistic and the non-ballistic performance of CNTs is developed. Similarly, the FETToy with non-ballistic effects model has extended the theoretical ballistic FETToy model [16] to include the non-ballistic effects. The simulation results from Section 5.1 illustrate that the drain current may be reduced due to the presence of non-ballistic effects. Two spline based non-ballistic CNT transistor models called Model C and Model D with number of spline intervals $n = 4$ and $n = 5$ respectively were simulated. Figure 5.6 and 5.7 respectively show the simulated drain current of FETToy

with non-ballistic effects and both the *FETToy+* models with different numbers of cubic spline pieces. As can be seen from the figures, there is a good correlation between the ballistic FETToy model and *FETToy+*.

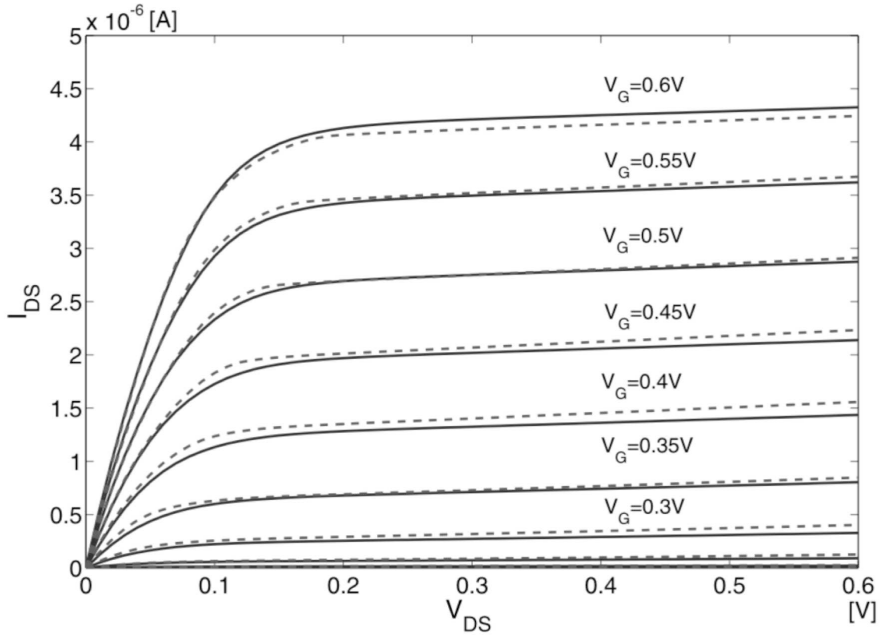

FIGURE 5.6: Drain current characteristics of FETToy with non-ballistic transport (solid lines) and *FETToy+* Model C (dashed lines) with $T = 300K$, $E_F = -0.32eV$, $d = 1nm$ and $L = 300nm$.

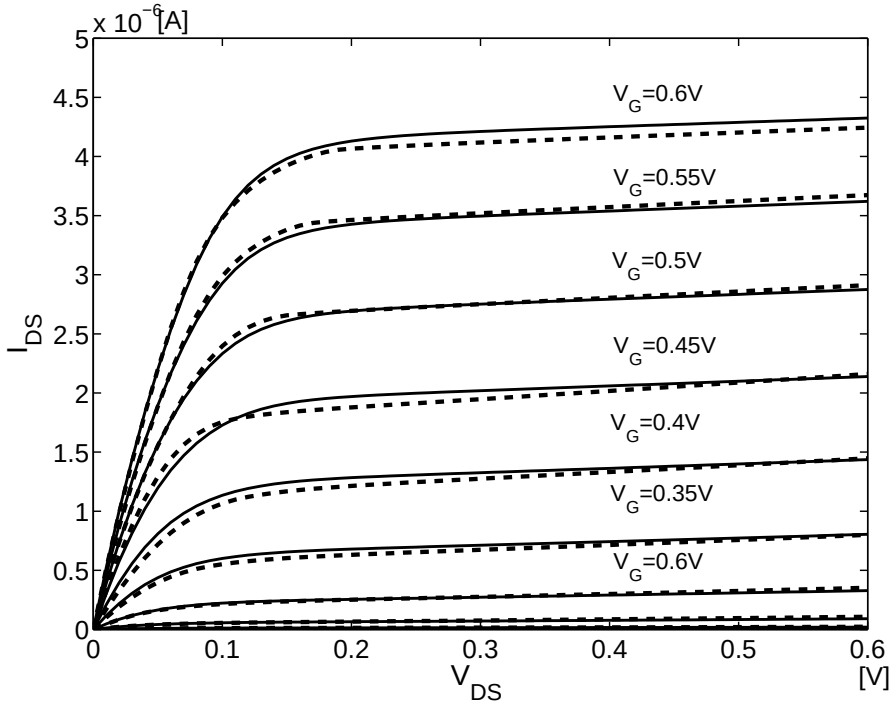

FIGURE 5.7: Drain current characteristics of FETToy with non-ballistic transport (solid lines) and *FETToy+* Model D (dashed lines) with $T = 300K$, $E_F = -0.32eV$, $d = 1nm$ and $L = 300nm$.

The accuracy and the simulation speed of the *FETToy+* models (Model C and D) were measured and compared with those of FETToy with non-ballistic effects, and results are listed in Table 5.1. As expected, the non-ballistic models require more CPU time than the ballistic models since more calculation is required. Although Model D, with more spline approximation pieces, achieves slightly higher accuracy than Model C, it requires more simulation time.

TABLE 5.1: Maximum drain current RMS errors and average CPU time of the proposed *FETToy+* model compared with FETToy.

FETToy with non-ballistic effects CPU time	**FETToy+ model**	**Max RMSE**	**CPU time**
2261s	**Model C**	2.9%	13.4s
	Model D	2.5%	22.8s

The drain current of the proposed *FETToy+* model with various Fermi levels and temperatures was also simulated. Figures 5.8 and 5.9 illustrate that, with higher temperature and Fermi level, the drain current of non-ballistic transistors increases, which matches the simulation results of ballistic CNT transistor models derived in Chapters 3 and 4.

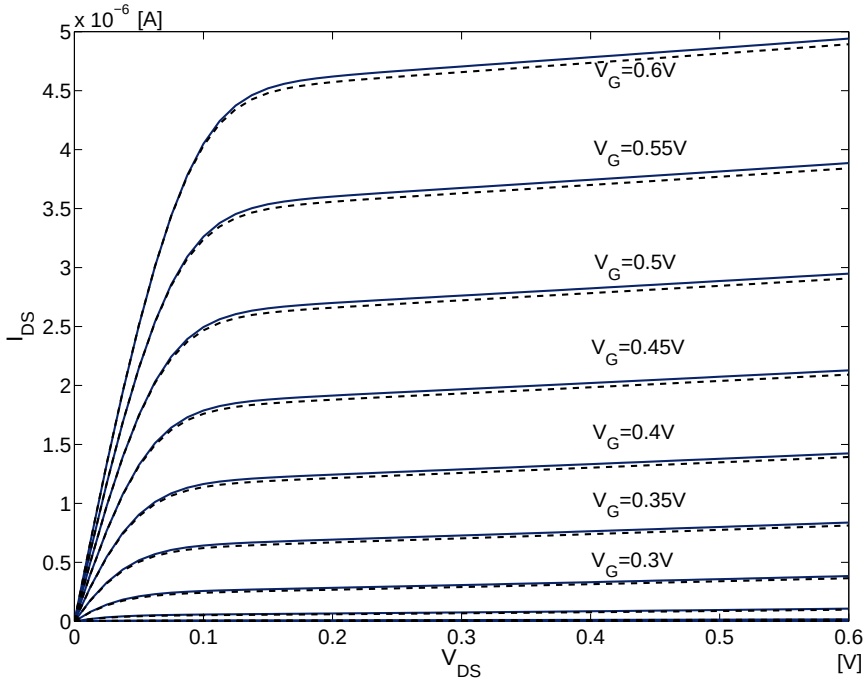

FIGURE 5.8: Drain current characteristics of FETToy with non-ballistic transport (solid lines) and *FETToy+* Model D (dashed lines) with $T = 450K$, $E_F = -0.32eV$, $d = 1nm$ and $L = 300nm$.

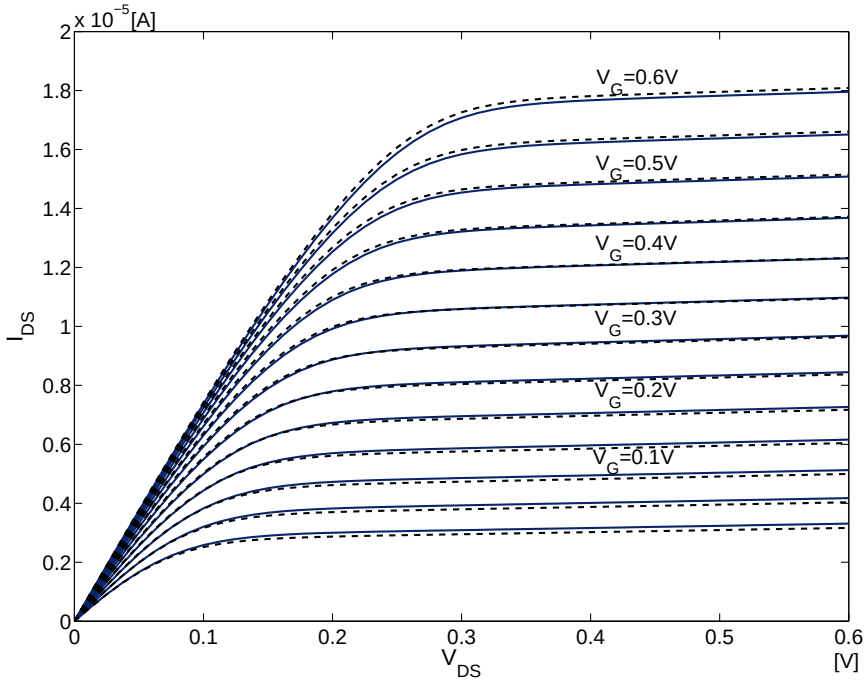

FIGURE 5.9: Drain current characteristics of FETToy with non-ballistic transport (solid lines) and $FETToy+$ Model D (dashed lines) with $T = 300K$, $E_F = 0eV$, $d = 1nm$ and $L = 300nm$.

The output drain source current characteristics were also derived and compared with the theoretical results generated by $FETToy+$ with specific temperature and Fermi level values. Tables 5.2, 5.3 and 5.4 show average RMS errors for both models with different temperatures ($T = 150K, 300K, 450K$) and Fermi levels ($E_F = -0.5eV, -0.32eV, 0eV$). The comparisons show that the numerical approximation used in the fast model causes a slight loss of accuracy, not exceeding 4%.

TABLE 5.2: Average I_{DS} RMS errors of $FETToy+$ Model D with $E_F = -0.32eV$.

$V_G[V]$	150K	300K	450K
0.1	3.5%	2.5%	2.6%
0.2	2.9%	2.4%	2.7%
0.3	2.8%	2.1%	2.2%
0.4	2.8%	2.5%	2.2%
0.5	2.6%	2.0%	2.3%
0.6	3.2%	2.3%	2.1%

TABLE 5.3: Average I_{DS} RMS errors of $FETToy+$ Model D with $E_F = -0.5eV$.

$V_G[V]$	150K	300K	450K
0.1	3.9%	3.8%	3.5%
0.2	3.5%	3.2%	3.4%
0.3	3.4%	2.9%	2.5%
0.4	3.6%	3.4%	2.3%
0.5	2.8%	2.7%	3.0%
0.6	3.1%	2.4%	2.6%

TABLE 5.4: Average I_{DS} RMS errors of $FETToy+$ Model D with $E_F = 0eV$.

$V_G[V]$	150K	300K	450K
0.1	2.7%	2.5%	3.1%
0.2	2.6%	2.2%	2.7%
0.3	2.8%	2.1%	2.0%
0.4	2.4%	1.9%	2.2%
0.5	2.1%	2.0%	1.9%
0.6	2.3%	2.2%	1.8%

5.3 Comparison with Experimental Results

To validate the performance of the proposed non-ballistic $FETToy+$ CNT transistor model based on spline approximation, some reported experimental characteristics were compared with the simulation results of an n-type CNT transistor with $d = 1.6nm$, $t_{ox} = 50nm$, $T = 300K$ and $E_F = -0.05eV$. Figure 5.10 shows the drain current performance captured from experimental measurement reported in [164] and simulation results of developed $FETToy+$ models with $n = 5$ cubic spline approximation of mobile charge densities.

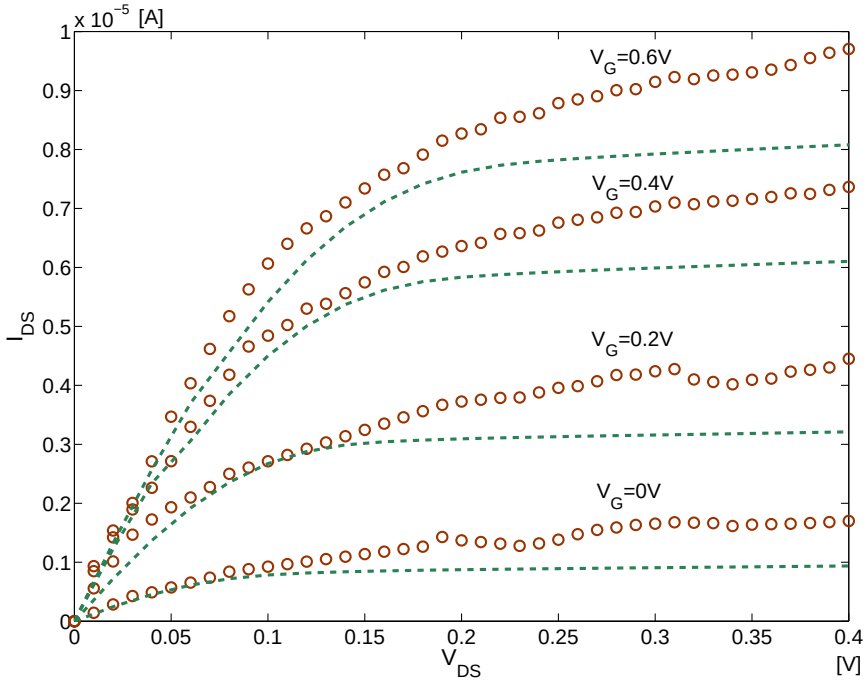

FIGURE 5.10: Drain current comparison between experimental results [164] (circlet lines) and the proposed $FETToy+$ model based on $n = 5$ approximation (dashed lines) with $d = 1.6nm, t_{ox} = 50nm, T = 300K, L = 300nm$ and $E_F = -0.05eV$.

Table 5.5 shows the normalised RMS error of drain current of the proposed $FETToy+$ models compared with the reported experimental results [164]. As can be seen from the figures, both models obtain RMS errors of less than 20% compared with the experimental results [164], with the non-ballistic model with $n = 5$ spline approximation providing more accurate results.

TABLE 5.5: Average I_{DS} RMS error comparison to the experimental data between two $FETToy+$ model based on 3-piece and 4-piece spline approximation with $d = 1.6nm, t_{ox} = 50nm, T = 300K$ and $E_F = -0.05eV$.

$V_G[V]$	**FETToy+ Model** $n = 4$	**FETToy+ Model** $n = 5$
0.2	17.7%	17.1%
0.4	18.9%	18.3%
0.6	19.6%	18.9%

5.4 Concluding Remarks

In this chapter, a new numerical technique for CNT transistor modelling, which allows incorporation of both ballistic and non-ballistic transport effects, has been developed. The four non-ballistic effects studied in this chapter are elastic scattering, band gap tuning with strain, tunnelling effect and phonon scattering. Adding numerical equations representing these effects, a CNT transistor model named $FETToy+$ based on cubic spline approximation of mobile charge densities of CNT transistors which combines ballistic transport characteristics and non-ballistic effects was implemented and the simulation results were compared with both theoretical and experimental results.

Chapter 6

Implementation of CNT Transistor Models in SPICE

Based on numerical piece-wise and cubic spline approximation of the non-equilibrium mobile charge density, ballistic CNT transistor models were proposed in Chapters 3 and 4. The non-ballistic transport effects of CNT transistors were considered and implementation of these effects was described in Chapter 5. Although these behavioural-level models can numerically describe the general transport performance of the CNT transistor, some electronic effects that might affect the operation of CNT devices at circuit level, for example, the bulk effect of the transistor, are not included in the proposed models. Therefore, SPICE-compatible CNT transistor models which can describe on-board physical effects and allow simulation of CNT based circuits are needed.

CNT transistor models are implemented in two versions of SPICE: HSPICE [165] using HSPICE macromodel development language, and Berkeley SPICE3 [166] by building additional C modules and incorporating them into the simulator's source code. Section 6.1 describes both n-type and p-type HSPICE macromodels of non-ballistic CNT transistors based on the cubic spline approximation of mobile charge densities described in Chapter 4. HSPICE is a widely used commercial simulation tool. However, there are some limitations in the HSPICE macromodelling language. One of the limitations is that HSPICE is an integrated simulator in which model libraries and mathematical functions are fixed,

which makes it difficult for users to add new modules or algorithms. To add new device models or properties to existing models, users need to develop external libraries which are invoked by the simulator at run time. In the light of the relatively closed system of HSPICE, in this research, the proposed CNT transistor model was added as a separate model library which is loaded into the HSPICE simulator when invoked. Another limitation of HSPICE comes from the syntax of the macromodelling language. In HSPICE, no loops or if statements are allowed. Therefore, not all the non-ballistic effects introduced in Chapter 5 can be added in the CNT transistor model. Tunnelling effect and phonon scattering cannot be implemented since if statements are needed for their implementation, so only elastic scattering and strain effect have been added. In Section 6.1.2, simulation of the developed CNT transistor macromodel and an inverter based on this model is carried out and results are given. The performance of the macromodel is compared to that of the reported Stanford HSPICE model [13, 14] and with experimental data [164]. The comparison results showed that the developed HSPICE macromodel performs more accurately than the Stanford model with approximately a 17% smaller RMS error while maintaining similar simulation speed.

Section 6.2 describes the implementation of the CNT transistor model in Berkeley SPICE3 [166] for Linux platforms. Compared with HSPICE, the main advantage of SPICE3 is that it is open source and thus allows more freedom for users to create new modules and functions and to combine them as internal components of the simulator. New device models can be added to SPICE3 by composing libraries using C language and recompiling them into the simulator. Both n-type-like and p-type-like CNT transistor models have been implemented and tested in SPICE3. The simulation results showed that the SPICE3 models not only support extensions of components compared with the HSPICE macromodels, but also operate approximately 40 times faster.

Section 6.2.2 shows the algorithm describing the implementation of the non-ballistic CNT transistor model in SPICE3. Taking advantage of the C programming language, which is less limited than the HSPICE macromodelling language, all the non-ballistic effects introduced in Section 5.1, Chapter 5 have been implemented in the developed SPICE model. Logic circuits with multiple transistors, including inverters, typical 6-

transistor static random access memory (SRAM) cells and pass-transistor logic (PTL) 1-bit full adders, have subsequently been simulated to validate the performance of the developed CNT transistor models in SPICE3.

Section 6.3 analyses the effect of parameter variation of the developed CNT transistor model in SPICE3. The aim of performing variation analysis is to evaluate how parameter variation may affect the performance of the device. The performance of inverters and 1-bit full adders based on the proposed CNT transistor models with various Fermi levels was analysed. Simulation results showed that the percentage of functionally working devices is related to the Fermi level variation, which implies that the proposed SPICE3 model is capable of reflecting the effect of parameter variation correctly and can be applied in circuit-level simulation. Finally, Section 6.4 summarises the work of this chapter.

6.1 HSPICE Macromodel of CNT Transistors

Based on the cubic spline approximation of mobile charge densities, HSPICE macromodels of both n-type and p-type CNT transistors were developed. In the following part of this section, the implementation of the HSPICE CNT transistor macromodel is described and the performance of this macromodel is tested and compared with results of both reported behavioural-level simulation [13, 14] and experiments [155].

6.1.1 HSPICE Macromodel Implementation

Algorithm 6.1 indicates the process of implementing the function package for the proposed CNT transistor model in HSPICE. As a new type of model which is not a built-in module of HSPICE, the CNT transistor model library which describes the transport characteristics of CNT transistors needs to be developed as an external module which can be invoked by HSPICE, named *CSmodel.lib*. In this new CNT library, the calculation of V_{SC} is also based on the cubic spline approximation introduced in Chapter 4. All parameters related to the computation of CNT transistor characteristics are included in

another library file with the name *param.lib*. Table B.5, Appendix B.3 lists all function files and their descriptions used in the HSPICE macromodel.

Algorithm 6.1: HSPICE Implementation of the CNT Transistor Macromodel

Input: terminal voltages V_G,V_D,V_S,V_{SUB}, Fermi level E_F, CNT diameter d_{cnt}, Temperature T, gate dioxide thickness $t0$ and Channel Length L

Output: drain current I_{DS}

1 define the terminals, including Drain, Gate, Source and Substrate, for the CNT transistor macromodel;
2 set default values and expressions for constants and parameters in the parameter library, which will be loaded by the model library;
3 build the model describing the CNT transport using cubic spline approximation in the model library;
4 implement non-ballistic effects (elastic scattering and strain effect) by adding related numerical equations in the model library;
5 obtain testbenches by building up simulation types, netlists, initial conditions and output environment;

The terminal definitions Drain, Gate, Source and Substrate for the CNT transistor are the same as that for a MOS device. The ports Drain and Source are not interchangeable in this macromodel. According to the description in Chapter 5, non-ballistic effects can be added to the model by implementing the numerical expressions which have been derived in Section 5.1. However, loops and if statements, which are required to numerically implement the tunnelling effect and phonon scattering equations, are not allowed in the HSPICE macromodel development language. Therefore, only the strain effect and elastic scattering were added to the HSPICE CNT transistor macromodel.

To improve the simulation of the developed macromodel, some statements setting the simulation environment were added to the model library. For example, to improve convergence and run time, the following lines of code are included at the beginning of the proposed CNT transistor model library (*CSmodel.lib*) in HSPICE:

```
.options POST  * store simulation results for analysis using graphical interface
.options AUTOSTOP  * stop the transient analysis automatically, resulting in substantial CPU time reduction
.options INGOLD=2      DCON=1  * specify exponential data format and invoke convergence check
.options GSHUNT=1e-12   RMIN=1e-15  * set the minimum value of internal time step
.options ABSTOL=1e-5    ABSVDC=1e-4  * set absolute node voltage error tolerance and minimum voltage
.options RELTOL=1e-2    RELVDC=1e-2  * set the relative error tolerance for voltages
.options NUMDGT=4   PIVOT=13  * set the number of significant digits for output and use fast pivot algorithm
```

The newly developed CNT transistor module needs to be invokable by the HSPICE simulator. To instantiate the device in the library, the module must be loaded at the beginning of the HSPICE deck using the following statement:

```
.lib 'CSmodel.lib' CNFET
```

The parameter library (*param.lib*), which contains all parameters required in the calculation of CNT transistor characteristics, will be loaded by the top level model file (*CSmodel.lib*) in simulation. The device parameters and their default values are described in Table 6.1. The values of these listed parameters can be changed by users when the CNT transistor macromodel is applied in various devices. If no changes are made, default values given in the parameter definition library (*param.lib*) will be used.

TABLE 6.1: Parameters of the proposed HSPICE CNT transistor macromodel.

Parameter Symbol	**Description**	**Default Value**
k	Relative dielectric constant of gate dioxide	3.9
t0	The gate dioxide thickness (m)	1.5e-9
L	Length of CNT (m)	3.0e-7
Cso	Source capacitance coefficient	0.097
Cdo	Drain capacitance coefficient	0.040
Ef	Fermi level (eV)	-0.32
dcnt	Diameter of the cnt (m)	1e-9
T	Temperature (K)	300

6.1.2 Performance of the HSPICE Macromodel

Following the development of an HSPICE macromodel for the CNT transistor, simulations were carried out to verify the macromodel's performance. An example of the testbench for n-type CNT transistor model is shown in listing 6.1. The power supply and voltage terminals are defined in lines 4-13, and the CNT transistor macromodel is set in line 17. For this simulation, a DC and a sweep measurement is applied in lines 19-22, while the results are output using the *.print* command in line 25.

```
1   .lib 'CSmodel.lib' CSmodel
2
3   **************************************************
4   *Supplies and voltage params:
5   .param Supply=0.6
6   .param Vg='Supply'
7   .param Vd='Supply'
8   **************************************************
9   * Define power supply
10  Vdd     Drain   Gnd     Vd
11  Vss     Source  Gnd     0
12  Vgg     Gate    Gnd     Vg
13  Vsub    Sub     Gnd     0
14  **************************************************
15  * Main Circuits
16  * nFET
17  CNT Drain Gate Source Sub nCNT Lch=L  Efi=Ef  dia=dcnt  Tox=t0
18  **************************************************
19  * Measurement
20  * test nFETs, Ids vs. Vgs
21  .DC      Vdd   START=0     STOP='Supply'   STEP='0.01'
22  + SWEEP  Vgg   START=0     STOP='Supply'   STEP='0.1'
23  **************************************************
24
25  .print I(Vdd)
26  .end
```

Listing 6.1: Testbench of a n-type CNT transistor model in HSPICE

Figure 6.1 shows the ballistic I_{DS} characteristics of an n-type CNT transistor implemented in HSPICE compared with the output current of a recently reported CNT transistor model from Stanford University [13, 14]. DC sweep simulation was carried out with gate voltage of $0V$ to $0.6V$ with $0.1V$ step and drain-source voltage $0V$ to $0.6V$ with $0.01V$ step. Discrepancies in the I_{DS} current values can be explained by the fact that the Stanford model considers subband effects which reduce the current [13, 14].

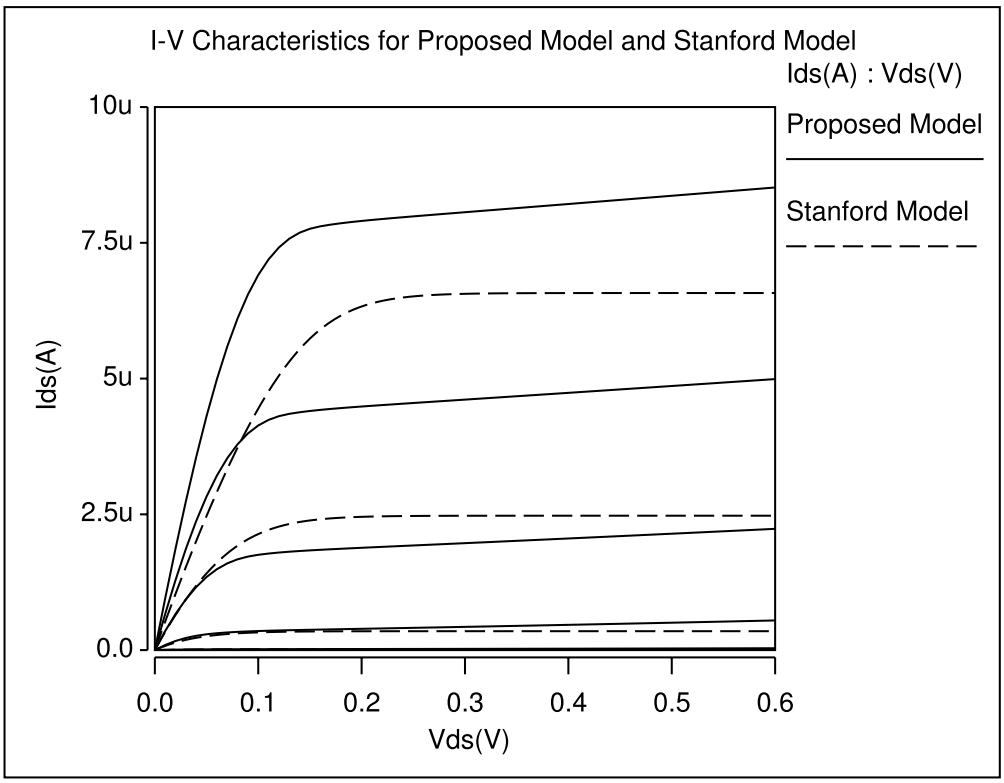

FIGURE 6.1: Sample simulated drain current comparison of ballistic CNT transistors between the HSPICE CNT transistor macromodel and the Stanford circuit-level model [13] with $T = 300K$, $L = 300nm$, $d = 1nm$ and $E_F = -0.32eV$.

As described in Section 6.1.1, the HSPICE macromodel has the potential to describe arbitrary non-ballistic transport effects including elastic scattering and band gap strain effect and therefore can be used to predict the performance of non-ballistic CNT transistors. Figure 6.2 shows the I_{DS} characteristics of the n-type CNT transistor macromodel implemented in HSPICE with elastic scattering [14] and strain effect on the channel region [155]. In the simulation, the gate voltage ramps from $0V$ to $0.6V$ with $0.1V$ step and the drain-source voltage rises from $0V$ to $0.6V$ with $0.01V$ step. Neither of these effects is included in the Stanford model. Elastic scattering may lower the transport ability of carriers, while the strain effect can widen the band gap of the CNT channel and thus reduce the drain current, which matches the simulation results well.

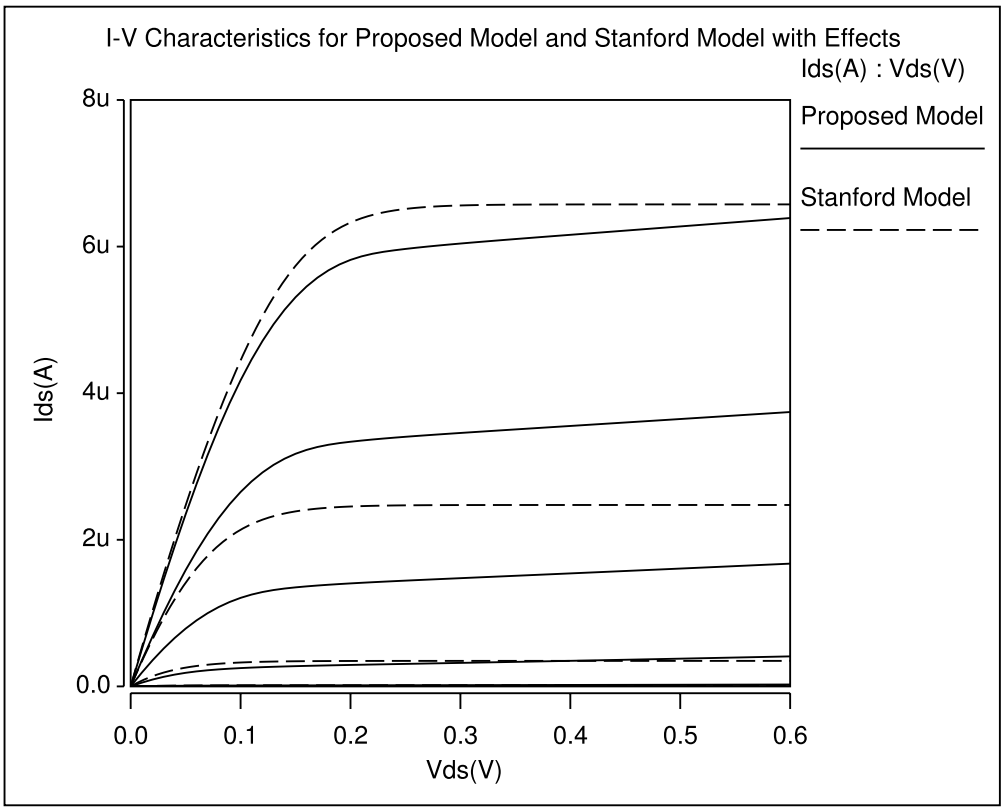

FIGURE 6.2: Sample simulated drain current comparison of CNT transistors between the HSPICE macromodel with non-ballistic transport effects and the Stanford circuit-level model [13] with $T = 300K$, $L = 300nm$, $d = 1nm$ and $E_F = -0.32eV$.

To verify the performance of the developed HSPICE non-ballistic CNT transistor macromodel, an n-type CNT transistor model, with $d = 1.6nm$, $t_{ox} = 50nm$, $T = 300K$ and $E_F = -0.05eV$, was simulated and the simulated drain chrrent was compared with recently reported experimental results [164] and the performance of the Stanford model with the same parameters [13, 14]. The simulation results are presented in Figure 6.3. This figure shows a close match between the proposed HSPICE CNT transistor macromodel and experimental results. It can be seen from Figure 6.3 that the proposed HSPICE macromodel matches the experimental results more closely than the Stanford model, especially in terms of the saturation region. Additionally, the developed HSPICE macromodel performs more accurately than the Stanford model while maintaining similar speed [32] as shown in Table 6.2.

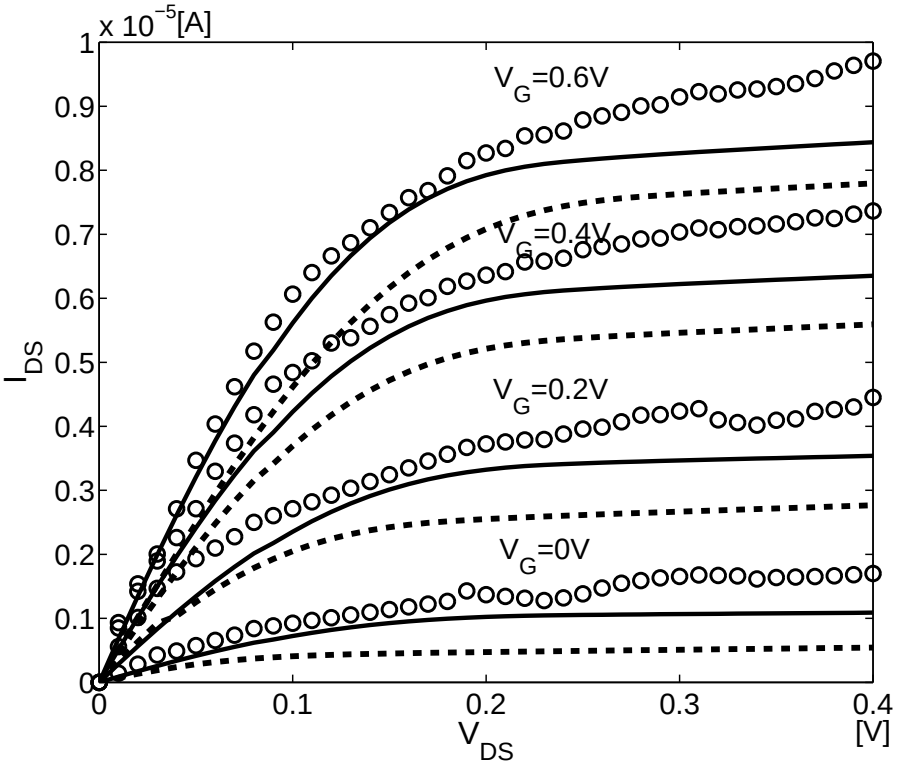

FIGURE 6.3: Drain current comparison between experimental results [164] (circlet lines) and the proposed HSPICE macromodel based on $n = 4$ spline approximation (solid lines) and Stanford model [13] (dashed lines) with $d = 1.6nm, t_{ox} = 50nm, T = 300K, L = 300nm$ and $E_F = -0.05eV$.

TABLE 6.2: Average I_{DS} RMS error and CPU time comparison between the Stanford model and the developed HSPICE macromodel with $d = 1.6nm, t_{ox} = 50nm, T = 300K$ and $E_F = -0.05eV$.

$V_G[V]$	**Proposed Macromodel** $n = 4$	**Stanford Model**
0.2	16.3%	35.7%
0.4	15.5%	29.6%
0.6	14.3%	25.2%
CPU Time[s]	40.32	47.60

A p-type CNT transistor macromodel was implemented in HSPICE and Figure 6.4 illustrates the simulated I_{DS} characteristics of the proposed model. In the simulation of the p-type model, the source of the transistor is set to $0.6V$, whilst the drain voltage goes up from $-0.6V$ to $0V$ with $0.01V$ step and the drain voltage ramps from $0V$ to $-0.6V$ with $0.1V$ step. In this p-type CNT transistor macromodel, the bulk voltage which may change the charge densities in the CNT channel is considered, which helps to reflect correctly the behaviour of a p-type CNT transistor.

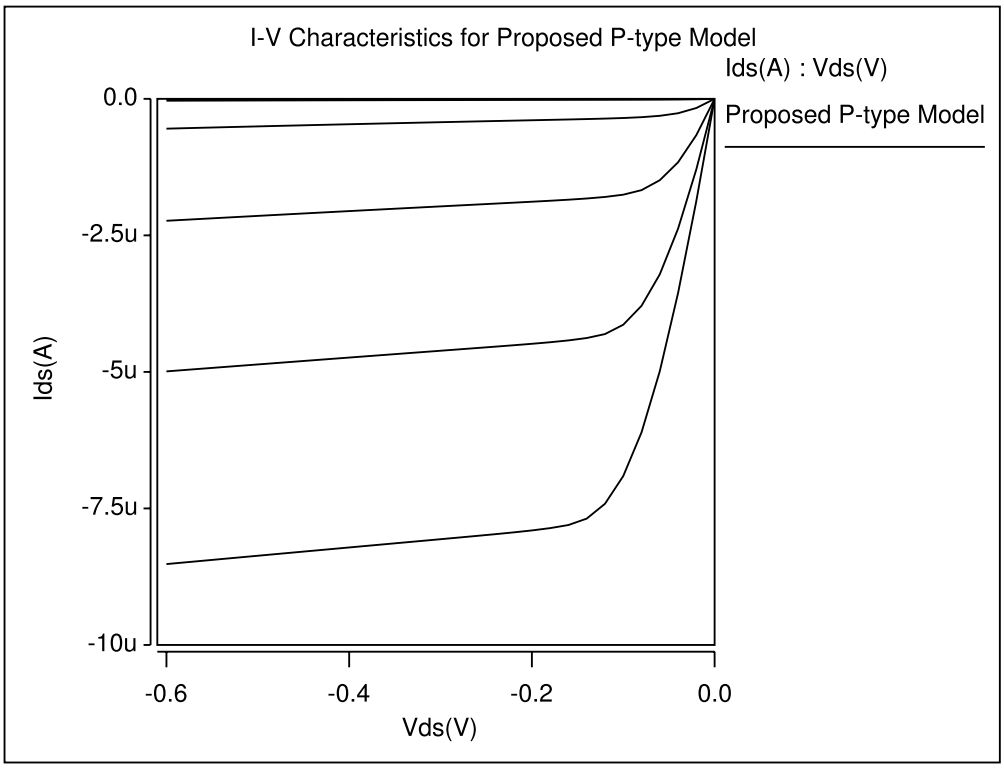

FIGURE 6.4: Simulated drain current characteristics of a p-type CNT transistor macro-model with $T = 300K$, $L = 300nm$, $d = 1nm$ and $E_F = 0.32eV$ in HSPICE.

Both n-type and p-type CNT transistor models are employed in the analysis of a complementary CNT inverter. The HSPICE simulation results of the complementary inverter are shown in Figure 6.5. The figure shows the transfer characteristics of the inverter with input voltage ramping from $0V$ to $0.6V$.

An example of the proposed inverter testbench code is shown in listing 6.2. Lines 3-6 describe the inverter with a capacitor load at the output. Lines 8-10 set the voltage input conditions and a DC simulation is applied as line 12 states.

```
1   .lib 'CSmodel.lib' CSmodel
2
3   * test inverter
4   XCNT1 OUT IN VSS VSS nCNT Lch=L  Efi=Ef  dia=dcnt  Tox=t0
5   XCNT2 OUT IN VDD VDD pCNT Lch=L  Efi=-Ef  dia=dcnt  Tox=t0
6   cLoad OUT VSS 100fF
7
8   vVDD VDD 0 0.6
9   vVSS VSS 0 0
10  vIN IN 0 pulse( 0 0.6 100ps 100ps 100ps 2ns 4ns )
11
```

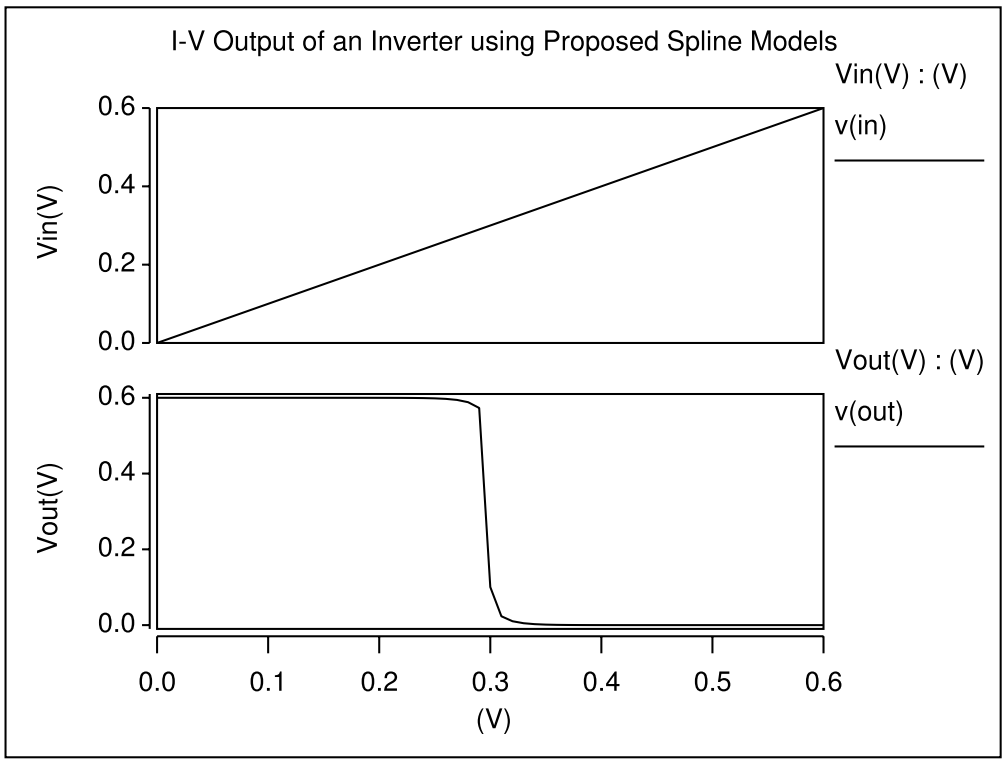

FIGURE 6.5: Performance of a CNT based inverter simulated in HSPICE; input ramps from $0V$ to $0.6V$.

```
12  .dc vIN start=0 stop=0.6 step=0.01
13
14  .print I(Vdd)
15
16  .end
```

LISTING 6.2: Testbench of an inverter based on CNT models in HSPICE

6.2 SPICE3 Implementation of CNT Transistor Model

Berkeley SPICE3 is an analogue-circuit simulator that is used to calculate and display circuit behaviour. As a general-purpose circuit simulation platform for device analysis, SPICE3 has been widely exploited in the circuit modelling area [166]. Differently from other simulators with fixed built-in models for semiconductor devices, SPICE3 is available for researchers to develop and add new models in the library of the simulator.

In this section, the modelling features and work flow of Berkeley SPICE3 is introduced first. Then the implementation of the proposed non-ballistic CNT transistor model in

SPICE3 is described in detail. Logic circuits including inverters, SRAM cells and full adders based on the developed SPICE3 models are constructed and simulated, and the simulation speed of the SPICE3 model is compared with that of the HSPICE macromodel introduced in the previous section. At the end of this section, the power dissipation of the proposed CNT transistor model is evaluated and compared with that of the MOS3 model via SPICE3 simulation.

6.2.1 Berkeley SPICE3 Working Process

Berkeley SPICE3 was developed by the EECS Department of the University of California at Berkeley [167], and is well known as a general-purpose circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analyses. SPICE3 originally consisted of two parts: the SPICE3 calculation engine which was run as a batch job, and an interactive front-end (*Nutmeg*) used to extract and display the results. Recent implementation of SPICE3 has combined these two parts together.

The source code of Berkeley SPICE3 is written using C language and has been freely available to public users. SPICE3 contains a function library which consists of all parameters and equations necessary to compute the physical characteristics of the target devices. The structure tree of the file package is illustrated in Figure B.1, Appendix B.4.

The proposed working process of the SPICE3 simulator is illustrated in Figure 6.6. The SPICE3 library has a set of header files describing the implementation of hardware objects including concurrent and hierarchical modules, ports, and clocks. The library also defines the internal parsers of the simulator and contains necessary mathematical functions. The configuration files (*configure.in*, *makefile.am*) set the compilation and path features of the source code. The code can be compiled and linked together using standard ANSI C compliant compilers. An executable SPICE3 simulator can then be derived after compiling. The simulator can read in testbench files, run the simulation, and output results. Users can invoke the graphics-terminal independent interface (*Nutmeg*) to display more details of the output results.

To add a new model that is not built in the SPICE3 device library, function files for the

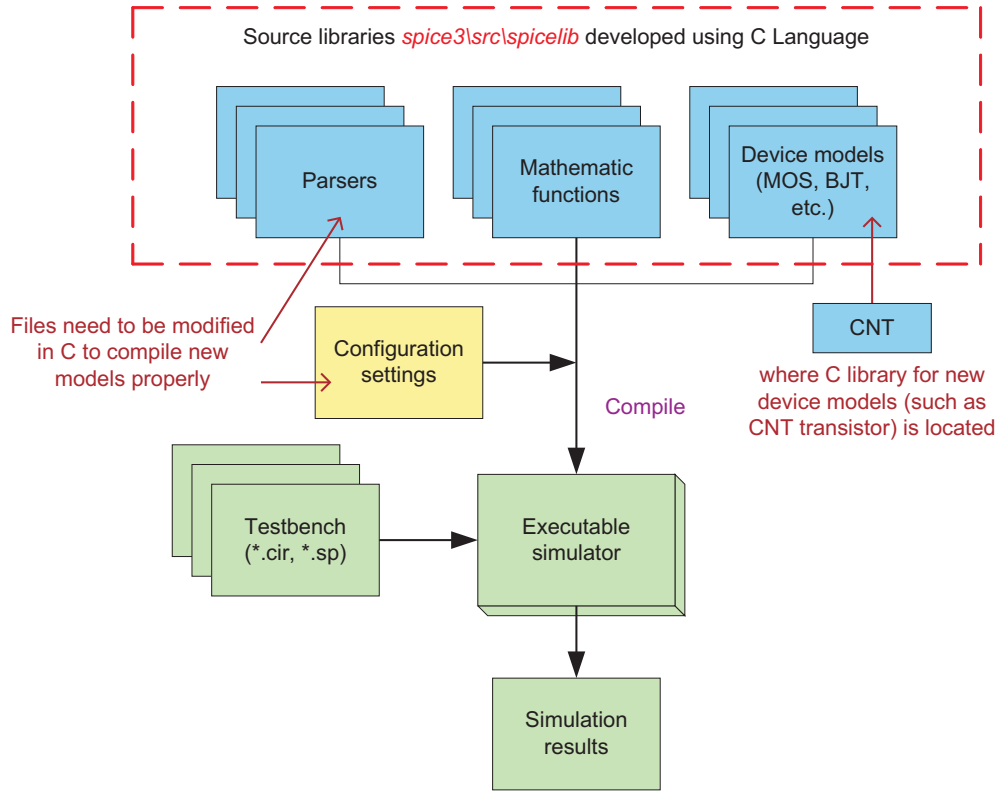

FIGURE 6.6: Proposed work process and steps of composing new models for CNT based circuits in SPICE3.

new model need to be developed using C language. Furthermore, related parser files and configuration settings, which allow the SPICE3 simulator to 'recognise' the new module, need to be modified to make sure the newly added model library can be compiled, which is also illustrated in Figure 6.6.

6.2.2 Implementation of the SPICE3 Model

Algorithm 6.2 indicates the implementation of the model library for the non-ballistic CNT transistor model in SPICE3. Firstly, the name and terminals of the newly added model are defined in line 1 in Algorithm 6.2. Parameters which are required in the calculation of the transport characteristics of CNT transistor are then set. The C programming language allows implementation of all the non-ballistic effects, including elastic scattering, phonon scattering, strain and tunnelling, introduced in Chapter 5 in the SPICE3 CNT transistor model. Therefore, the developed model incorporates both ballistic and non-ballistic transport effects of CNT transistors. After creating the model

library, the configuration files of SPICE3 need to be modified so that the new library can be compiled. Following compilation of the CNT transistor module and derivation of the executable SPICE3 simulator, CNT based circuits can be simulated.

Algorithm 6.2: Berkeley SPICE Implementation of the CNT Transistor Model Library

Input: terminal voltages V_G,V_D,V_S,V_{SUB}, Fermi level E_F, CNT diameter d_{cnt}, Temperature T and gate dioxide thickness $t0$

Output: drain current I_{DS}

1 define the name of the model (nCNT/pCNT) and terminals, Drain, Gate, Source and Substrate, for the SPICE3 CNT transistor model;
2 set constant values and define parameters which will be compiled into the simulator;
3 build the DC transport model using the cubic spline approximation of mobile charge densities;
4 implement non-ballistic effects by adding related numerical equations ;
5 modify configuration files to make the new CNT library compilable in the SPICE3 simulator;
6 obtain testbenches (*.sp* or *.cir* files) by setting up circuit netlists, simulation types, initial conditions and output environment;

As stated in Algorithm 6.2, after creating the proposed CNT transistor model in the SPICE3 library of devices, the configuration files of SPICE3 need to be modified to make the new library compilable, which is described in Appendix B.4. To generate the executable SPICE3 simulator, compilation commands under the Linux system are employed as follows:

```
./autogen.sh
./configure
make
sudo make install
```

When the SPICE3 simulator has been created, the simulation of circuits based on the developed SPICE3 CNT transistor models can be carried out. For example, the command synopsis to run a simulation of a specific testbench is:

```
spicecnt [-b] [-r rawfile] [-i] [testbench files]
```

In the synopsis, $-b$ allows the simulation to run in batch mode and $-i$ activates the interactive mode in which interactive inputs are available. The derived *.raw* files can be read in the *Nutmeg* program which can produce graphic output based on the data. For SPICE3, the input testbenches are usually *.sp* or *.cir* files.

After obtaining the non-ballistic CNT transistor model in SPICE3, simulations of single n-type CNT transistors and logic gates were carried out using the developed SPICE3 simulator. Figure 6.7 shows the I_{DS} characteristics of the n-type-like transistor implemented in SPICE3. DC sweep simulation was carried out with gate voltage of $0V$ to $0.6V$ with $0.1V$ step and drain-source voltage $0V$ to $0.6V$ with $0.01V$ step.

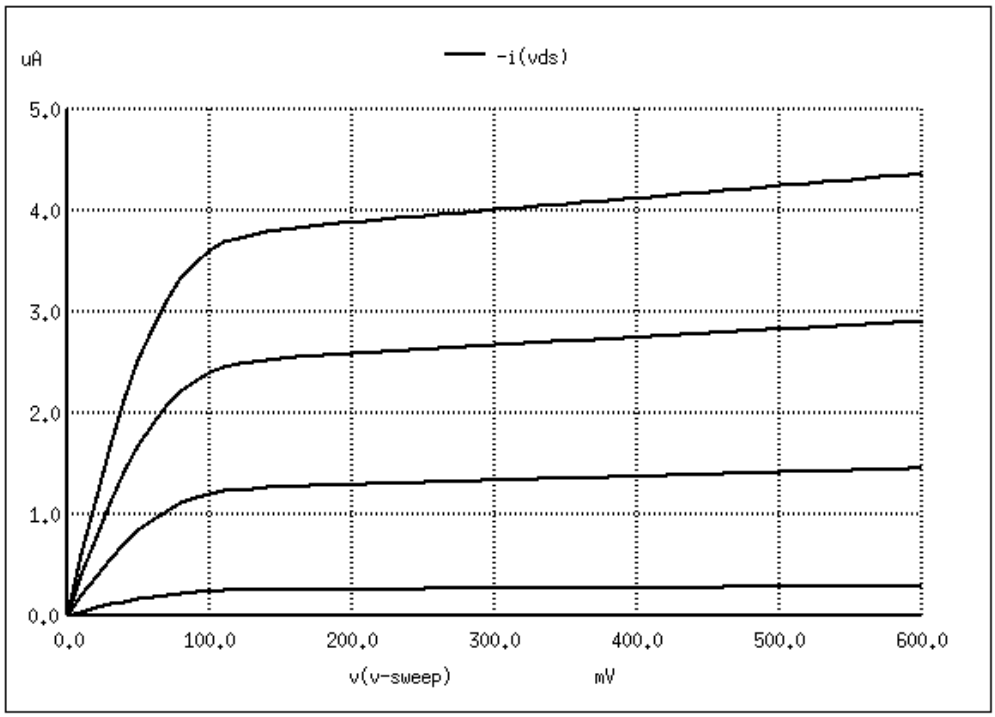

FIGURE 6.7: Drain current characteristics of the proposed n-type SPICE3 CNT transistor model with $T = 300K$, $L = 300nm$, $dcnt = 1nm$ and $E_F = -0.32eV$.

A corresponding p-type CNT transistor model was also implemented in SPICE3 and Figure 6.8 illustrates the simulated I_{DS} characteristics with V_{GS} of the p-type transistor ramping from $0V$ to $-0.6V$ with $-0.1V$ step and V_{DS} from $0V$ to $0.6V$ with $0.01V$ step. It can be seen from Figures 6.7 and 6.8 that the channel current of the n-type transistor is slightly larger than that of the p-type transistor under the same voltage input. This discrepancy is caused by the bulk voltage of the p-type CNT transistor which might affect the charge densities in the CNT channel and thus reduce the current.

Complementary logic inverters have been obtained using a pair of n-type and p-type CNT transistor models. The SPICE simulation results of the complementary inverter are shown in Figure 6.9. The figure demonstrates that the inverter functionally works with voltage input ramping from $0V$ to $0.5V$.

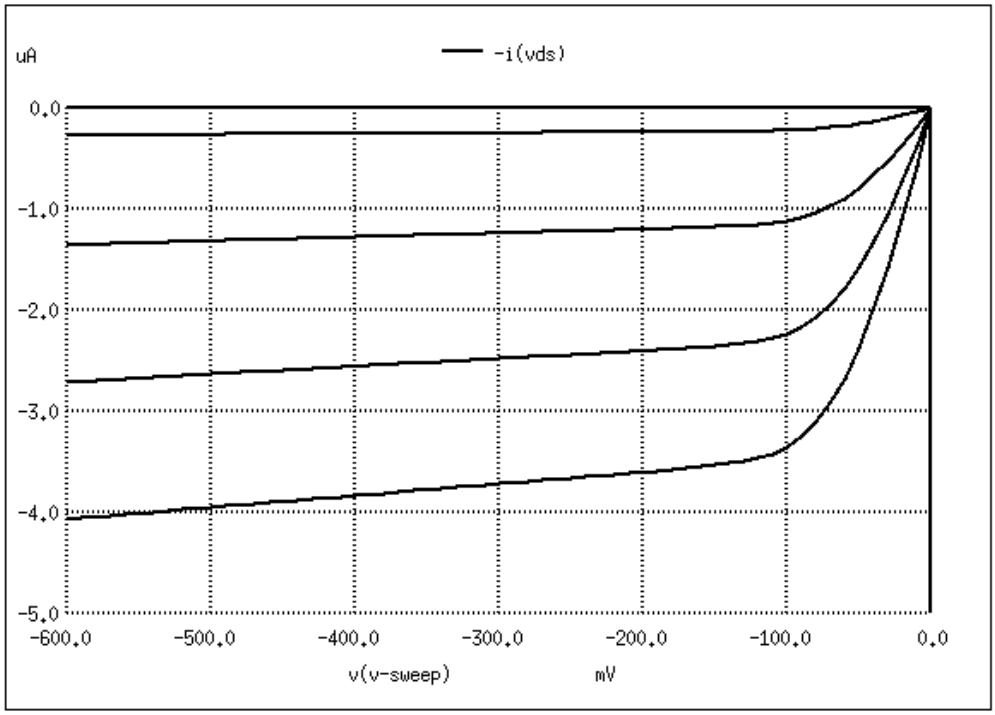

FIGURE 6.8: Drain current characteristics of the proposed p-type SPICE3 CNT transistor model with $T = 300K$, $L = 300nm$, $dcnt = 1nm$ and $E_F = 0.32eV$.

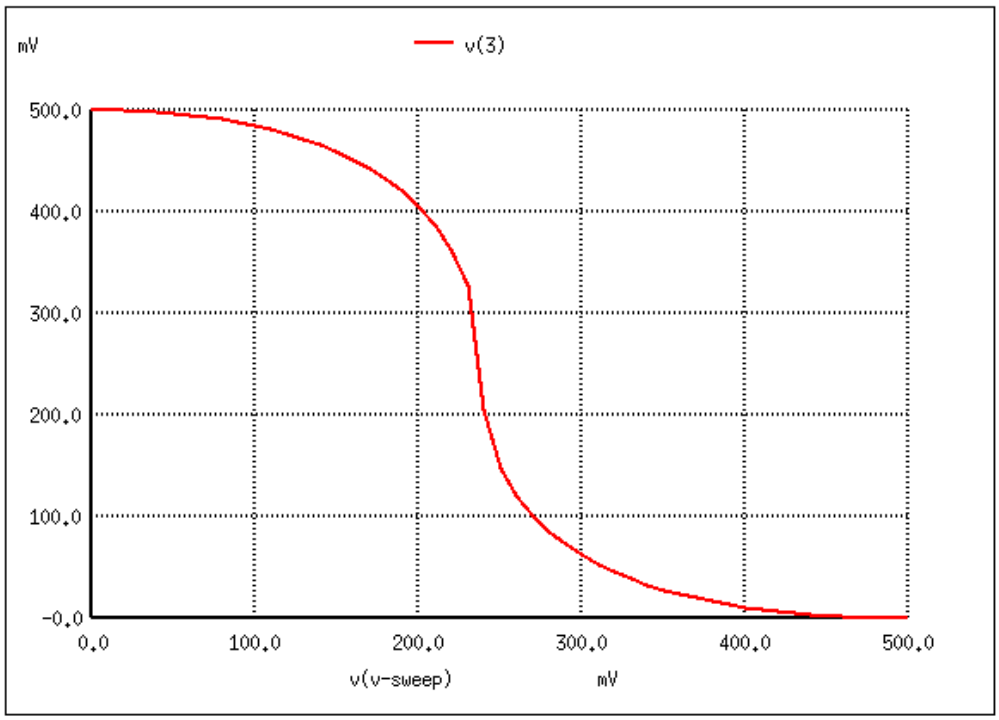

FIGURE 6.9: CNT based inverter simulation result in SPICE3; input ramps from $0V$ to $0.5V$.

6.2.3 Case Studies of CNT Based Logic Circuits (SRAM and Adder)

To validate the feasibility of the developed SPICE3 model in more logic circuits, a six-transistor static random access memory cell using both n-type and p-type SPICE-like CNT transistor models was constructed and simulated. The schematic of a typical SRAM cell is given in Figure 6.10.

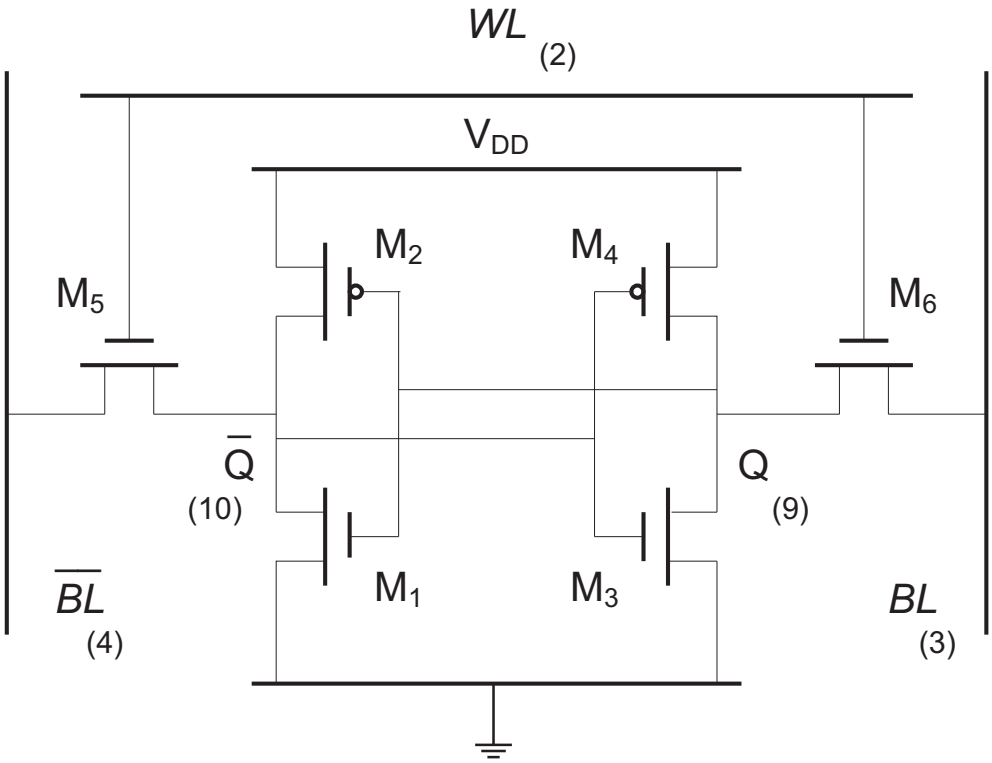

FIGURE 6.10: Schematic of a six-transistor SRAM cell.

The testbench to simulate the SRAM cell based on the proposed SPICE3 CNT transistor model is shown in listing 6.3. In this script, lines 3-6 provide the reference voltage and input waveforms. The SRAM netlist shown in lines 8-20 is a typical SPICE description which connects components and nodes for analysis. Note that the transistor models given by lines 17 and 18 use the developed non-ballistic CNT transistor model based on spline approximation of mobile charge densities. A transient measurement is applied and the output stage is shown in lines 22-25.

```
1  CNT SRAM cell output characteristics
2  .opt nopage
3  Vds 1 0 DC=.5
4  Vgs1 2 0 PWL 0 0 1PS .5 600PS .5 601PS 0
```

```
5   Vgs2 3 0 PWL 0 0 1PS .5 300PS .5 301PS 0 600PS 0 601PS .5 900PS .5 901PS 0
6   Vgs3 4 0 PWL 0 .5 1PS 0 300PS 0 301PS .5 600PS .5 601PS 0 900PS 0 901PS .5
7
8   * ef is the Fermi Level, dia is the diameter of the CNT
9   * default silicon dioxide thickness t0 is 15nm
10  * and relative static permittivity equals to 3.9
11  M1 10 9 0 0 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
12  M2 10 9 1 1 mod2 ad=10f as=10f dia=1.0e-9 ef=0.3
13  M3 9 10 0 0 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
14  M4 9 10 1 1 mod2 ad=10f as=10f dia=1.0e-9 ef=0.3
15  M5 4 2 10 10 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
16  M6 3 2 9 9 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
17  .model mod1 ncnt vto=0.15 nsub=1.0e15 u0=550 tox=15e-9
18  .model mod2 pcnt vto=-0.15 nsub=1.0e15 u0=150 tox=15e-9
19  C1 9 0 .1f
20  C2 10 0 .1f
21
22  .dc  Vgs 0.0 .5 .1
23  .TRAN 2PS 1200PS
24  .plot dc -i(vds)
25  .end
```

LISTING 6.3: Testbench of an SRAM cell based on the proposed CNT transistor model in SPICE3

It can be seen in Figure 6.11 that the SRAM cell performs as expected. As the word line (WL) is asserted, data can be written into the memory cell by applying proper values to bit lines (BL and $\overline{BL}$). After the writing period, the SRAM cell comes into standby status while the word line is set to 0, and the memory cell will store the data until next working period. The simulation time of the CNT based SRAM is short, with an average CPU time of circa 1 second. The output current of the SRAM cell has also been obtained to analyse the power consumption of the device. Figure 6.12 illustrates that the drain current of the transistors within the memory cell is less than $1.6\mu A$. With small supply voltages at terminals of the transistors, the SRAM can be estimated to be power efficient.

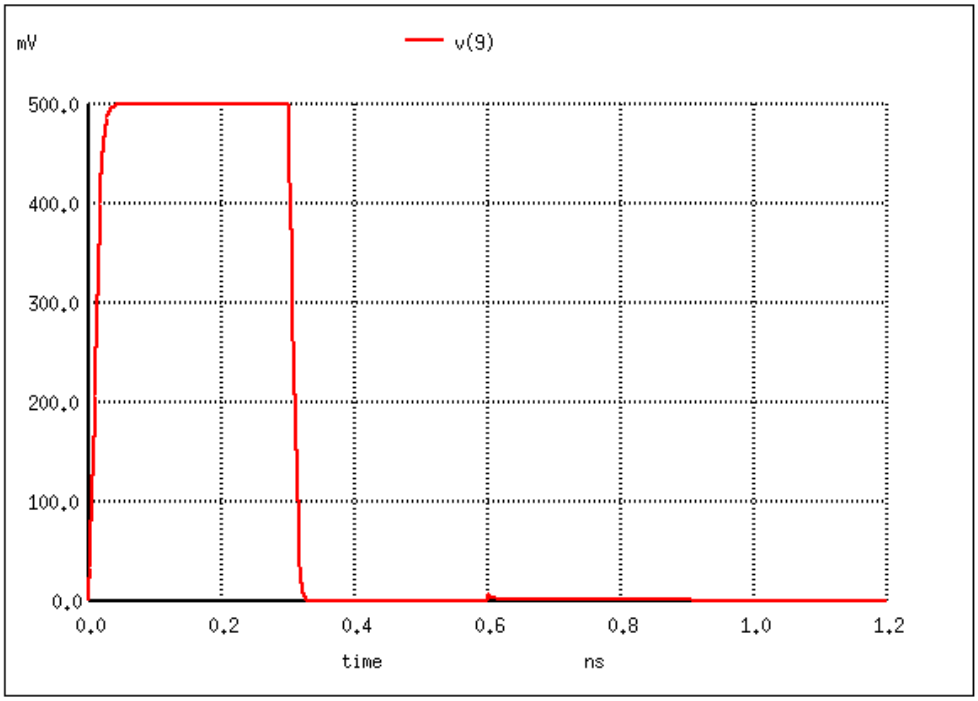

FIGURE 6.11: The output characteristics of the SRAM cell based on the proposed SPICE3 CNT transistor model.

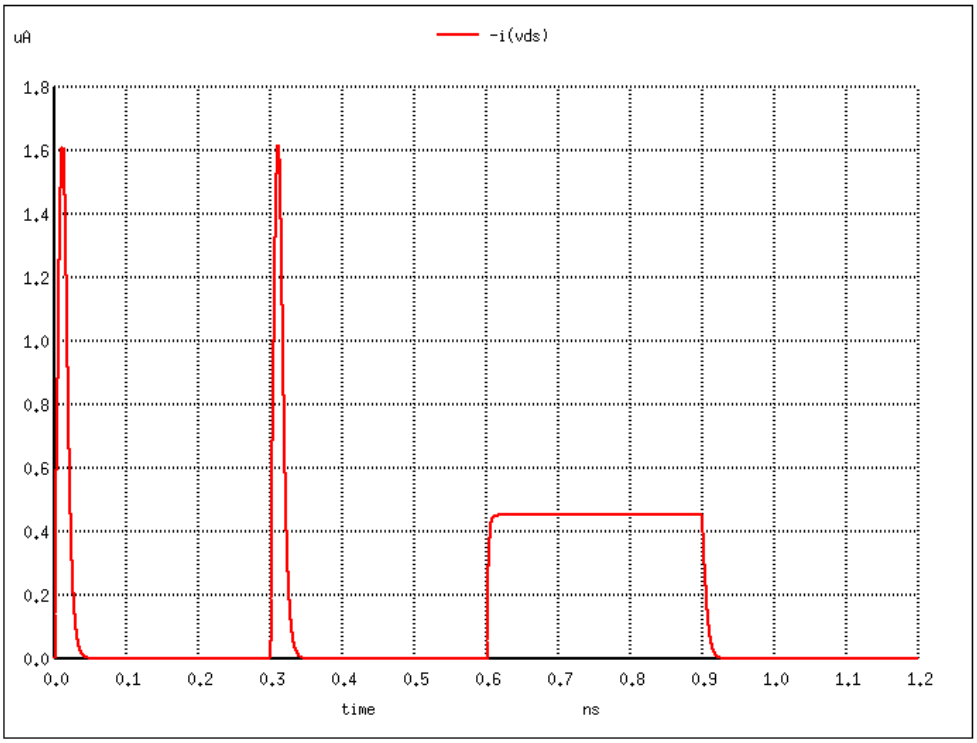

FIGURE 6.12: The operation current characteristics of the SRAM cell based on the proposed SPICE3 CNT transistor model.

With the current characteristics of the simulated CNT transistor shown in Figure 6.12, the power consumption of the SRAM cell can be estimated using Eq. 6.1 [168]:

$$P_{SC} = \frac{1}{2} V_{DD} I_{peak} t_t f \cdot n \tag{6.1}$$

where V_{DD} is the drain supply voltage ($0.5V$ for this SRAM simulation), f is the operation frequency ($3.33GHz$), t_t represents the transition time of the input ($0.1ns$), I_{peak} is the maximum saturation current of the CNT transistor in the SRAM cell ($1.6uA$), and n is the number of transistors (6 transistors) used in the SRAM cell. With the parameters which can be derived from the simulation, the power consumption P_{SC} can be estimated to be circa $0.8\mu W$ for the simulated SRAM cell using Eq. 6.1, which dissipates very small energy (around $2.4 \times 10^{-16} J$ per switch for the CNT SRAM cell).

A 1-bit full adder based on the SPICE3 CNT transistor models was also simulated. Figure 6.13 illustrates the schematic of the pass transistor implementation of a full adder [169] which employs 16 n-type CNT transistors and two complementary inverters. The netlist of the simulated 1-bit pass-transistor logic adder is shown in listing 6.4. Be aware that the developed SPICE3 non-ballistic CNT transistor models are invoked by lines 28 and 29. Two inverters were built at the output ports of the adder as described in lines 10-11 and 22-23. Two $50fF$ capacitors were used as loads at the output (lines 25-26).

```
1   M1 5 6 11 11 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
2   M2 11 7 9 9 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
3   M3 2 6 12 12 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
4   M4 12 4 9 9 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
5   M5 2 3 13 13 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
6   M6 13 7 9 9 mod1  ad=10f as=10f dia=1.0e-9 ef=-0.3
7   M7 5 3 14 14 mod1  ad=10f as=10f dia=1.0e-9 ef=-0.3
8   M8 14 4 9 9 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
9
10  M9 19 9 1 1 mod2 ad=10f as=10f dia=1.0e-9 ef=-0.3
11  M10 19 9 0 0 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
12
13  M11 1 6 15 15 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
14  M12 15 7 10 10 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
15  M13 5 6 16 16 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
16  M14 16 4 10 10 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
17  M15 5 3 17 17 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
```

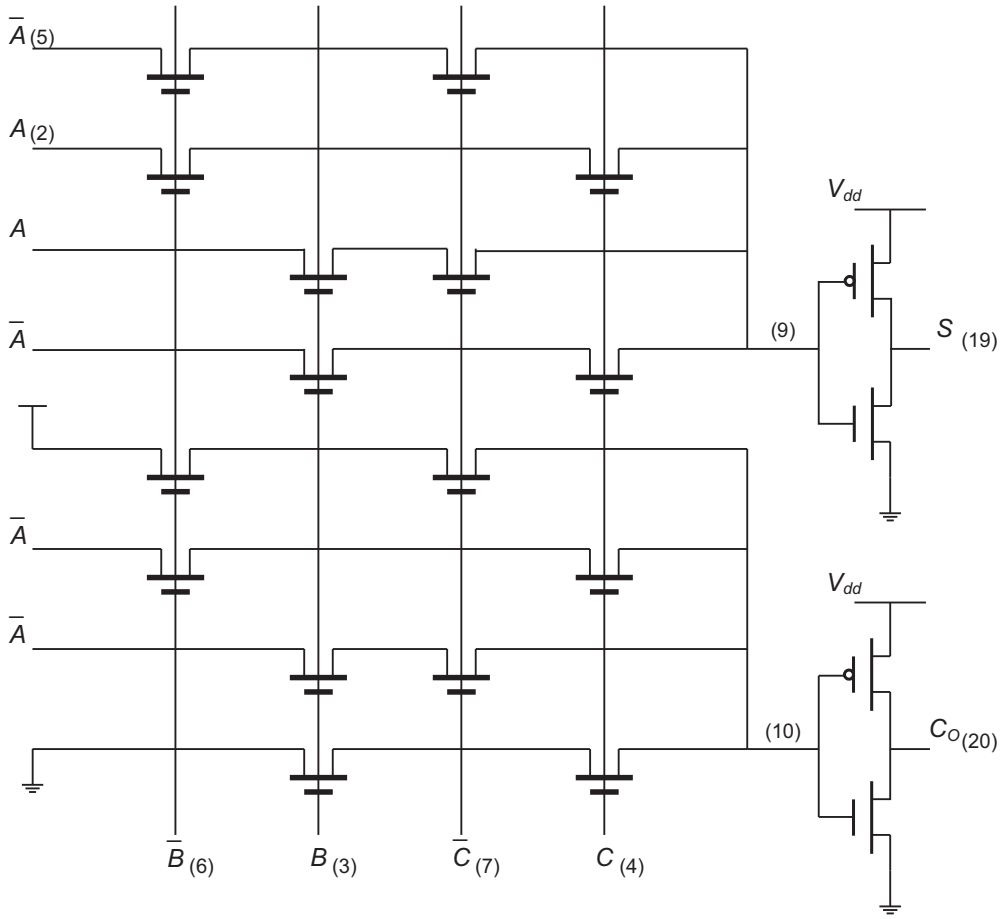

FIGURE 6.13: Schematic of a pass transistor logic 1-bit full adder based on the proposed SPICE3 CNT transistor model.

```
18  M16 17 7 10 10 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
19  M17 0 3 18 18 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
20  M18 18 4 10 10 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
21
22  M19 20 10 1 1 mod2 ad=10f as=10f dia=1.0e-9 ef=0.3
23  M20 20 10 0 0 mod1 ad=10f as=10f dia=1.0e-9 ef=-0.3
24
25  C1 19 0 50f
26  C2 20 0 50f
27
28  .model mod1 ncnt vto=0.15 nsub=1.0e15 u0=550 tox=15e-9
29  .model mod2 pcnt vto=-0.15 nsub=1.0e15 u0=150 tox=15e-9
```

LISTING 6.4: Testbench of a 1-bit pass-transistor logic adder based on the proposed CNT transistor model in SPICE3

There are three input ports of the pass-transistor logic adder, A, B and C, as shown

in Figure 6.13. The input signals of A, B and C in the simulation are square waves with cycles of 1200*ps*, 600*ps* and 300*ps* respectively. The logic performance of the pass-transistor logic adder is shown in Figures 6.14 and 6.15.

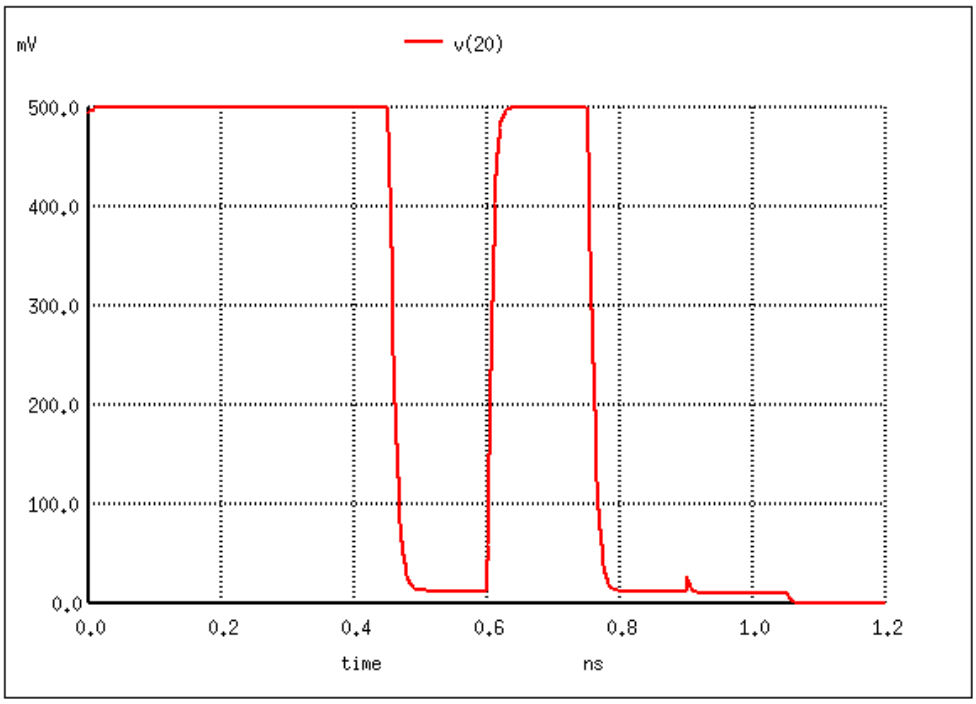

FIGURE 6.14: Simulated C_{out} performance of the pass transistor logic 1-bit adder based on the proposed SPICE3 CNT transistor model.

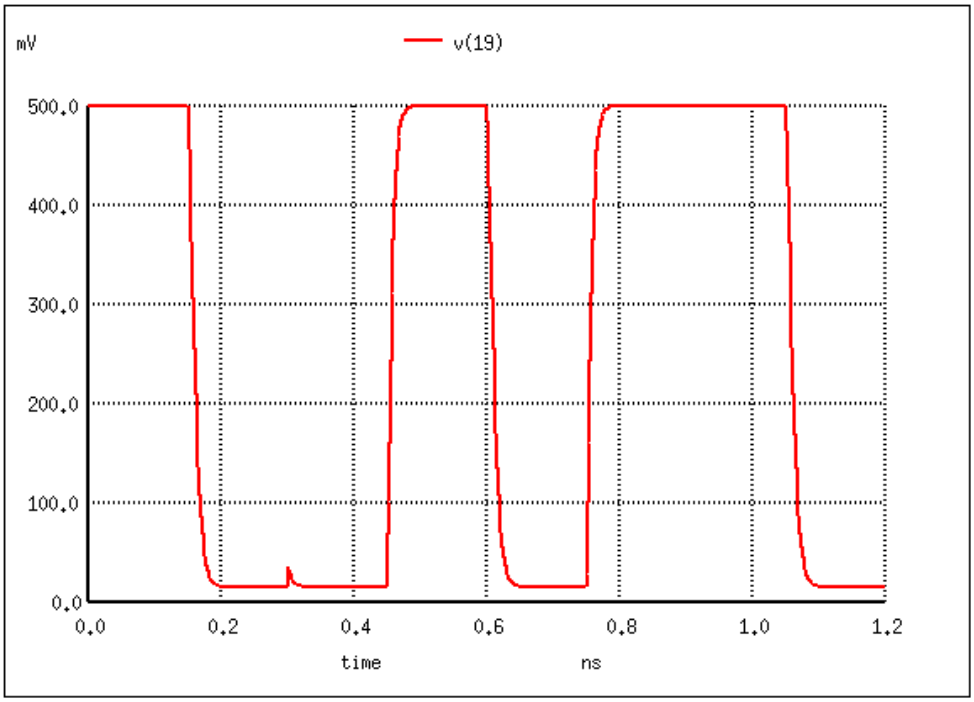

FIGURE 6.15: Simulated S performance of the pass transistor full logic 1-bit adder based on the proposed SPICE3 CNT transistor model.

The drain current of the transistors within the adder circuit was also traced and the results are shown in Figure 6.16. Similarly to the power evaluation of SRAM cell, the power consumption of the pass-transistor logic adder can be estimated to be around $8.7\mu W$ using Eq. 6.1, and the energy needed for each switch is $1.3 \times 10^{-15} J$ approximately.

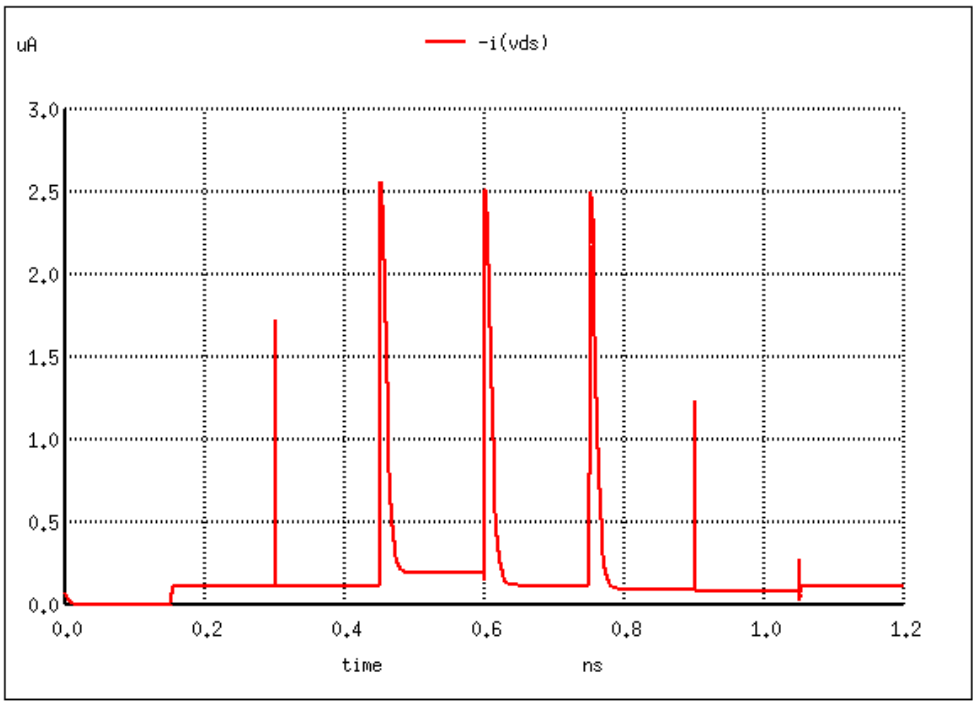

FIGURE 6.16: The operation current characteristics of the full adder based on the proposed SPICE3 CNT transistor model.

To validate the speed of the SPICE3 model, the simulation time of the developed CNT transistor model was obtained and compared with that of the Stanford HSPICE model [13, 14]. Table 6.3 shows that the SPICE3 model runs over 40 times faster than the reported HSPICE model.

TABLE 6.3: Average CPU Time of the proposed CNT transistor model in SPICE3 compared with HSPICE Stanford model.

Model	SPICE3 Model	HSPICE Stanford Model
SRAM	1.0264s	42.87s
1-bit Full Adder	4.9336s	211.92s

Table 6.4 shows the estimated power consumption per switch of three different logic circuits implemented using the proposed CNT transistor model in SPICE3. Comparison was made between the simulation results of the CNT-based circuits and those of

conventional MOS3 devices. According to the data shown in Table 6.4, circuits based on the developed CNT transistor model can save more than 90% of the power compared with circuits with MOS3 transistor models, which indicates strong potential for CNT transistors in low power applications.

TABLE 6.4: Comparison of power consumption per switch of logic circuits based on the proposed SPICE3 CNT transistor model and conventional MOS based devices.

Model	SPICE3 CNT Based Model	MOS3 Based Model
Inverter	6.3e-17J	9.5e-16J
SRAM	2.4e-16J	6.8e-15J
1-bit Full Adder	1.3e-15J	3.2e-14J

6.3 Variation Analysis

An important consideration in the design and reliability of CNT circuits is the role of parameter variation which can affect the characteristics of CNT devices. Most of the parameter variation is caused by defects within the CNT structure. Researchers have reported that various types of defects exist in CNT transistors such as metallic CNTs [24], impurities [25], poor contacts, and misaligned tubes [107]. All these defects lead to CNT parameter variation. To verify the performance of the developed CNT transistor model with parameter variation, variation analysis was carried out in this research.

According to Equations 3.14 and 3.19 introduced in Chapter 3, the Fermi level is a key factor to determine the transport characteristics of the CNT transistor. However, it is difficult to control the Fermi level value of a CNT transistor in fabrication. For circuits with large numbers of CNT transistors, the Fermi level variation of CNTs may lead to functional failure of certain transistors and thus affect the performance of the entire circuit. Therefore, Fermi level variation should be analysed when designing circuits based on CNT transistors. The typical Fermi level value of an n-type CNT is around $-0.32eV$ [12]. In the Fermi level variation analysis of this work, a series of Fermi level values was randomly generated using the Gaussian Distribution algorithm [170] with $\mu = \pm 0.32$ (- for n-type and + for p-type) and $\sigma = 0.2$ in MATLAB. Simulation of logic circuits based on the proposed SPICE3 CNT transistor models with these generated

Fermi levels was carried to provide quantitative estimation of the failure rate caused by Fermi level variation.

Logic inverters based on the developed n- and p-type CNT transistor models were analysed in SPICE3. With randomly generated Fermi levels, the transport capabilities of the two transistors in one inverter may vary significantly. With strong n-type and weak p-type transistors, the threshold voltage of the inverter may bias lower, and vice versa. In the simulation, the supply voltage is $0.6V$ and the input voltage of the inverter ramps from 0 to $0.6V$. In this Fermi level variation study, inverters with threshold voltage (V_T) between $0.2V$ and $0.4V$ are considered to function correctly, while inverters having $V_T < 0.2V$ or $V_T > 0.4V$ work improperly. Table 6.5 shows details of the various Fermi level values of CNT transistors and it is shown in Figure 6.17 that nearly half (53%) of the inverters have threshold voltages between $0.2V$ and $0.4V$ in this set of simulations, which implies that the proposed SPICE3 CNT transistor model can capture the effect of Fermi level variation on CNT based circuits.

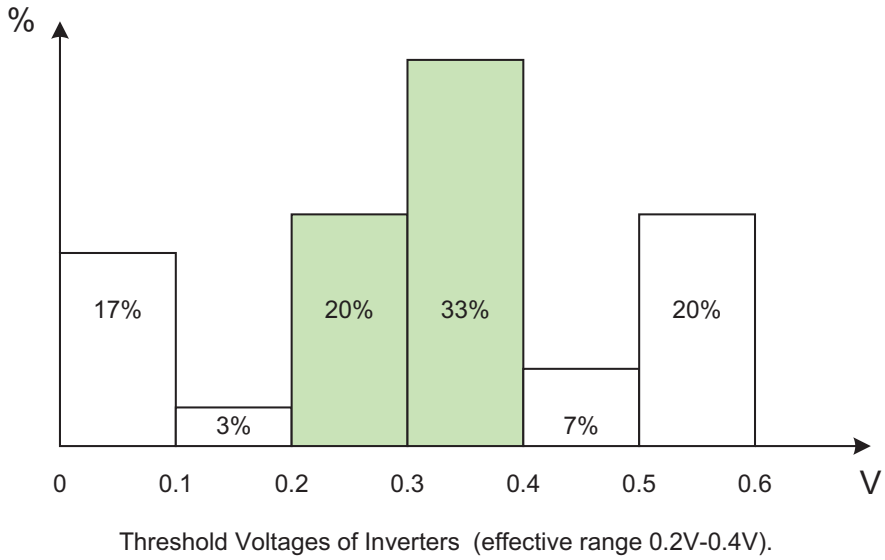

FIGURE 6.17: Distribution of threshold voltages of inverters consisting of the proposed SPICE3 CNT transistor model with various Fermi levels.

TABLE 6.5: Performance of inverters consisting of the proposed SPICE3 CNT transistor model with randomly generated Fermi levels.

n-type CNT E_F (eV)	**p-type CNT** E_F (eV)	**Inverter** V_T (V)
-0.3296	0.2937	0.34
-0.32	0.398	0.16
-0.3836	0.3376	0.39
-0.101	0.1929	0.27
-0.6948	0.2081	0.6
-0.2344	0.4087	0.09
-0.1409	0.13	0.3
-0.1738	0.4762	0.02
-0.2044	0.4338	0.06
-0.3119	0.1557	0.4
-0.1846	0.2669	0.25
-0.2062	0.0824	0.36
-0.3711	-0.1205	-
-0.3955	0.5173	0.05
-0.3792	0.2163	0.47
-0.615	0.3855	0.6
-0.3668	0.3668	0.3
-0.2963	0.3243	0.27
-0.257	0.1192	0.36
-0.0313	0.1306	0.27
-0.3902	0.2451	0.47
-0.1954	0.0828	0.34
-0.1602	0.1088	0.32
-0.1318	0.6145	0
-0.5184	0.3311	0.58
-0.2776	0.0765	0.39
-0.2724	0.3118	0.26
-0.5216	0.0943	0.6
-0.4684	0.0501	0.58
-0.1035	0.2678	0.22

Another set of simulations of pass-transistor logic 1-bit full adders, which contain 16 n-type CNT transistors and 2 inverters, was carried out. Similarly to the Fermi level variation analysis of inverters, the Fermi level of each CNT transistor in the full adder was randomly calculated using the Gaussian Distribution algorithm in MATLAB. The simulation results showed that five out of thirty adders performed functionally and the percentage of correctly working units with Fermi level variation was approximately 17%. The failure rate of full adders is higher than that of inverters, which implies that circuits

with a larger number of CNT transistors are more likely to fail with parameter variation. The simulation results of this research demonstrate that the Fermi level variation of CNT transistors can affect the performance of CNT devices.

6.4 Concluding Remarks

This chapter has described two implementations of the proposed CNT transistor models in SPICE. Firstly an HSPICE implementation of the CNT transistor macromodel based on the cubic spline approximation of non-equilibrium mobile charge densities is presented. Non-ballistic effects, including elastic scattering and the strain effect, were implemented in both n-type and p-type HSPICE macromodels. The performance of the the macromodel was compared with the results of behavioural-level simulation [32] and recently published experimental measurement [164]. The comparison results showed that the accuracy of the proposed HSPICE implementation was superior to that of the state-of-the-art CNT HSPICE macromodel developed at Stanford University [13, 14], with nearly 17% smaller RMS error, while maintaining similar simulation speed. An efficient SPICE3 CNT transistor model was also developed. Single transistors and logic circuits based on the implemented SPICE3 CNT transistor model, including inverters, SRAM cells and 1-bit full adders, were simulated and they all performed as expected while requiring little CPU time. This showed great potential for the proposed SPICE3 model to analyse circuits with a large number of CNT transistors. Simulation results also showed that the SPICE3 model could work with low supply voltages while maintaining high operation speed (approximately 40 times faster than HSPICE macromodels). The power consumption per switch of the CNT-based SRAM cell and adder was estimated and compared with that of circuits based on conventional silicon MOS3 models in SPICE3. Comparison results showed that circuits based on the developed SPICE3 CNT transistor model consume much less power (nearly 90%) than the MOS3 devices, which implies the potential of CNT transistors in low power applications. The effect of parameter variation was discussed. Simulation of logic circuits, including inverters and PTL 1-bit full adders, consisting of CNT transistors with randomly generated Fermi levels were carried out. Simulation results indicated the Fermi level variation may cause

failure of CNT devices and demonstrated that the proposed SPICE3 model is capable of capturing the effect of parameter variation on CNT based logic circuit performance.

Chapter 7

Conclusions and Future Research

One of the most promising nano devices is the carbon nanotube transistor [105]. Ideal CNT transistor based logic circuits can provide significant energy and performance benefits over silicon CMOS. This represents the motivation for CNT transistor based devices and applications in logic circuit design. Nano devices suffer from high defect rates and material variation due to the fundamental limitation of the fabrication processes. To understand quantitatively the impact of defects and variation on the electrical characteristics of CNT transistor based devices and their applications in circuit design, computer models for CNT transistors play an important role. The contributions presented in this thesis provide fast and accurate simulation models for CNT transistors including ballistic and non-ballistic transport effects based on numerical solution of the theoretical CNT mobile charge density equations. A summary of the contributions is given in the next section followed by proposed future work.

7.1 Thesis Contributions

In Chapter 2 the state of the art of electronic CNT devices modelling was investigated and studied in order to provide ideas for an efficient modelling technique for CNT transistors. The overview of the electronic characteristics of CNTs, traditional modelling approaches for CNT devices and issues existing in reported CNT transistor models provided an inspiration for this research on new CNT transistor models.

The simulation of models that numerically describe the characteristics of devices has two key parameters: accuracy and simulation time. Over the last ten years, numerous CNT transistor models have been developed [11, 12]. In these models, numerical integrations and iterations were eliminated when calculating the charge densities of the CNT transistor, leading to a significant speed-up in model simulation ($>$ 100 times faster than FETToy [16]). New, fast ballistic CNT transistor models based on numerical approximation of non-equilibrium mobile charge densities of CNTs were proposed. With respect to the piece-wise linear and quadratic polynomial approximation based models introduced in Chapter 3, the numerical piece-wise approximations replaced complicated calculations in traditional modelling techniques and resulted in fast and efficient models which can be developed further for implementation in SPICE-like circuit simulators. The transport performance of the piece-wise approximation based models were compared with previously reported simulation results and it was demonstrated that the proposed linear and quadratic approximation techniques led to a dramatic computational cost saving without sacrificing the accuracy of the model. For example, Section 3.3.2 demonstrated that the developed CNT transistor model with 4-piece quadratic approximation of mobile charge densities can achieve more than three orders of magnitude speed-up ($\sim$ 1100 times) than FETToy [16], while maintaining normalised RMS error not exceeding 4%.

In Chapter 4, cubic spline approximation was used in the calculation of the mobile charge densities of CNT transistors. The spline algorithm can automatically generate matching approximation with higher speed than the piece-wise approximation techniques introduced in Chapter 3. Based on the numerical model implemented in MATLAB, both n-type and p-type CNT transistor models were developed using VHDL-AMS and the behavioural-level performance of the developed model was analysed. Simulation results show that the cubic spline approximation based model leads to a simulation speed-up of up to two orders of magnitude compared with FETToy [16] with RMS errors of less than 3%. Moreover, an inverter based on these VHDL-AMS models was simulated and its functional performance was analysed. Simulation results showed that although the cubic spline approximation based model requires more simulation time in the modelling calculation process, it has higher accuracy than the piece-wise approximation based model when compared with theoretical models [16]. Both the numerical piece-wise and cubic

spline approximation based models significantly improve the efficiency of simulating the ballistic transport in CNT transistors.

The numerical approximation of non-ballistic transport characteristics was also a significant part of this work as discussed in Chapter 5. The existence of defects, energy barriers, scattering effects and a number of other non-ballistic transport properties cannot be ignored when analysing the performance of a carbon nanotube transistor. In this research, four main non-ballistic transport effects, including elastic scattering, strain effect on the band gap, tunnelling effect and phonon scattering, were added to the proposed cubic spline based models. A new MATLAB model named $FETToy+$ was developed to allow analysis of both ballistic and non-ballistic transport of CNT transistors. The accuracy of the spline based non-ballistic $FETToy+$ model was compared with experimental results. For example, Section 5.3 showed that the simulated drain current of the n-type $FETToy+$ model with $d = 1.6nm$, $t_{ox} = 50nm$, $T = 300K$ and $E_F = -0.05eV$ had a good correlation with the experimental data [164] with RMS errors of less than 20%.

Using the developed numerical models, SPICE compatible models were developed and corresponding circuit-level implementation of the proposed models was carried out in Chapter 6. HSPICE and Berkeley SPICE3 were used for the SPICE-level implementation of the CNT transistor models. Firstly, n-type and p-type HSPICE macromodels of non-ballistic CNT transistors based on the cubic spline approximation of CNT mobile charge densities were developed. Due to syntax limitations of the HSPICE macromodelling language, not all non-ballistic effects discussed in Section 5.1 were added in the model, while elastic scattering and strain effect were developed. The performance of the macromodel was compared to that of the previously reported Stanford HSPICE models [13, 14] and to experimental results [155] respectively. Comparison results showed that the proposed HSPICE macromodel performed more accurately than the Stanford model [13, 14] with approximately 11% smaller RMS error while maintaining similar simulation time.

SPICE3 models of both n-type-like and p-type-like CNT transistors were implemented by developing and incorporating necessary C modules into the Berkeley SPICE3 source code and recompiling the simulator for Linux platforms. Not only do the proposed

SPICE3 models support extensions of components compared with the HSPICE macro-models, they also operate faster ($\sim$ 40 times) in simulation. The speed efficiency makes the SPICE3 models particularly suitable for simulation of circuits consisting of large numbers of transistors. CNT based logic circuits based on the developed SPICE3 model including inverters, SRAM cells and full adders were simulated. The power consumption per switch of the CNT-based SRAM cell and adder was estimated and compared with that of circuits based on conventional silicon MOS3 models in SPICE3. Comparison results showed that circuits based on the proposed SPICE3 CNT transistor model consume much less power ($\sim$ 90%) than the MOS3 devices, which implies the potential of CNT transistors in low power applications. Finally, variation analysis of logic circuits, including inverters and full adders, consisting of CNT transistors with randomly generated Fermi levels was carried out and the percentage of working circuits out of all simulated circuits was calculated to demonstrate the feasibility of using the developed SPICE3 models for parameter variation and defect analysis. Simulation results shown in Section 6.3 demonstrated that nearly half ($\sim$ 53%) of the simulated inverters functioned with Fermi level variation.

The contributions presented in this thesis proposed novel, efficient and accurate CNT transistor models based on the approximation of mobile charge densities of CNT transistors, while implementing both ballistic and non-ballistic transport characteristics and analysing the performance of CNT transistor based logic circuits. The contributions made in this thesis are supported by extensive analysis of transport characteristics of CNT transistors, modelling languages and the use of computer-aided simulation tools. It is expected that the modelling techniques developed in this thesis will make useful contributions towards the development of future CNT based circuit design.

7.2 Directions for Future Work

Carbon nanotube transistor modelling has a number of areas which may be subject to further development. So far this research has focused on modelling the channel current properties of the CNT transistor, and the models developed in Chapters 3 and 4 only

consider the inner transistor characteristics. However, to develop a model suitable for SPICE simulators, more peripheral effects of CNT transistors, including parasitics, p-n junctions and substrate leakage [49, 95], need to be implemented. With peripheral effects added, the CNT transistor model may describe both the inner transport characteristics and the interaction between transistors in circuit-level simulation.

In Chapter 5, four non-ballistic transport effects, elastic scattering, strain effect on the band gap, tunnelling effect and phonon scattering effect, were analysed and implemented in the proposed CNT transistor models. However, more non-ballistic transport effects of CNT transistors including Schottky contacts and doping effects [91, 120] may significantly affect the performance of CNT transistors. Therefore, further analysis of the impact of such transport effects on the performance of CNT transistors needs to be established and numerical expressions representing these effects are expected to be developed.

Following the development of SPICE-level models which can simulate the DC performance of CNT transistors in Chapter 6, AC and transient analysis of the model would be valuable extensions of this research. Current experiments [90, 117] have illustrated the AC performance of CNTs, and models with AC and transient simulation features would be necessary for CNT circuit design.

As part of this Ph.D. programme, this research attempted a Fermi level variation analysis of the proposed SPICE3 model in Section 6.3. Considering that CNT fabrication techniques are not yet mature and the electronic characteristics of CNT transistors are not uniform [25, 150, 171], defect and variation analysis is of significant importance for CNT device modelling and thus needs further study. It is known that with different channel diameters, the threshold voltages of CNT transistors may vary [144, 145], which shows the potential of applying CNT transistors in multi-valued logic circuits. Furthermore, issues such as how to control the diameter of a CNT in synthesis are yet to be solved.

Appendix A

Published Papers

This appendix lists all papers published during the course of this research.

1. Tom J. Kazmierski, Dafeng Zhou, Bashir M. Al-Hashimi, "A Fast, Numerical Circuit-Level Model of Carbon Nanotube Transistor", Nanoscale Architectures, 2007. NANOSARCH 2007. IEEE International Symposium on, pp.33-37, 21-22 Oct. 2007.

2. Tom J. Kazmierski, Dafeng Zhou, Bashir M. Al-Hashimi, "Efficient circuit-level modelling of ballistic CNT using piecewise non-linear approximation of mobile charge density", DATE08, Munich, Germany, pp.146-151, Mar. 2008.

3. Dafeng Zhou, Tom J. Kazmierski, Bashir M. Al-Hashimi, "VHDL-AMS implementation of a numerical ballistic CNT model for logic circuit simulation", Forum on Specification, Verification and Design Languages, 2008. FDL 2008, pp. 94-98, 23-25 Sept. 2008.

4. Tom J. Kazmierski, Dafeng Zhou, Bashir M. Al-Hashimi, Peter Ashburn, "Numerically efficient modeling of CNT transistors with ballistic and non-ballistic effects for circuit simulation", IEEE Transactions on Nanotechnology, vol. 8, 10 Mar. 2009.

5. Tom J. Kazmierski, Dafeng Zhou, Bashir M. Al-Hashimi, "HSPICE implementation of a numerical CNT transistor model for I-V characteristics simulation",

Forum on Specification, Verification and Design Languages, 2009. FDL 2009, 22-24 Sept. 2009.

Appendix B

Implementation of CNT Transistor Models in the Research

Computer aided modelling languages and tools including MATLAB, VHDL-AMS, HSPICE and Berkeley SPICE3 were utilised to implement the proposed CNT device models in this thesis. In the following, the functional structure of each developed model is described. All these model archives have been published on the Southampton Carbon Nanotube Transistor Modelling website [163].

B.1 MATLAB Functions to Implement CNT Transistor Models

This section presents the MATLAB functional structures of the models developed in this project. Section B.1.1 describes the MATLAB functions to implement the ballistic cubic spline based CNT transistor model described in Chapter 4. Then in Sections B.1.2 and B.1.3 the functional structures of both FETToy model with non-ballistic effects and *FETToy+* based on cubic spline approximation of non-equilibrium charge densities proposed in Chapter 5 are introduced respectively.

B.1.1 MATLAB Functions to Implement Ballistic Cubic Spline Based CNT Transistor Model

Table B.1 lists the MATLAB function files for the implementation of the CNT transistor model based on cubic spline approximation of mobile charge densities. Input and output are set and parameters required by the CNT transistor model are also defined in the top level function archive $I\_CNT\_vsc.m$. In simulation, when the input terminal voltages V_G, V_D, and V_S are given, interior functions are invoked to implement the cubic spline approximation of mobile charge densities and return V_{SC} to the top level function, in which drain-source current is computed and plotted out.

TABLE B.1: MATLAB function files for the proposed ballistic CNT transistor model based on cubic spline approximation of mobile charge densities.

Function Name	**Description**
I_CNT_vsc.m	Top level function of the proposed ballistic model.
N_CNT.m	Interior function to derive the equilibrium mobile charge density.
Fvsc.m	Interior function to compute the self-consistent voltage.
Uscfall.m	Interior function to obtain spline approximation of mobile charge densities.
Fsy.m	Interior function to calculate the cubic spline coefficients.

B.1.2 MATLAB Functions to Implement FETToy with Non-Ballistic Effects

Table B.2 shows the MATLAB function files implementing the FETToy model with non-ballistic effects. The calculation of V_{SC} in this model is based on the iterative Newton-Raphson algorithm, which is the same as in the original FETToy [16]. However, with numerical equations representing the non-ballistic transport effects described in Section 5.1, the extended FETToy model can describe the non-ballistic transport of CNT transistors.

B.1.3 MATLAB Functions to Implement *FETToy+*

It can be seen from Table B.3 that the functional structure of *FETToy+* model is similar to that of the ballistic cubic spline based model. Both of them are built based on

TABLE B.2: MATLAB function files for the FETToy model with non-ballistic effects.

Function Name	**Description**
enhancedFETToy.m	Top level function of extended FETToy with non-ballistic effects.
N_CNT.m	Interior function to derive the equilibrium mobile charge density.
Fvsc.m	Interior function to calculate V_{SC} using Newton-Raphson method.

the cubic spline approximation of mobile charge densities so the calculation functions $Fsy.m$, $Uscfall.m$ and $Fvsc.m$ are the same. However, by implementing the numerical equations describing the non-ballistic transport effects in the top level function $I\_CNT\_effects.m$, *FETToy+* can capture the non-ballistic transport of CNT transistors.

TABLE B.3: MATLAB function files for *FETToy+*.

Function Name	**Description**
I_CNT_effects.m	Top level function of *FETToy+*.
N_CNT.m	Interior function to derive the equilibrium mobile charge density.
Fvsc.m	Interior function to compute the self-consistent voltage.
Uscfall.m	Interior function to obtain spline approximation of mobile charge densities.
Fsy.m	Interior function to calculate the cubic spline coefficients.

B.2 VHDL-AMS Functions to Implement Ballistic CNT Transistor Model

Table B.4 shows the VHDL-AMS functions which implement the proposed cubic spline approximation based CNT transistor model and lists their descriptions. The files listed in the table should be used as a whole package to simulate the proposed model. This model has been verified using Mentor Graphics SystemVision Professional 4.4 and 5.5. In the top level package $CNTtransistor.vhd$, the ports definitions including drain, gate, source, and bulk for the CNT transistor model are the same as for a typical MOS transistor in VHDL-AMS. To simulate this model, the coefficient library file (coefficient.vhd) needs to be generated from $Fsy.m$ in MATLAB and then invoked to calculate the cubic spline

approximation of mobile charge densities.

TABLE B.4: VHDL-AMS function files for the proposed cubic spline approximation based model.

Function Name	**Description**
CNTTransistor.vhd	Top level function of the proposed model.
cntcurrent.vhd	Interior function to calculate the drain current characteristics.
coefficient.vhd	Library of coefficients generated by Fsy.m.
FindQRange.vhd	Interior function to obtain spline approximation of mobile charge densities.
SolveVscEquation.vhd	Interior function to calculate the self-consistent voltage.
testbench.vhd	Sample VHDL-AMS testbench of the proposed transistor model.
v_pulse.vhd	Pulse voltage source.
v_source.vhd	Constant voltage source.

B.3 HSPICE Archives to Implement CNT Transistor Model

Table B.5 lists HSPICE archives to implement the CNT transistor macromodel based on spline approximation of mobile charge densities which is described in Section 6.1, Chapter 6. This macromodel is developed in the form of external libraries which can be invoked by the HSPICE simulator. *CSmodel.lib* contains functions to describe the transport characteristics of the proposed CNT transistor model including elastic scattering and strain effect, while *param.lib* provides parameter values required by the developed macromodel.

TABLE B.5: HSPICE archives to implement the proposed cubic spline based CNT transistor macromodel.

Archive Name	**Description**
CSmodel.lib	Function describing the transport characteristic of the proposed macromodel.
param.lib	Parameter library of the HSPICE macromodel.
cntmodel.sp	Sample HSPICE testbench of the developed transistor macromodel.

B.4 Berkeley SPICE3 Library Structure

In this thesis, the SPICE3 non-ballistic CNT transistor model is implemented for an i386 Linux environment (SUSE10.0 and Fedora10 verified in this research). In the *spicelib* library of SPICE3 source code, there are catalogs including device models, sample netlists, parser definitions and instruction documentation. In the library of models, most fundamental semiconductor devices including resistors, capacitors, inductors, diodes, transistors and sources are all included. The structure tree of the device library is illustrated in Figure B.1. It can be seen from this structure tree that the device models are located in the library named *devices* where the proposed CNT transistor model should be added by creating a new subfolder with the name *cnt*.

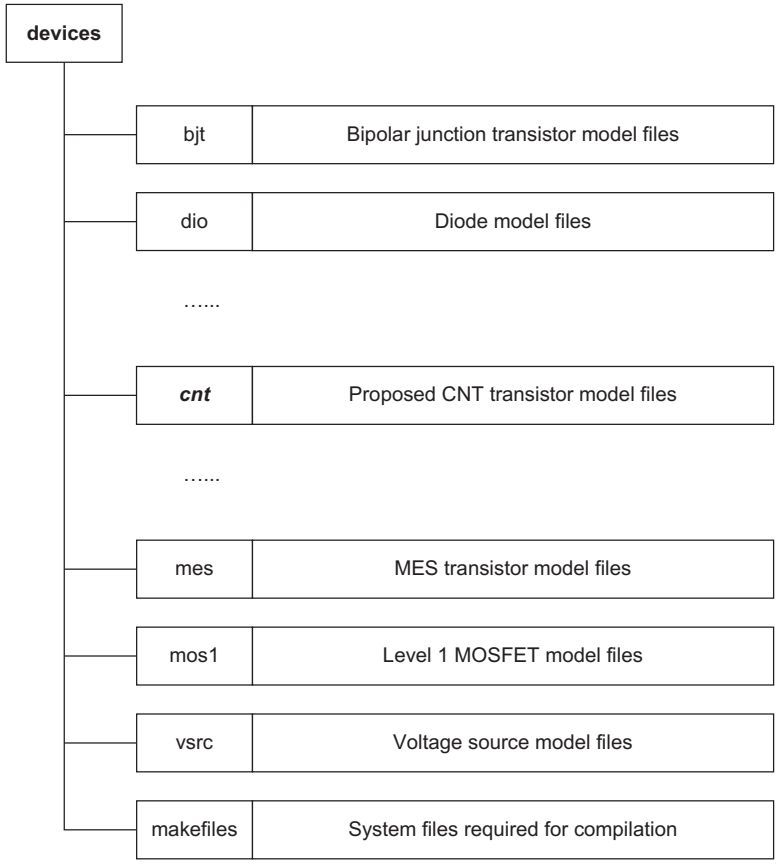

FIGURE B.1: Schematic of the SPICE3 *devices/* folder file structure tree.

Following the implementation of the proposed non-ballistic CNT transistor model in the SPICE3 library of devices, the configuration files of SPICE3 need to be modified to make the new CNT library compilable. The path routing the developed CNT library needs

to be recognised by SPICE3. Below are listed the files in which necessary statements about the path should be added:

```
spice3/configure.in
spice3/makefile.am
spice3/src/spicelib/parser/inp2m.c
spice3/src/spicelib/parser/inpdomod.c
spice3/src/spicelib/devices/dev.c
spice3/src/spicelib/devices/makefile.am
spice3/src/spicelib/makefile.am
spice3/src/makefile.am
```

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