High speed silicon optical modulator with self aligned fabrication process

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Abstract: With the imminent commercialisation of silicon photonic devices comes the requirement for a fabrication process capable of high yield and device performance repeatability. The precise alignment of the different elements of a device can be a major fabrication challenge for minimising performance variation or even device failure. In this paper a new design of high speed carrier depletion silicon optical modulator is introduced which features the use of a self-aligned fabrication process to form the pn junction. Experimental results are presented from an initial fabrication run, which has demonstrated a 6dB modulation depth at 10Gbit/s from a 3.5mm long device.

OCIS codes: (130.4110) Modulators; (060.4080) Modulation.

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1. Introduction

Silicon photonics has been a highly active area of research in recent years. The result of this is the rapid development of the photonic building block components which facilitate a range of applications. One such component which has seen significant development is the high speed silicon based optical modulator, so much so that silicon based devices in certain application areas are now appearing on the market [1]. Less than a decade ago devices generally reported bandwidths limited to the MHz regime, due to the device size and use of carrier injection to electrically control the effective index of the propagating optical mode. Nowadays the majority of modulators still operate via the plasma dispersion effect but use either carrier depletion or carrier accumulation techniques which are not limited by minority carrier recombination lifetimes. Most silicon based optical modulators reported in the previous few years have bandwidths which are compatible with data transmission rates of 10Gb/s [2–12] and even 40Gb/s [13]. A common design feature of many of these devices is a vertical pn junction within the waveguide [2,3,7,9–12] and whilst impressive performance has been demonstrated, they require precise alignment of the junction within the waveguide. The next era of silicon modulator development is likely to involve the integration with other photonic and electronic components together with further product commercialisation. Consequently other building block metrics will emerge with greater importance, one example being the ease and cost of fabrication. Alignment variations are an unavoidable characteristic of semiconductor fabrication processes, and can result in device performance variations and a reduction in yield. One challenge in the fabrication of carrier depletion silicon based optical modulators is the precise alignment of the pn junction within waveguide. Self-aligned processes have been successfully employed in the CMOS industry for many years to eliminate alignment errors and to minimise performance variations. In this paper we introduce a new design of carrier depletion based silicon optical modulator for which a self aligned process can be used to form the pn junction. Experimental results obtained from an initial fabrication batch have demonstrated data transmission at 10Gbit/s with 6dB of modulation depth from a 3.5mm phase shifter.

2. Device design and fabrication

A cross-sectional diagram of the device is shown in Fig. 1. Initial device designs were incorporated into waveguides of height 220nm, width 450nm and slab height 50nm. Within the phase modulator the rib region and slab region to one side of the rib are doped lightly p type. The slab region on the other side of the rib is then doped lightly n type. The slab regions doped n and p type then abut highly doped n and p type regions respectively to allow the formation of resistive contacts with electrodes used to drive the device, thus forming a pn diode. The concentration of the lightly doped n type region is sufficiently larger than the lightly doped p type region such that with the diode under reverse bias, free carrier depletion occurs mainly in the waveguide. A separation of 675nm was used between the rib edge and the highly doped regions in the first fabrication batch. Coplanar travelling waveguide (CPW) electrodes are used to drive the modulator at high speed. The CPW were designed to have a characteristic impedance of 50Ω taking into account the effects of the diode capacitance. S parameter measurements performed on fabricated devices have demonstrated a reflected signal below −20dB over the frequency range 100MHz to 40GHz.

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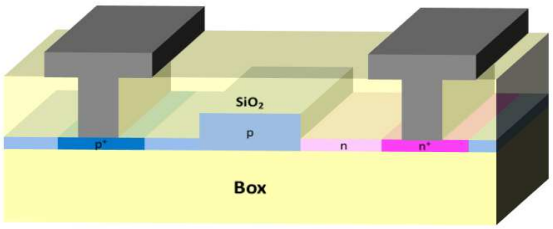

Fig. 1. – Cross sectional diagram of phase modulator

The devices are incorporated into Mach Zehnder Interferometers (MZI) to translate from phase to intensity modulation. Asymmetric MZI structures are used for ease of modulator characterisation; however symmetrical structures could equally be used to avoid wavelength and thermal sensitivity. Compact MMI structures are used to perform the splitting and combining function within the MZI. Phase modulators are formed in both arms of the MZI to balance the optical power and therefore allow for a large extinction ratio, however only one arm is driven at a time.

Device fabrication was performed in 200mm microelectronics clean room of CEA-LETI. Devices are formed in 220nm overlayer SOI wafers from SOITEC, which has a 2um thick buried oxide layer. As mentioned above, one of the main features of this device is the use of a self aligned process to form the pn junction. These process steps are depicted in Fig. 2. The active region of the device is firstly implanted with boron to form a lightly doped p type region. A SiO_2 layer is then deposited onto the wafer surface and etched through a resist mask with the waveguide pattern defined by DUV lithography. This layer firstly acts as a hard mask through which to etch the optical waveguides. The remaining SiO_2 hard mask is then used together with a resist defined implant window to form the n type region at the side of the rib. Since one edge of the phosphorus implanted region butts up against the side of the waveguide, the second edge of the resist implant window can be approximately aligned anywhere on top of the waveguide. This crucial step in the process is therefore self-aligned to the edge of the waveguide. The remaining process steps used to form the highly doped regions and contacts are performed using standard CMOS processes. In future device iterations self-alignment of more steps will also be possible, making the design even more robust against typical fabrication tolerances. Some images of an example fabricated device are shown in Fig. 3.

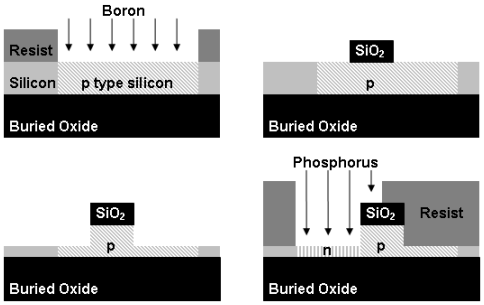

Fig. 2. – Self alignment of pn junction

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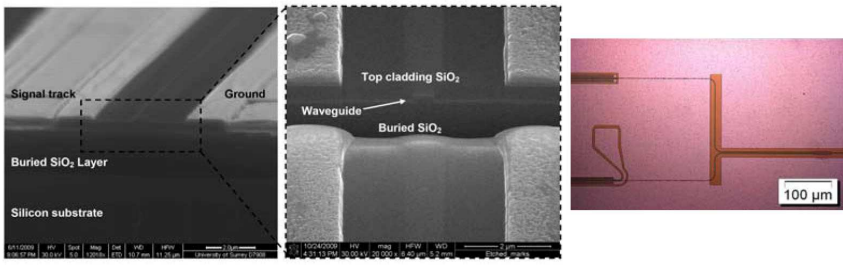

Fig. 3. – Scanning electron microscope images of the device cross section (left and centre), optical microscope image of the MZI end (right)

3. Experimental results

After fabrication, devices were tested in the high speed characterisation facility at the University of Surrey. Surface gratings were used to couple light to and from the optical waveguides. An Agilent 81940A tunable laser source of wavelength range around 1550nm was used at the input side of the device and Agilent 81634B detector used at the output side for DC measurements. To access the DC extinction ratio and efficiency of the modulators the wavelength of the source was scanned and output power monitored to reveal the characteristic asymmetric MZI response. The MZI output power was then normalised to the output power of a straight waveguide of identical length to factor out the wavelength dependence of the grating couplers. A typical result achieved is as shown in Fig. 4, which is the response of an MZI with 3.5mm phase shifters in each arm. The MZI structure has a static extinction ratio of almost 40dB; this allows for large DC extinction ratios to be achieved with a modest drive voltage-length product. The DC modulation is assessed by analysing the shift in the wavelength response of the MZI with different reverse bias voltages applied across the diode. Also shown in Fig. 4 is the spectral response of the device with 3V, 6V and 9V reverse bias voltages. It can be seen that if operating close to the null on the 0V curve, approximate DC extinction ratios of 25dB, 31dB and 33dB are achieved with a 3V, 6V and 9V reverse bias voltages respectively, however since this is at the null of the MZI response the corresponding loss figures at the 1 level are approximately 23dB, 16dB and 13dB respectively.

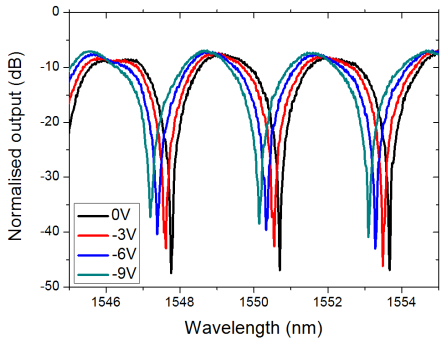

Fig. 4. - Modulator normalised spectral response

The shift in the spectral response of the MZI can be used to equate the resulting phase shift, and therefore the modulation efficiency using the following expression (1):

$$\Delta\varphi = 2\pi \frac{\Delta\lambda}{FSR}, \tag{1}$$

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where $\Delta\lambda$ is the spectral shift and FSR is the free spectral range of the MZI response. Using this expression the modulation efficiency for the device measured in Fig. 3 can be estimated to be 8V.cm. Devices elsewhere on the wafer have reported modulation efficiencies down to 6V.cm. The high speed performance of the device has been analysed by its ability to carry data at different rates. A Centellax TG1P4A and TR1D4A PRBS source and DEMUX, with an external variable clock source are used to generate 2^7-1 pattern length data streams at different data rates. The PRBS output is passed through a driver amplifier which produces a 6.5v peak-to-peak output voltage. A DC bias voltage is combined with the data signal using a bias tee to ensure that the device is always in reverse bias. High speed ground-signal-ground (GSG) probes are used to couple the RF signal to the CPW and to provide a 50Ω termination at the end of the line. The output light from the modulator is passed through an EDFA (Alnair Labs LNA-150) to boost the signal to the required input levels of the DCA (Agilent 86116C). A tunable wavelength filter is used to remove the noise from surrounding wavelengths produced by the EDFA. As shown in Fig. 5, the optical eye diagram is open at 10Gbit/s with an extinction ratio of 6dB. The normalised output power of the modulator is −15dB at the 1 level due to the operating point of the modulator. Although the eye is clearly open it is also quite distorted. If the worst case is considered (defined by the separation of the maximum-lower-rail data points and the minimum-upper-rail data points in the eye diagram) the modulation depth drops to approximately 3dB.

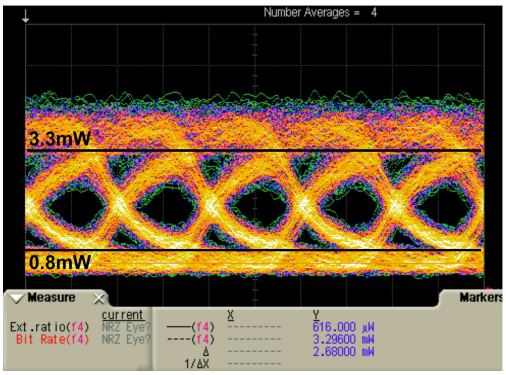

Fig. 5. – Data transmission at 10Gbit/s

Experimental characterisation of the doping levels in the fabricated devices has revealed that the DC and high speed performance of the device can be improved by optimising the implantations also the geometry. Optimisation of the design for future fabrication iterations has been performed using a combination of electrical and optical modelling packages. ATLAS a device physics modelling package from SILVACO has first been used to model the electrical behaviour of the device with a range of bias conditions. The free carrier profiles and material properties are then imported into an optical mode solver to calculate changes in effective index and propagation loss.

Table 1. – Design parameters

Parameter	Value	Units
Waveguide width	**400**	**nm**
Waveguide height	**220**	**nm**
Slab height	**100**	**nm**
N + , P + concentration	**1e20**	**Ions.cm^{-3}**
N concentration	**1.5e18**	**Ions.cm^{-3}**
P concentration	**3e17**	**Ions.cm^{-3}**
N to rib separation	**500**	**nm**
P to rib separation	**450**	**nm**

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The results of DC and transient simulations performed on a device with the parameters as listed in Table 1 are shown in Fig. 6 and Fig. 7 respectively. The modelling predicts that modulation efficiency at 3V, of 2.2V.cm is achievable and that the intrinsic dynamic response of the device is limited by a fall time of 7.4ps which corresponds to an intrinsic bandwidth in excess of 47GHz.

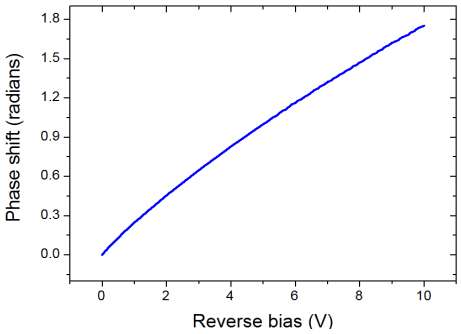

Fig. 6. – Phase shift versus reverse bias voltage for a 1.5mm phase shifter

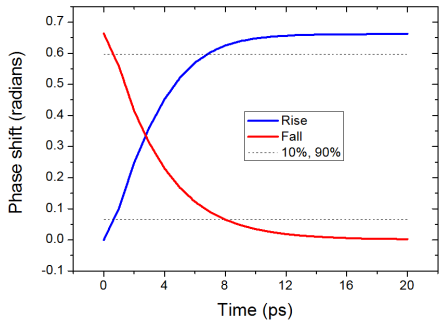

Fig. 7. – Intrinsic dynamic response of a 1.5mm phase shifter

4. Conclusion

A novel silicon optical modulator design has been introduced which uses a self-aligned process to form the pn junction in proximity of the waveguide. Experimental results from an initial fabrication run have revealed a large passive extinction ratio, which allows for large DC modulation depths when operating at the null point (albeit with a reduced optical throughput). Data transmission at 10Gbit/s has also been demonstrated with 6dB of extinction. Optical modelling has also shown that through optimisation of the doping levels and the device geometry, both the DC and the high speed performance can be significantly enhanced.

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