**Supplementary data for a detailed explanation and demonstration of the design rules presented in this work**

Section 4 of the manuscript was aimed to present a set of design rules in order for the process to be used in the fabrication of different type of applications. In this section a detailed explanation of these design rules are presented and supported with figures where suitable.

In order to fabricate a device using this process, the following design rules should be considered during the design stage. The values used in this work for the fabrication of the accelerometers are shown in parentheses where applicable:

1. SOI wafer properties:
    i. Structural layer thickness, $th_{ST}$, should be 5–70μm (50μm in this work)
    ii. BOX layer thickness is, $th_{BX}$, 0.5–5μm (2μm in this work)
    iii. Handle wafer thickness is, $th_{HL}$, 350–700μm (500μm in this work)
2. The minimum feature size is:
    i. $mfs_{ST}$ = 2μm for the structural layer (5μm in this work)
    ii. $mfs_{HL}$ =20μm for the handle wafer (40μm in this work)
3. The release holes that are used on the structural layer in order to release the devices are equally spaced from each other in all regions and distributed along a rectangular coordinate system. This is demonstrated in Figure S.1 that shows a feature to be released (blue) with a series of release holes (red) that are separated equally from each other along two orthogonal axes. The release holes have a diameter, $rh_{DIA}$, of 10–50μm (18μm in this work) and are distributed equally with a pitch, $rh_{PI}$, of 10–150μm (35μm in this work). Assuming a radial undercut profile (i.e. equal oxide etch rate in all directions), the release holes are used on any feature that is to be released and is larger than $ma_{RL} = \left(\sqrt{2} \times rh_{PI} - rh_{DIA}\right)$ along any axis.

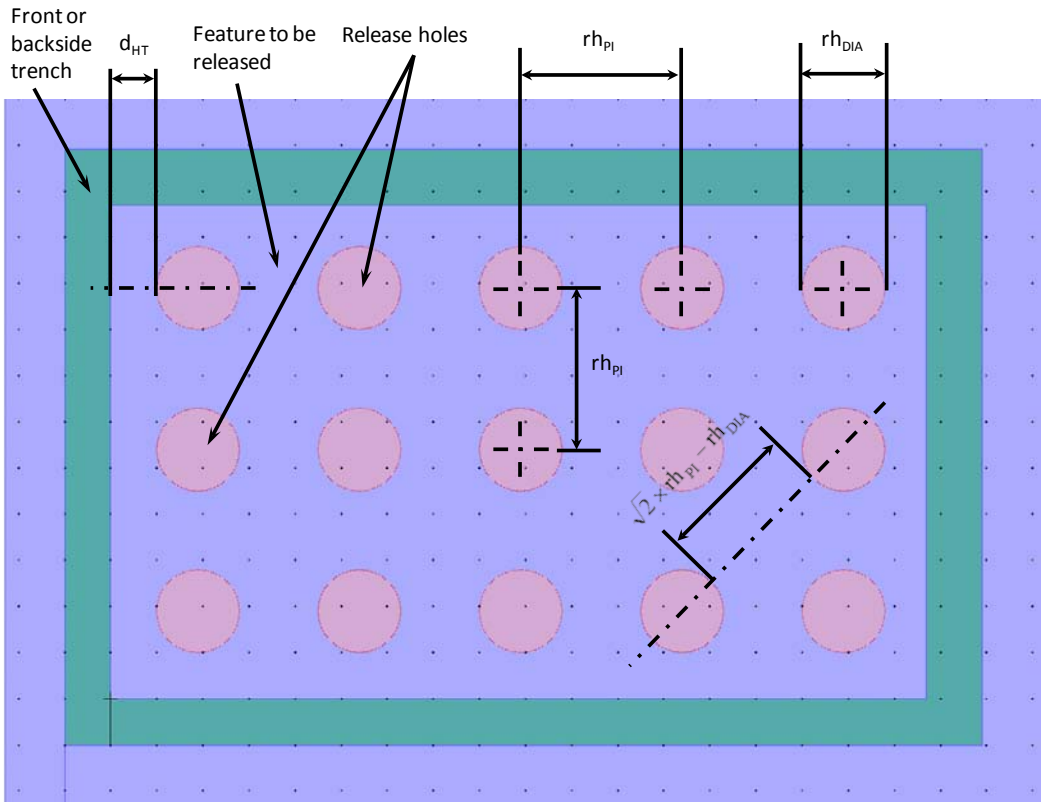


Figure S.1: Illustration of release holes (red) that are equally spaced from each other along two orthogonal axes. The feature to be released (blue) is also shown and surrounding the feature is a front or backside trench (green).

4. Different areas of a design can be released at different times to protect delicate device features or for other design considerations. This can be achieved by varying the distance, $d_{HT}$, between the outermost release holes to the front or backside trenches in different areas of the design. Figure S.1 shows an illustration of $d_{HT}$ where a feature (blue) is shown next to a front or backside trench (green). The constraints on this distance is:

   i. The minimum value of $d_{HT}$ is determined by the minimum feature size on the structural layer, i.e. 2μm (5μm in this work). However, if a region is aimed to be released at a different time compared to another region then $d_{HT}$ should be at least $\left(\left(\sqrt{2} \times rh_{PI} - rh_{DIA}\right)/2\right)$. If $d_{HT}$ were smaller, there would be no difference in release time of different regions.

   ii. The maximum value for $d_{HT}$ is determined by the maximum undercut that can be achieved using the HF VPE tool and the thickness of the BOX layer. For a standard 2μm thick BOX layer the maximum clearance is 80μm (60μm in this work).

5. The minimum size of an anchored feature, $ma_{AF}$, is 300x300μm$^2$ in order to avoid its accidental release (375x375μm$^2$ in this work).

6. Overlap between front and backside trenches should be avoided as much as possible. If this is unavoidable then the overlap area should be smaller than $\text{moa}_{\text{FB}} = 100 \times 100 \mu\text{m}^2$ ($30\text{x}50\mu\text{m}^2$ in this work) for an SOI wafer with a BOX layer thickness of 2µm. This is to avoid any cracking of the SOI wafer in the chamber of the DRIE tool due to the pressure difference between the backside and front side of the wafer. The allowed overlap value is also dependent on the thickness of the BOX layer and should be verified with the tool manufacturer where possible if another BOX thickness is intended to be used.

7. Figure S.2 shows the layout of a device (blue) that is viewed from the front side and with the backside trenches (red) overlaid. The device is surrounded by backside trenches in two different regions: 1) to define the device border (outer trench) and 2) to outline the 'handle wafer block' area (inner trench). The 'handle wafer block' after release is going to rest on the four resting areas at each corner of the device. If these areas are not large enough, the released 'handle wafer block' can slip and unintentionally move over the device features thus damaging them. For this reason, the 'handle wafer blocks' should be supported on the four corners of each device by a region with a minimum size of $\text{moa}_{\text{HW}} = 250 \times 250 \mu\text{m}^2$ ($380\text{x}380\mu\text{m}^2$ in this work). These regions provide a means of support for the released 'handle wafer block' where it would be resting upon after release.

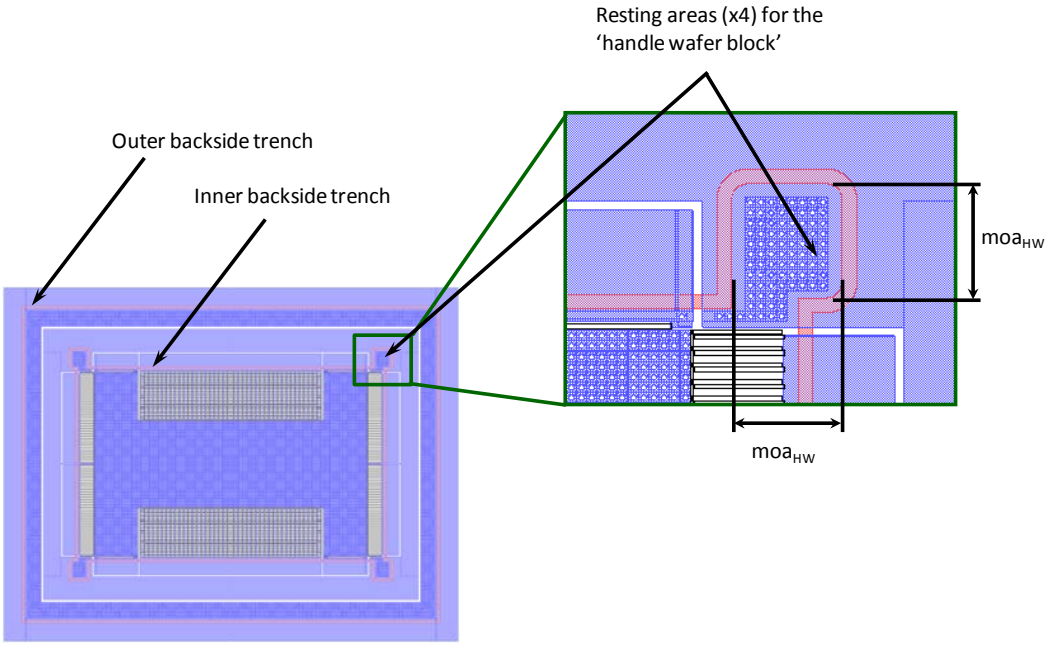


Figure S.2: Illustration of the resting areas where the released 'handle wafer' block is supported.

8. The discussion of item 7 also applies for the outer backside trench, which surrounds the device and hence defines the device border; the trench on the front side and the outer trench on the backside should have a minimum spatial offset of $\text{mso}_{\text{FB}} = 200\ \mu\text{m}$ (400µm in this work) in order to support the devices on the wafer grid. This is illustrated in

Figure S.3 that shows the spatial offset between the front side and outer backside trenches.

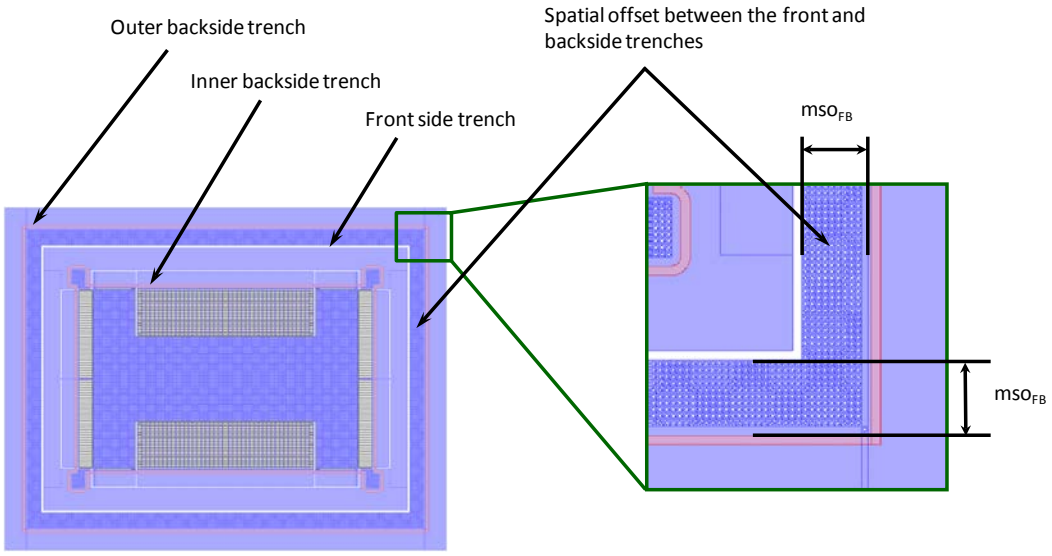


Figure S.3: Illustration of the spatial offset between the front side and outer backside trenches.

9. The wafer grid surrounding each device should be $2 \times mw_{WG} = 2 \times 400\ \mu m$ wide (2x800µm in this work), which is illustrated in Figure S.4. Ideally, the wafer grid should be designed as wide as possible as it carries the weight all the devices.

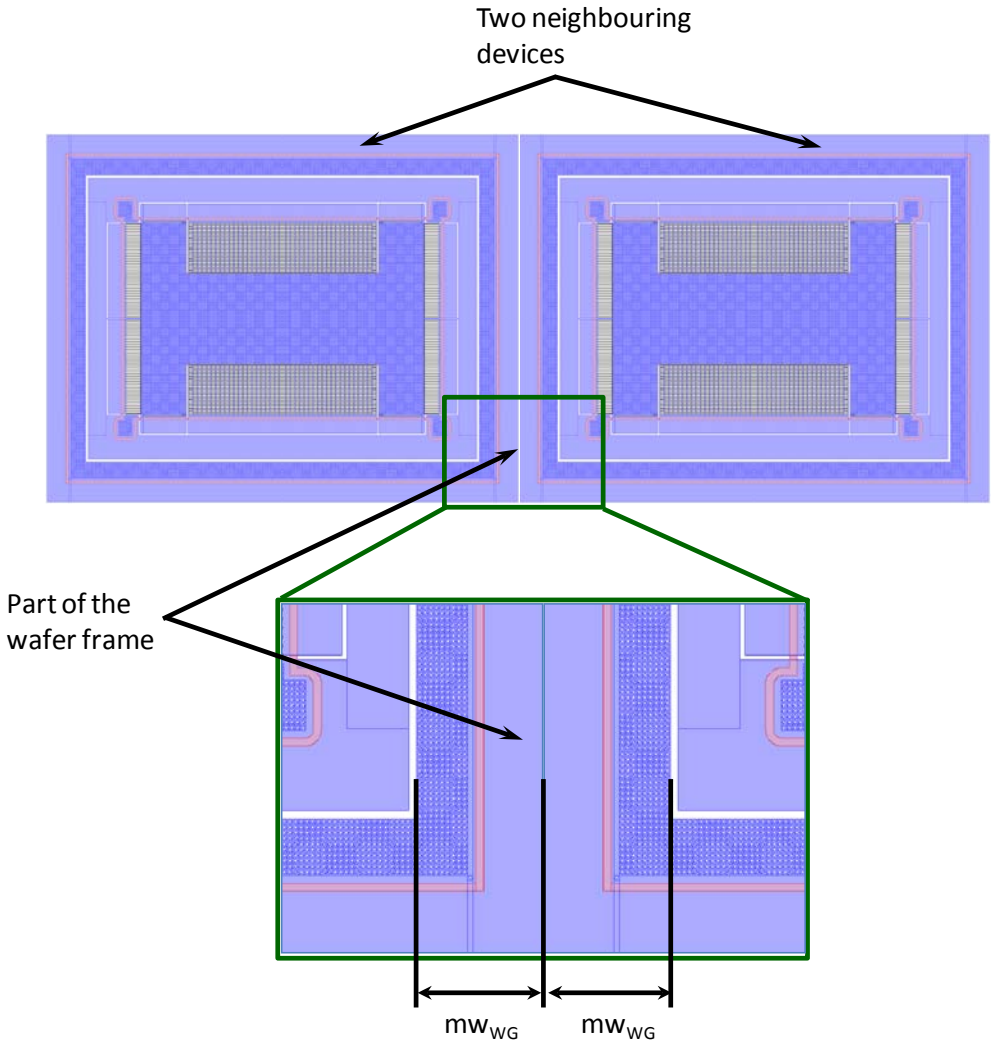


Figure S.4: Illustration part of the wafer grid that is in between two consecutive devices. The wafer grid should be at least $2 \times mw_{WG} = 2 \times 400\ \mu m$ wide in order to support the devices after release.

10. All front side trenches, $wt_{FS}$, which define the borders of the devices on the structural layer, should be minimum 5µm, maximum 100µm wide (50µm in this work).

11. All backside trenches, $wt_{BS}$, which define the borders of the devices and the 'handle wafer blocks' on the handle wafer, should be minimum 30µm, maximum 100µm wide (50µm in this work).